✧ Features

- Worldwide FM band support (64–109 MHz)
- Worldwide AM band support (520–1710 kHz)
- LW band support (153–288 kHz) (FSV4743/45 only)
- MW (520–1710 kHz) and SW (2.3–30 MHz) support (FSV4743/45 only)
- NOAA weather band support (162.4–162.55 MHz) (FSV4743 only)
- Received signal quality indicators (RSSI, SNR, frequency offset, multi-path interference)
- AM and FM programmable seek tuning
- AM and FM programmable soft mute control
- Power line noise rejection/AM lo-cut filter
- FM programmable stereo-mono blend
- AM and FM programmable channel bandwidth filters
- Digital FM stereo decoder
- Advanced patented RDS/RBDS processor (FSV4741/43/45 only)
- Automatic gain control (AGC)
- Integrated AM and FM low-noise amplifier (LNA)
- Image-rejection mixer
- Frequency synthesizer with integrated voltage controlled oscillator (VCO)
- Low-IF conversion with no external ceramic filters
- FM multipath detection and mitigation
- AM/FM noise blanker (FSV4743/45 only)
- FM Hi-cut control (FSV4743/45 only)
- 2.7 to 3.6 V supply voltage
- Programmable reference clock
- –40 to 85 ºC operation
- Digital audio output (I2S) (FSV4741/43/45 only)
- 24-pin 4 x 4 mm QFN package

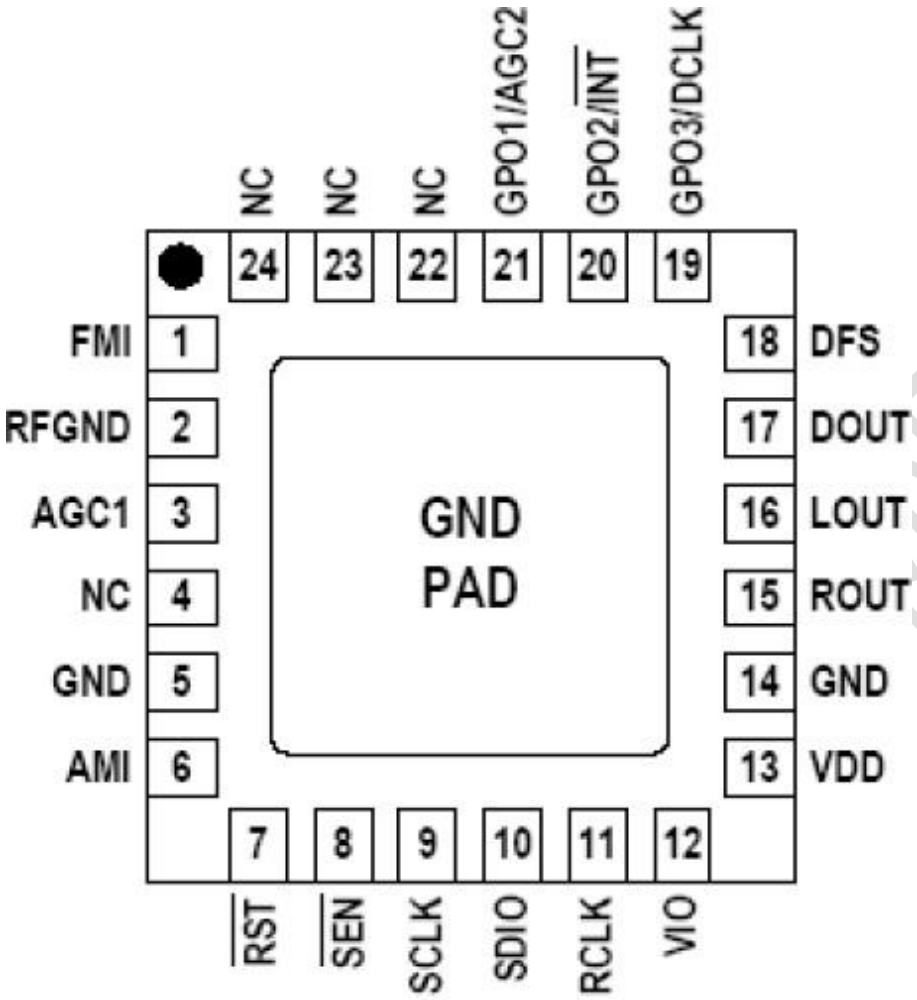
✧ Applications

- **OEM car audio systems**
- **After-market car audio systems**

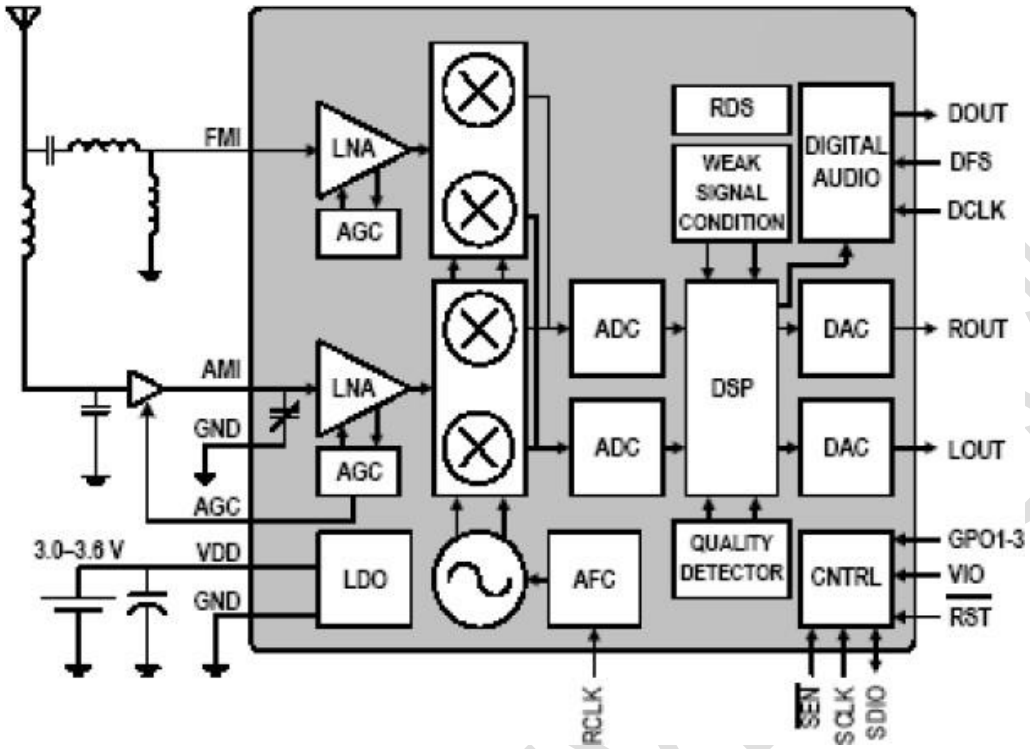
✧ Description

The FSV474x AM/FM receiver family is the most highly integrated automotive grade and performance solution available.

✧ Pin Assignment



✧ Block Diagram



✧ Pin Descriptions

Pin Number(s)	Name	Description
1	FMI	FM RF inputs. FMI should be connected to the antenna trace.
2	RFGND	RF ground. Connect to ground plane on PCB.
3	AGC	Automatic gain control.
4, 22–24	NC	No connect. Leave floating.
5, 14, GND PAD	GND	Ground. Connect to ground plane on PCB.
6	AMI	AM RF input. AMI should be connected to the AM antenna.
7	$\overline{RST}$	Device reset (active low) input.
8	$\overline{SEN}$	Serial enable input (active low).
9	SCLK	Serial clock input.
10	SDIO	Serial data input/output.
11	RCLK	External reference oscillator input.
12	V_{IO}	I/O supply voltage.
13	V_{DD}	Supply voltage. May be connected directly to battery.
15	ROUT	Right audio line output.
16	LOUT	Left audio line output.
17	DOUT	Digital output data in digital output audio mode
18	DFS	Digital frame synchronization input in digital output mode
19	GPO3/DCLK	General purpose output/Digital bit synchronous clock input in digital output mode
20	GPO2/$\overline{INT}$	General purpose output/interrupt pin.
21	GPO1/AGC2	General purpose output/AM external attenuator control.

✧ Electrical Specifications

➢ Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	—	3.6	V
Interface Supply Voltage	V_{IO}		2.7	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

➢ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI and AMI.

➢ DC CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

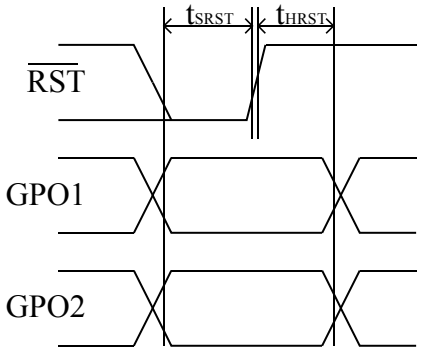
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Supply Current	I_{FM}		—	26	—	mA
WB Mode						
Supply Current	I_{FM}		—	22	—	mA
Supply Current	I_{FM}	Low SNR level	—	21	—	mA
AM Mode						
Supply Current	I_A		—	19	—	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	400	—	µA
Powerdown Current[1,2]	I_{PD}		—	10	20	µA
Interface Powerdown Current[1]	I_{IO}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	—	V
Low Level Input Voltage[3]	V_{IL}		—	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. Specifications are guaranteed by characterization.
2. Refer to Section "4.19. Control Interface" on page 35.
3. For input pins SCLK, SEN, SDIO, RST, and RCLK.
4. For output pins SDIO, DFS, GPO1, GPO2, and GPO3.

➢ Reset Timing CharacteristiFSV

(V_{DD}=2.7 to 3.6V, V_{IO}=2.0 to 3.6V, T_A=-20 to 85 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
RST Pulse Width and GPO1,GPO2 Setup to $\overline{RST}$	t_{SRST}	100	—	—	µs
GPO1,GPO2 Setup Hold From $\overline{RST}$	t_{HRST}	30	—	—	ns



➢ 2-wire Control Interface CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 - 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 - 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:
1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

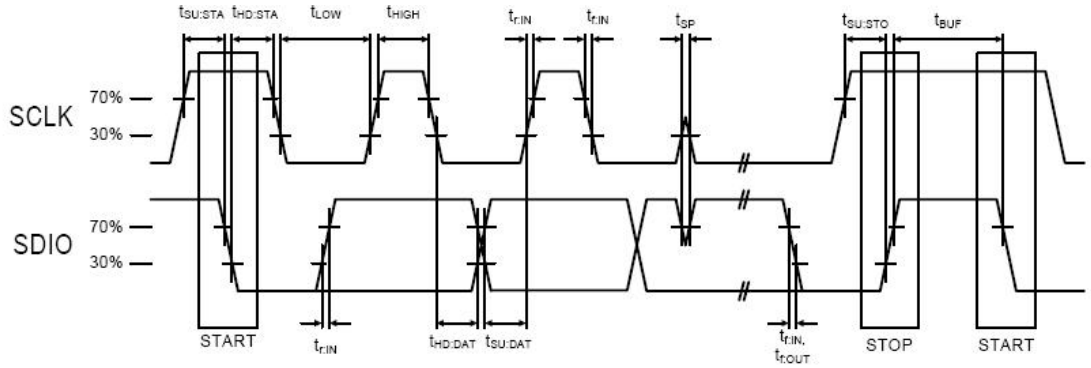


Figure 2-Wire Control Interface Read and Write Timing Parameters

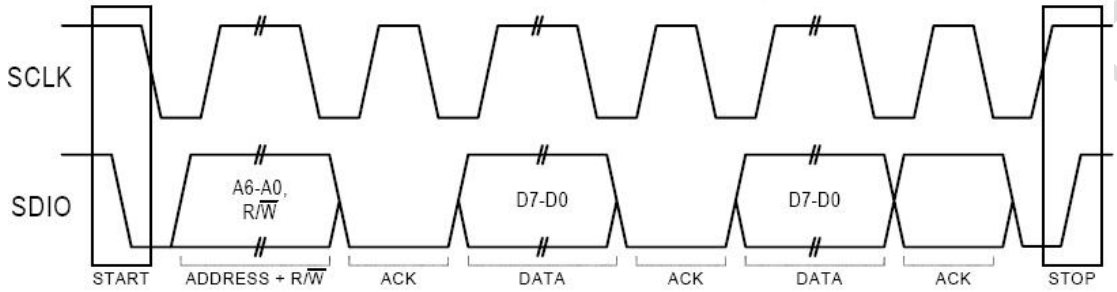


Figure 2-Wire Control Interface Read and Write Timing Diagram

➢ 3-wire Control Interface CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

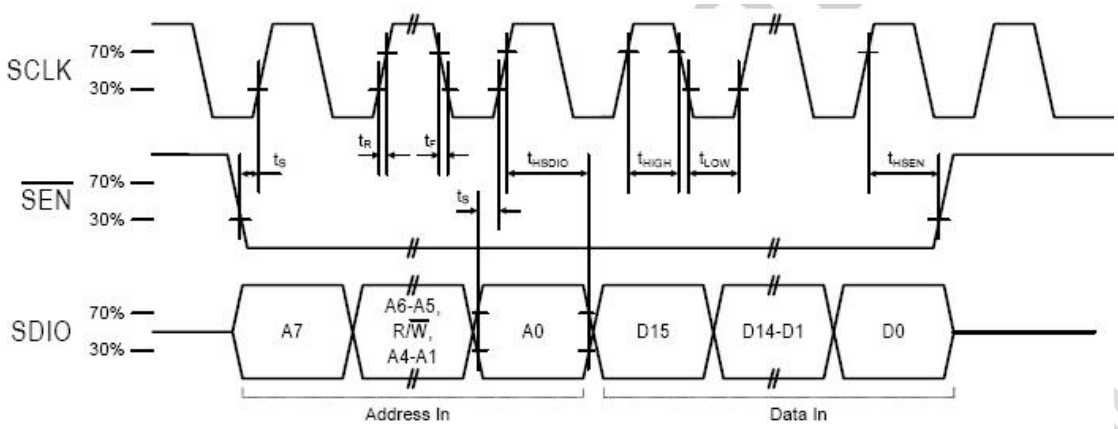


Figure 3-Wire Control Interface Write Timing Parameters

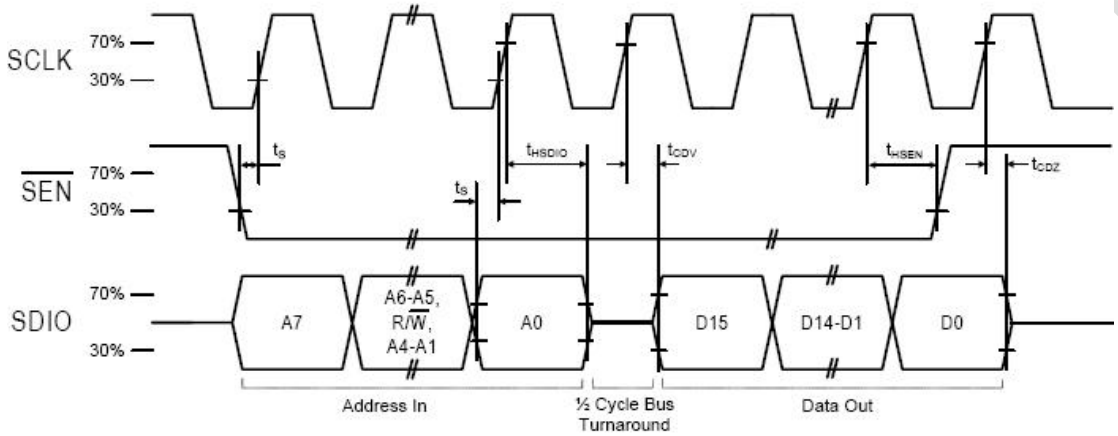


Figure 3-Wire Control Interface Read Timing Parameters

➢ SPI Control Interface CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns
Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.						

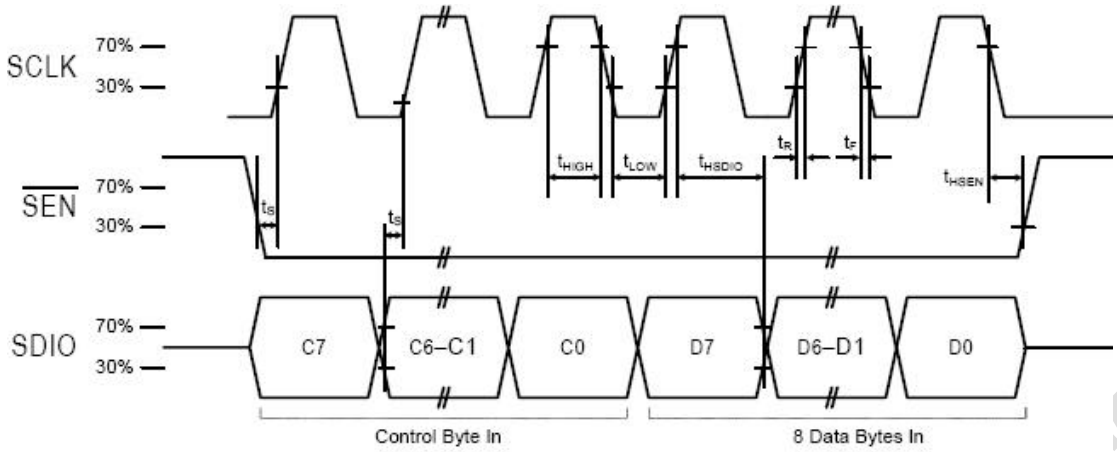


Figure SPI Control Interface Write Timing Parameters

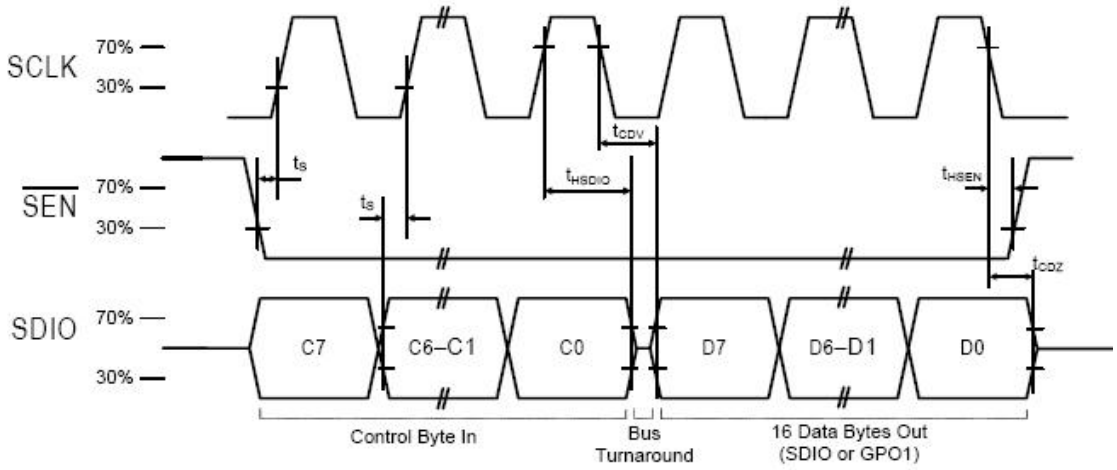


Figure SPI Control Interface Read Timing Parameters

➢ Digital Audio Interface CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns
Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.						

Digital Audio Interface Timing Parameters, I^2S Mode

➢ FM Receiver CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
FM Receiver					
Specifications Referred					
Input Frequency		64	—	108	MHz
FM Frequency Steps		10	—	200	kHz
Sensitivity[3,4,5,6,7]	(S+N)/N = 26 dB	—	2	—	µV EMF
RDS Sensitivity[8]	Δf = 2 kHz, RDS BLER < 5%	—	8	—	µV EMF
RDS Synchronization Persistence[8]	Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	3.8/60	—	µV EMF/ RDS BLER%
RDS Synchronization Stability[8]	Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	5.9/10	—	µV EMF/ RDS BLER%
RDS Synchronization Time[8]	Δf = 2 kHz RF input = 60 dBµV EMF	—	90	—	ms
RDS PI Lock Time[8]	Δf = 2 kHz RF input = 60 dBµV EMF	—	105	—	ms
LNA Input Resistance[6,8,9]		3	4	—	kΩ
LNA Input Capacitance[6,8,9]		4	5	6	pF
Input IP3[3,4,7]	400 and 800 kHz blockers	—	105	—	dBµV EMF
AM Suppression[3,4,6,8,9]	m = 0.3	—	55	—	dB
Image Rejection[8]	Δf = 22.5 kHz	—	55	—	dB
Adjacent Channel Selectivity	±200 kHz	—	44	—	dB
Alternate Channel Selectivity	±400 kHz	—	66	—	dB
Spurious Response Rejection[3,4,8,9]	In-band	35	—	—	dB
Strong Signal Distortion[3,4,5,6,8]	RF Level 120 dBµV EMF	—	58	—	dB SINAD
Audio Output Voltage[3,4,8,9]		—	80	—	mVRMS

Notes:

1. Additional testing information is available in application note, Procedure." Volume = maximum for all tests. Tested at Rf = 98 MHz.
2. To ensure proper operation and receiver performance,
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz.
6. f_{RF} = 76 to 108 MHz.
7. AGC is disabled.
8. Guaranteed by characterization.
9. Measured at V_{EMF} = 60 dBµV_{EMF}.
10. Δf = 75 kHz.
11. At LOUT and ROUT pins.

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
Audio Output L/R Imbalance[3,6,9,10]		—	—	1	dB
Audio Frequency Response Low[9]	–3 dB	—	—	30	Hz
Audio Frequency Response High[8]	–3 dB	15	—	—	kHz
Audio Stereo Separation[3,6,9,10]		—	45	—	dB
Audio SNR[3,4,5,6,9]		—	63	—	dB
Audio THD[3,4,5,6,9]		—	0.1	0.5	%
De-emphasis Time Constant	FM_DEEMPHASIS = 2	70	75	80	µs
	FM_DEEMPHASIS = 1	45	50	54	µs
Audio Common Mode Voltage[11]		0.7	0.8	0.9	V
Audio Common Mode Voltage[8]	High-Z mode	—	0.5 x V_{IO}	—	V
Audio Output Load Resistance[8,10,11]	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[6,10,11]	Single-ended	—	—	50	pF
Seek/Tune Time[11]	RCLK tolerance = 100 ppm	—	40	60	ms/ channel
Powerup Time	From powerdown	—	—	110	ms
FM RSSI Offset	Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:
1. Additional testing information is available in application note, Procedure.* Volume = maximum for all tests. Tested at Rf = 98 MHz.
2. To ensure proper operation and receiver performance,
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz.
6. f_{RF} = 76 to 108 MHz.
7. AGC is disabled.
8. Guaranteed by characterization.
9. Measured at V_{EMF} = 60 dBµV_{EMF}.
10. Δf = 75 kHz.
11. At LOUT and ROUT pins.

➢ WB Receiver CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_R		162.4	—	162.55	MHz
Sensitivity[2,3]		SINAD = 12 dB	—	0.45	—	µV EMF
Adjacent Channel Selectivity		±25 kHz	—	55	—	dB
Audio S/N[2,3,4]		Mono	—	45	—	dB
Audio Frequency Response Low[5]		–3 dB	—	—	300	Hz
Audio Frequency Response High[5]		–3 dB	3	—	—	kHz

Notes:
1. To ensure proper operation and receiver performance,
2. F_{MOD} = 1 kHz.
3. Δf = 3 kHz.
4. Measured at V_{EMF} = 60 dBµV EMF.
5. Guaranteed by characterization.

➢ AM Receiver CharacteristiFSV

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
AM Receiver					
Specifications referred voltages at antenna dummy input.					
Input Frequency	AM/MW	520	—	1710	kHz
	AM/LW	144	—	288	kHz
	AM/SW[2]	2.3	—	30	MHz
Frequency Steps		1	—	10	kHz
Sensitivity [3,4,5,6]	(S+N)/N=26 dB	—	28	—	µV EMF
IP3[9]	40 and 80 kHz Offset	—	99	—	dBuV EMF
Audio SNR [3,4,7,8]		—	53	—	dB
Audio THD [3,4,7,8]		—	0.1	—	%
Strong Signal THD [2,7,8,9]	RF input level 120 dBµV EMF	—	0.2	—	%
Strong Signal SINAD [2,7,8,9]	RF input level 120 dBµV EMF	—	53	—	dB
Power Supply Rejection Ratio[9]	ΔV_{DD} = 100 mVRMS, 100 Hz	—	40	—	dB
Audio Output Voltage [3,4]		54	60	67	mVRMS
Seek Time/Channel[9]	RCLK tolerance = 100 ppm	—	TBD	—	ms
Tune Time[9]	RCLK tolerance = 100 ppm	—	TBD	—	ms
Powerup Time[9]	From powerdown	—	—	110	ms

Notes:
1. To ensure proper operation and receiver performance,
2. operation and performance.
3. FMOD = 1 kHz, 30% modulation, 2 kHz channel filter.
4. Measured at V EMF = 75 dBµV EMF.
5. fRF = 520 to 1710 kHz.
6. System-level sensitivity performance including recommended applications circuit.
7. BAF = 300 Hz to 15 kHz.
8. fRF = 1000 kHz
9. Guaranteed by characterization.

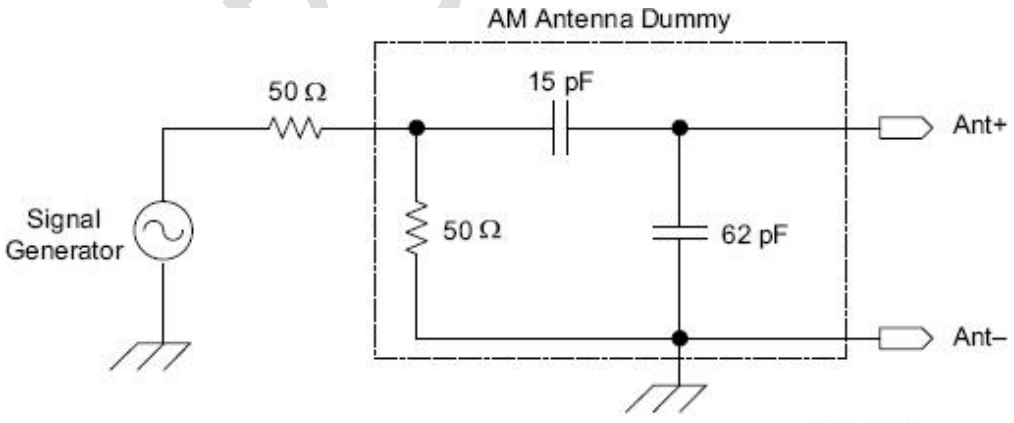


Figure 9. AM Test Circuit

➢ Reference Clock and crystal CharacteristiFSV

(V_{DD} = 2.7 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RCLK Supported Frequencies			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance			–100	—	100	ppm

✧ Functional Description

The FSV474X AM/FM receiver family offers 100% CMOS receiver integrated circuits (IC), providing the full receive functionality from antenna to audio for use in the automotive market. The family includes a portfolio of highly integrated receivers for primary AM/FM receivers that support worldwide broadcast audio bands and corresponding attributes including AM/FM and "college bands" down to 64 MHz, long wave, NOAA weather band, and dedicated companion RDS background receivers.

The FSV474X products are feature -rich solutions, providing both highly automated performance, and extensive flexibility for customized audio and system performance. Programmable algorithms include advanced seek with multiple signal qualifiers and thresholds in all supported bands, FM stereo blend rates and thresholds, soft mute characteristiFSV, multi-path detection and mitigation, AM/FM noise blankers, and selectable FM Hi-cut filters. The part accepts programmable reference clock values. The IC provides audio output in standard line-level analog audio using high fidelity stereo DAFSV or digital audio format.

➢ FSV4740/41/43/45 Product Family

Feature	FSV4740	FSV4741	FSV4743	FSV4745
FM band coverage	✓	✓	✓	✓
FM RDS reception		✓	✓	✓
AM band coverage	✓	✓	✓	✓
LW band coverage			✓	✓
SW band coverage			✓	✓
WB (w/o SAME) band coverage			✓	
FM multi-path detection and stereo/mono blend mitigation	✓	✓	✓	✓
Advanced stereo-mono blend	✓	✓	✓	✓
Advanced soft mute	✓		✓	✓
Hi-cut			✓	✓
FM noise blanker			✓	✓
AM noise blanker			✓	✓
Digital audio I^2S		✓	✓	✓

➢ Operating Modes

The device operates in either an FM receive or an AM receive mode. In FM mode, radio signals are received on FM-IN (pin 2) and processed by the FM frontend circuitry. In AM mode, radio signals are received on AM-IN (pin 4) and processed by the AM front-end circuitry. In addition to the receiver mode, there is a clocking mode to choose to clock the device from a reference clock or crystal. The receiver mode and the clocking mode are set by the POWER_UP command.

➢ FM Receiver Front-end

The FSV474x family integrates the entire FM receive chain from antenna to audio out. The FM band is received on the FMI pin via an input coupling network with the recommended application circuit. This input coupling network isolates the FM band for best performance. The LNA supports US, Europe, Japan, OIRT, and Rest of World FM broadcast bands (64 to 109MHz) . The AGC circuit automatically controls the LNA gain to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled.

➢ AM Receiver Front-end

The FSV474x family provides an integrated LNA, which works in conjunction with an external cascode amplifier to provide an AM receive chain from antenna to audio out. There are very few external components and no manual alignment required. The AM signal is

received on the AMI pin via a cascode amplifier external circuit. The cascode circuit degeneration is automatically adjusted via the AGC pin .The amount of degeneration depends on the network, the tuned frequency, and present blockers. An additional GPO1 signal is used to attenuate the signal via a shunt for very strong signal handling when the signal exceeds the AGC pin degenerative control of the cascode amplifier stage.

➢ Received Signal Qualifiers

A tuned signal's quality can vary with the environmental conditions, time of day, and position of the antenna among many other factors. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the FSV474x monitors and provides indicators of the signal quality, allowing the host processor to perform additional processing if required by the customer. The FSV474x monitors and reports a set of standard industry signal quality metriFSV including RSSI, SNR, and multi-path interference on FM signals.

As with other FSV474x features, how these variables are used to improve audio performance can be left to the Silicon Labs on -chip algorithms (recommended), or they can be brought out for host-processor instructions.

➢ Digital Audio Interface

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of one DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

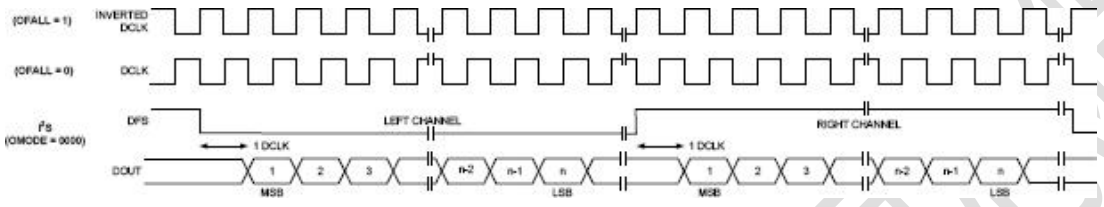
In all audio formats, depending on the word size, DCLK frequency and sample rates, there

may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

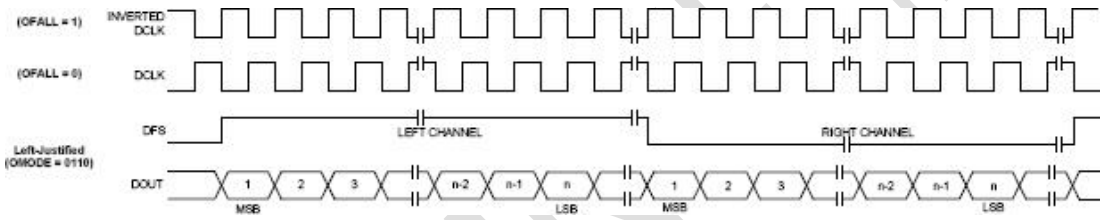
The number of audio bits can be configured for 8, 16, 20, or 24 bits.

Audio Sample Rates

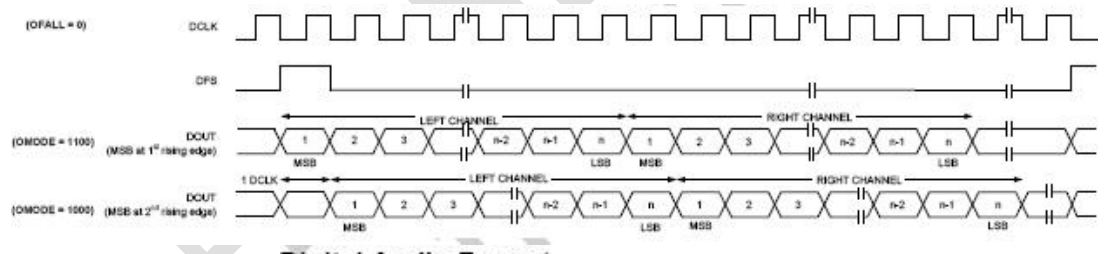
The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz.



I²S Digital Audio Format



Left-Justified Digital Audio Format



Digital Audio Format

➢ Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown below.

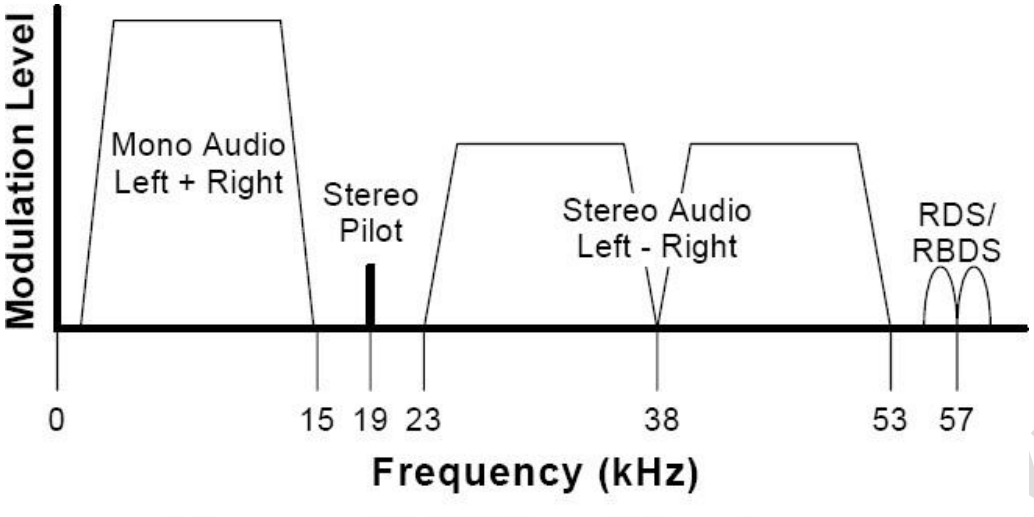


Figure MPX Signal Spectrum

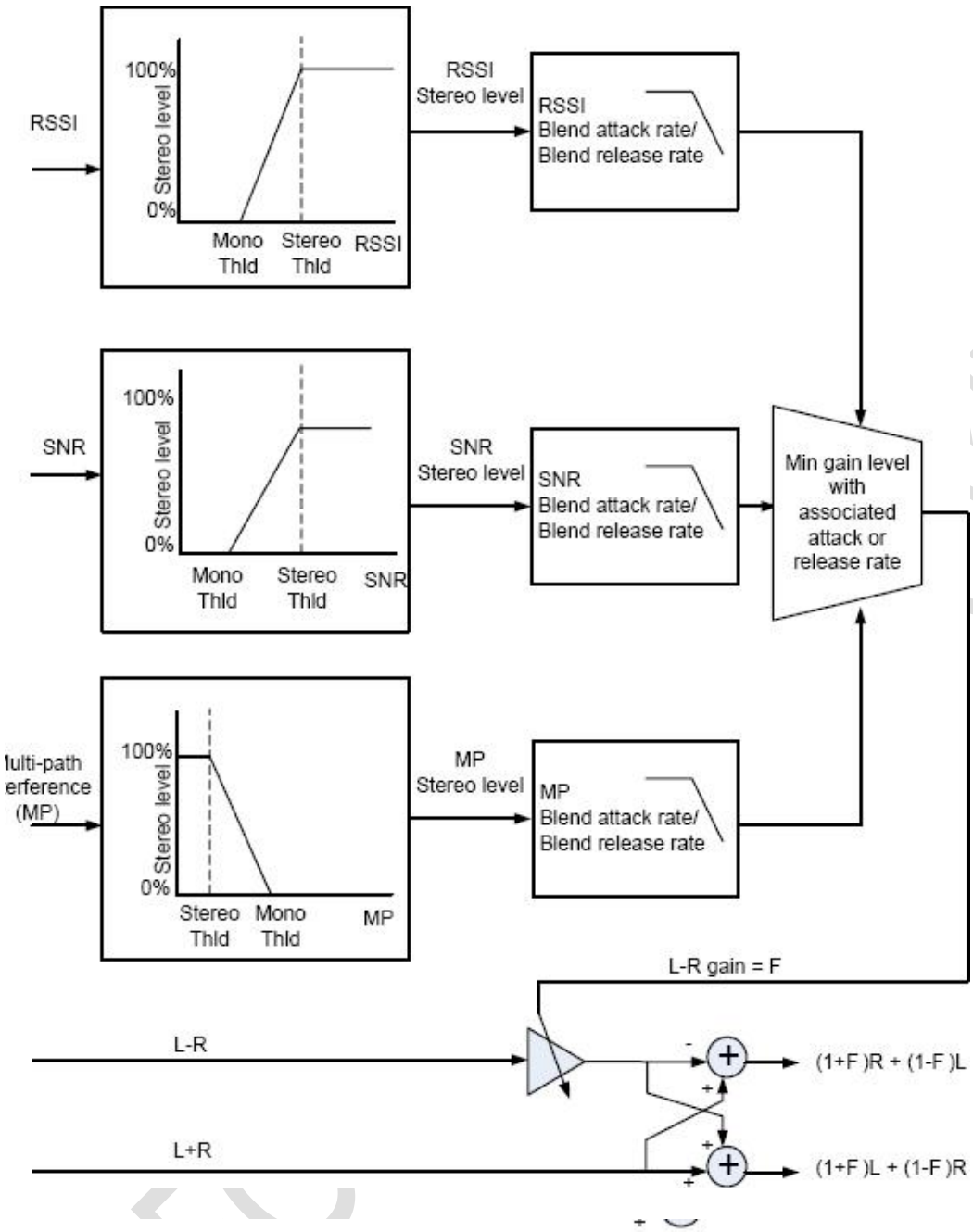
Stereo Decoder

The device's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

The device uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.



Stereo-Mono Blend Based on Active Monitoring of RSSI, SNR, and Multi-Path Interference

➢ De-emphasis

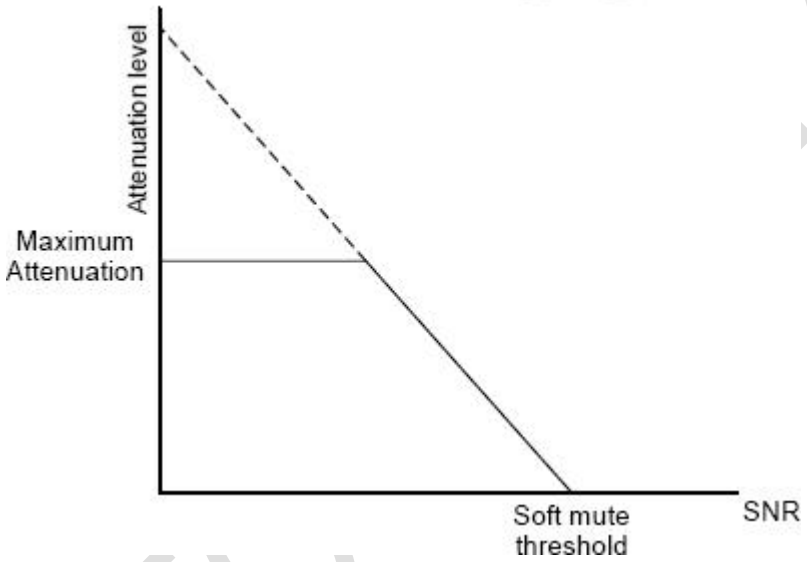
Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The device incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The deemphasis time constant is programmable to 50 or 75 μs and is set by the FM_DEEMPHASIS property.

➢ Stereo DAC

High- fidelity stereo digital-to-analog converters (DAFSV) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property. It is necessary that the volume be maintained at maximum levels to ensure the highest dynamic range audio outputs to the external audio processing stage in a car radio.

➢ Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. This process is shown conceptually in Figure 16. The FSV474x triggers soft mute feature by monitoring the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and decay rates. The FSV474x provides the soft mute feature in FM and AM bands.



Soft Mute Based on Active Monitoring of SNR

➢ Seek and valid Station Qualification

The seek function will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations, or if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt.

The FSV474x seek functionality is performed completely on-chip or can be brought out to a

companion processor. The FSV474x can provide base values for signal quality variables to a companion processor for qualification or can further process the base values to qualify valid or invalid stations.

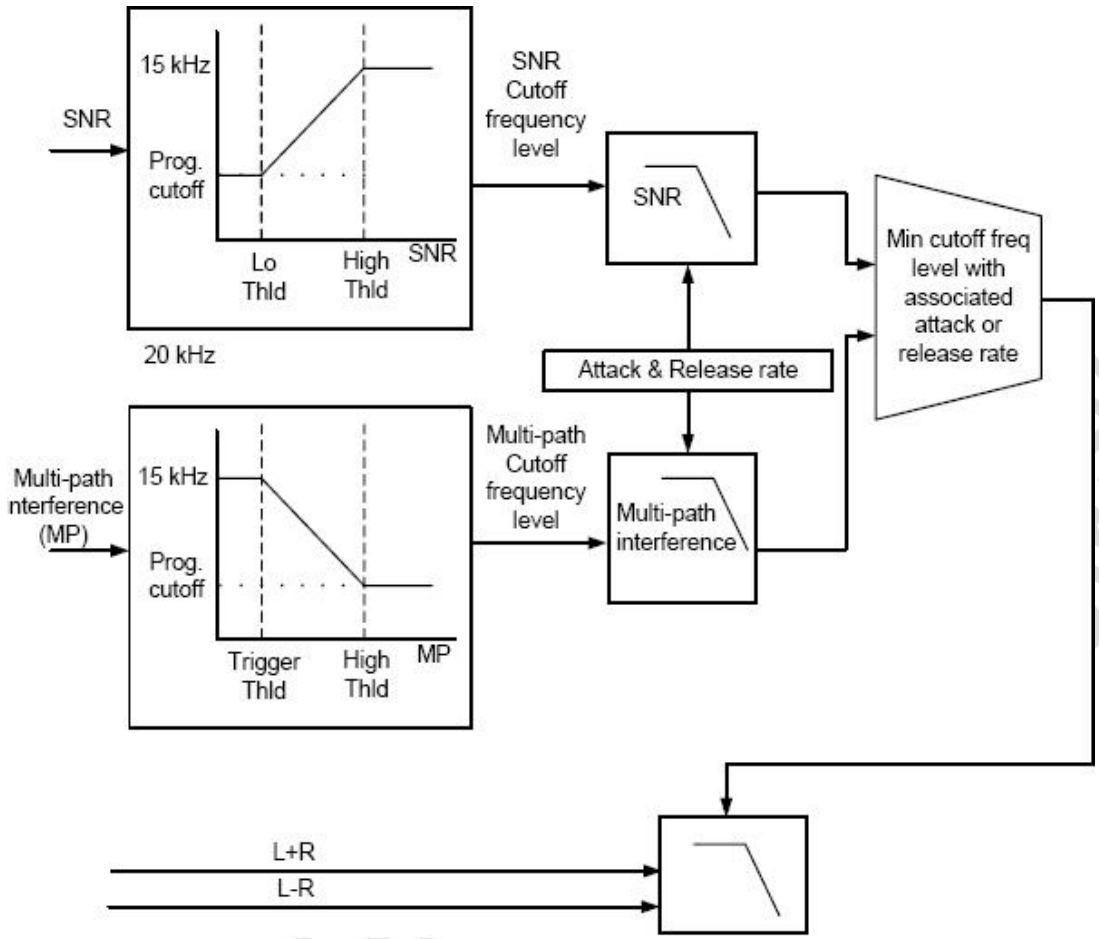
The FSV474x uses RSSI, SNR, and AFC to qualify stations. Most of these variables have programmable thresholds to tailor the seek function to the subjective tastes of customers.

RSSI is employed first to screen all possible candidate stations. SNR and AFC are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations; however, the more challenging levels the thresholds are set to, the longer the overall seek time as more stations and more qualifiers will be assessed. It is recommended that RSSI be set to a mid-level threshold in conjunction with an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations whilst keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire AM or FM band with all thresholds engaged is very short depending on the band content.

Seek is initiated using the FM_SEEK_ START or AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties.

➢ FM Hi-Cut Control

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multi-path interference. Two metriFSV, SNR and multi-path interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metriFSV. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. A single set of attack and release rates for hi -cut are programmable for both metriFSV from a range of 2 ms to 64 s. Figure 17, “FM Hi- Cut Based on Active Monitoring of SNR and Multi-Path Interference,” illustrates hi-cut. The level of hi-cut applied can be monitored with the FM_RSQ _STATUS command. Hi-cut can be disabled by setting the hi-cut filter setting to the default audio bandwidth of 15 kHz.



FM Hi-Cut Based on Active Monitoring of SNR and Multi-Path Interference

➢ AM/FM Noise Blanker

In an automotive environment, noise spikes from engine ignition and/or various other electrical sources can significantly impair and disrupt the audio output. The FSV4743/45 includes a noise blanker to mitigate or eliminate these noise spikes and audible artifacts. Figure shows a conceptual flow chart for the FSV4743/45 noise blanking function. The FSV4743/45 offers five properties for configuring the AM and FM noise blankers including detection threshold, blanking interval, trigger rate, noise-floor bandwidth, and delay. Each property is configurable for adopting customers to refine and apply unique noise-blank behavior.

FM Noise Blanker Property Settings

The FM noise blanker detection threshold property sets the level threshold for detection of the noise impulses/spikes in dB from a range of 1 dB to 90 dB above the noise floor. The FM noise blank rate property sets the maximum rate in Hz at which the noise blanker is triggered from a range of 100 Hz to 6400 Hz. The FM noise blank interval property sets the noise

blanking interval in microseconds at which the original samples are replaced by interpolated "clean" samples from a range of 8 µs to 48 µs. The FM noise blanker IIR filter property sets the noise floor bandwidth from a range of 390 Hz to 2480 Hz. This property sets the rms noise floor above which the noise impulse level detect threshold is set for noise impulse detection. The FM noise blank delay property sets the delay in microseconds in applying impulse blanking to the original samples, which allows for insertion and alignment of the blanked samples with the original sampled signal. The range of values for FM noise blanker delay is 125 µs to 219 µs.

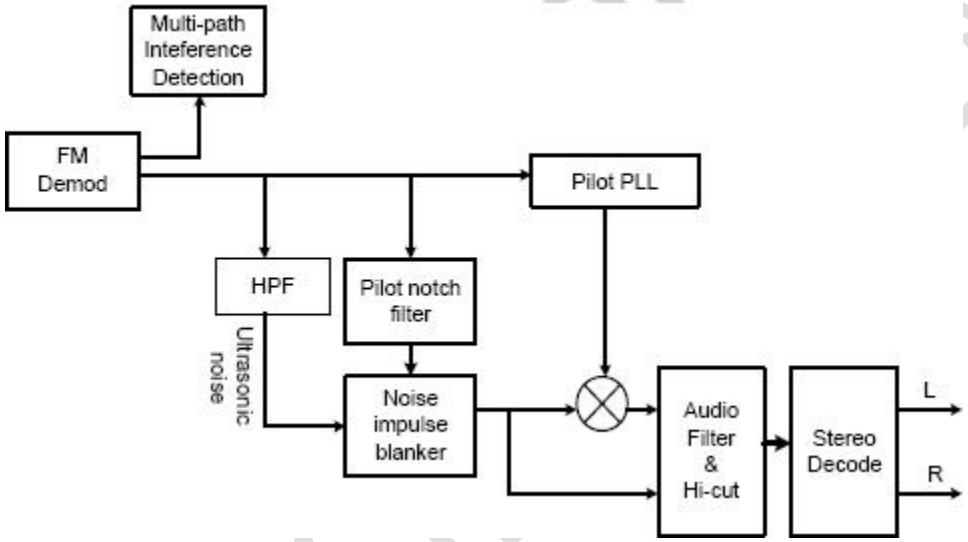


Illustration of Noise Blanker in FM Signal Path

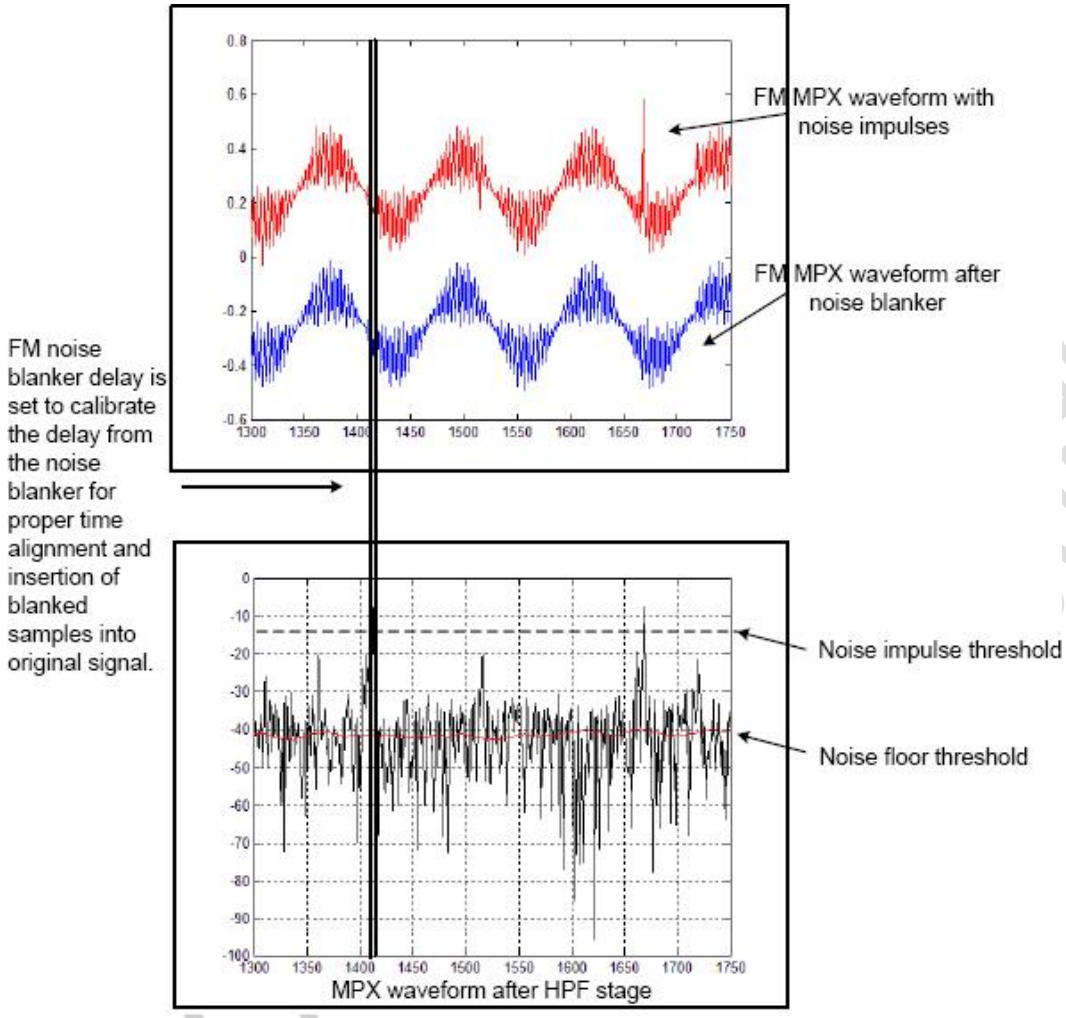
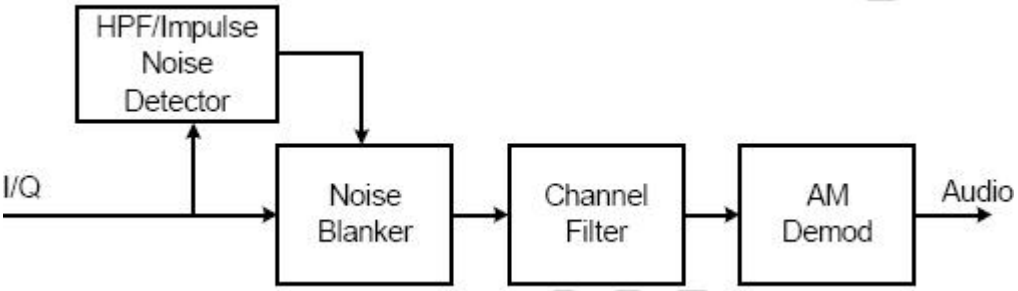


Illustration of FM Noise Blanker Property Settings for Proper Detection of Noise Impulses (FM MPX waveforms are offset vertically for illustration purposes)

➢ AM Noise Blanker Property Settings

The AM noise blanker detection threshold property sets the level threshold for detection of the noise impulses/spikes in dB from a range of 1 dB to 90 dB above the noise floor. The AM noise blank rate property sets the maximum rate in Hz at which the noise blanker is triggered from a range of 100 Hz to 6400 Hz. The AM noise blank interval property sets the blanking interval in microseconds at which the original samples are replaced by previous samples using a "sample and hold" scheme from a range of 15 µs to 110 µs. The AM noise blanker IIR filter property sets the noise floor bandwidth from a range of 300 Hz to 2480 Hz. This property sets the rms noise floor above which the noise impulse level detect threshold is set for noise impulse detection. The AM noise blank delay property sets the delay in microseconds in applying impulse blanking to the original samples, which allows for insertion and alignment of the blanked samples with the original sampled signal. The range of values for the AM noise blanker delay is 125 µs to 219 µs.



. Illustration of Noise Blanker in AM Signal Path.

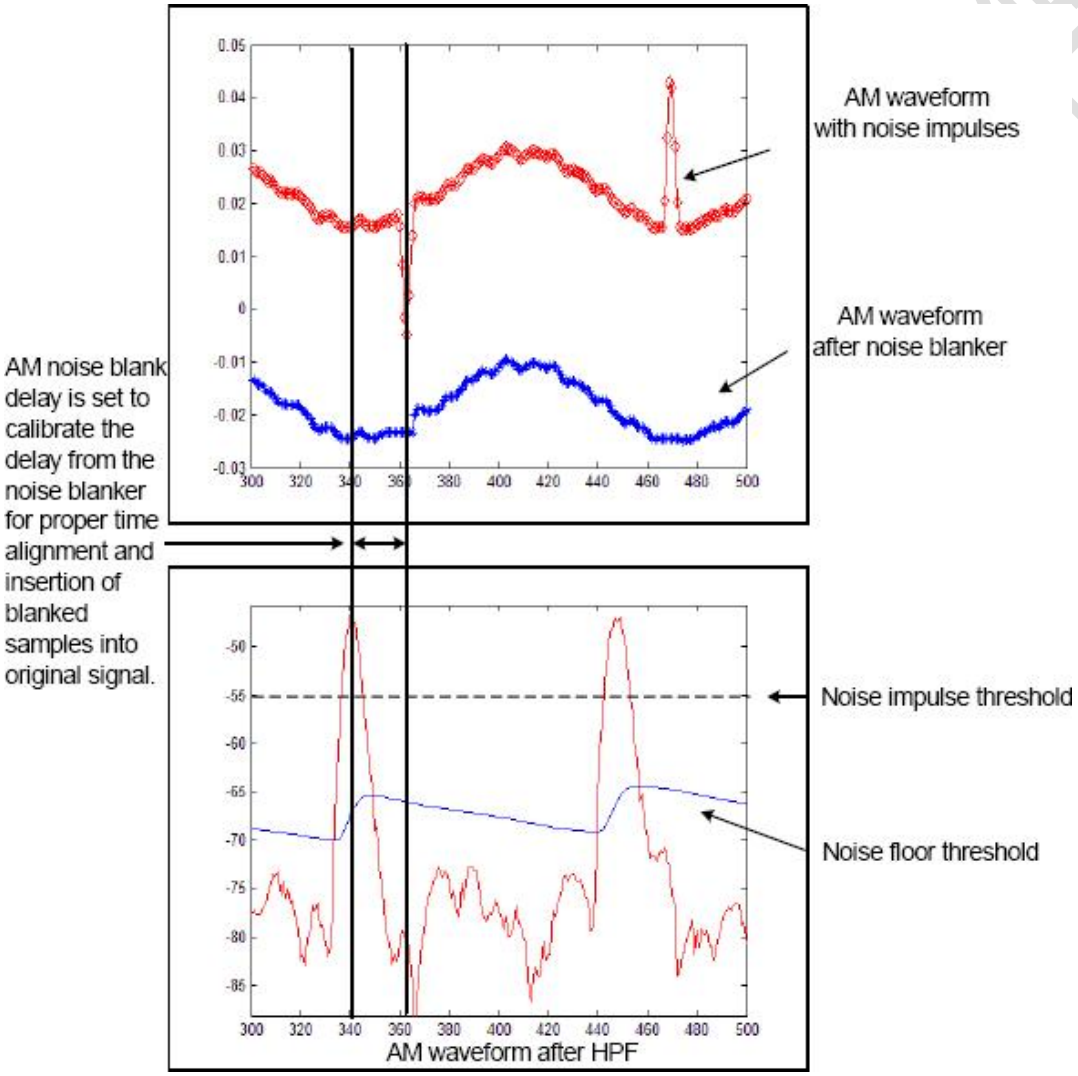


Illustration of AM Noise Blanker Property Settings for Proper Detection of Noise Impulses (AM Waveforms are Offset Vertically for Illustration Purposes)

➢ Programming Section

To ease development time and offer maximum customization, the device provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control an action such as power up the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after power-up. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a one-byte status update indicating interrupt and clear-to-send status information.

➢ Reset, Power-up, and Power-down

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A power-down mode is available to reduce power consumption when the part is idle. Putting the device in power-down mode will disable analog and digital circuitry while keeping the bus active.

➢ GPO Output

The GPO 1–3 pins can be set to output a constant low or high output, or optionally be set to provide a hardware interrupt to the controller such as scan complete, stereo/mono indicator, and RDS/RBDS. After reset and POWER_UP into AM receiver mode, GPO1 is reserved for AM AGC external attenuator control.

➢ RDS/RBDS Advanced Processor

The device implements an RDS/RBDS processor for symbol decoding, block synchronization, error detection, and error correction.

The device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The device reports RDS decoder synchronization status, and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicate that the corresponding block information word contains six or more non-correctable errors, or that the block checkword contains errors.

➢ Tuning

The frequency synthesizer includes a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency can be directly programmed using the FM_TUNE_FREQ and AM_TUNE_FREQ commands. The device supports channel spacing of 50, 100, or 200 kHz in FM mode and 9or 10 kHz in AM mode.

➢ Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START and AM_SEEK_START commands.

Two seek options are available. The device will either wrap or stop at the band limits. If the seek operation is unable to find a channel, the device will indicate failure and return to the channel selected before the seek operation began.

➢ Reference Clock

The device reference clock is programmable.An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided.

The device performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the device is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Unique recommends that all SDIO data traffic be suspended during device seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The STC (seek/tune complete) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

➢ Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the device, and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The device selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor which is connected while RST is low, and the GPO2 pin includes an internal pulldown resistor which is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table below:

Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2
2-wire	1	0
SPI	1	1(must drive)
3-wire	0(must drive)	0

After the rising edge of RST, the pins GPO1 and GPO2 are used as general purpose output (O) pins. In any bus mode, commands may only be sent after VIO and VDD supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven bit device address, followed by a read/write bit (read = 1, write = 0). The device acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the device will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the seven-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an eight bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The device acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the device has acknowledged the control byte, it will drive an eight bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the device.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

3-wire bus mode uses the SCLK, SDIO and SEN_ pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a three-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a five-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the device will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

0x48 = write a command (controller drives 8 additional bytes on SDIO).

0x80 = read a response (device drives one additional byte on SDIO).

0xC0 = read a response (device drives 16 additional bytes on SDIO).

0xA0 = read a response (device drives one additional byte on GPO1).

0xE0 = read a response device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly 8 data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

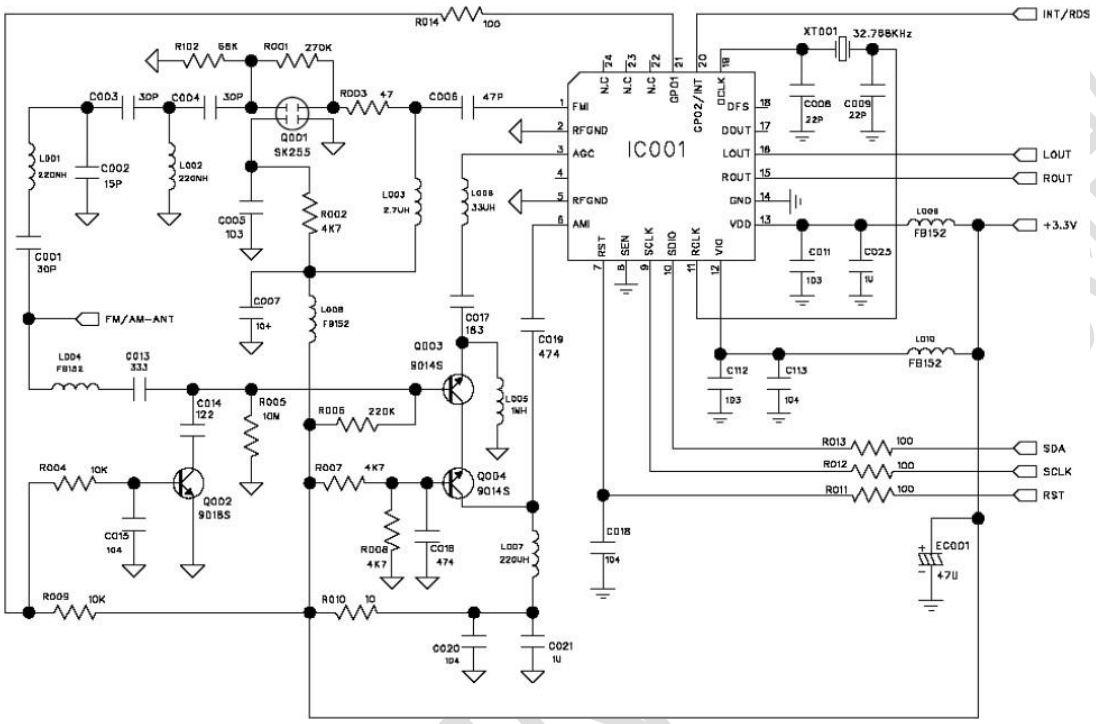
For read operations, the controller must read exactly one byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep SEN low until all bytes have transferred. A transaction may be aborted at any time by setting SEN high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

✧ Commands and Properties

Refer to “FSV47332：FSV47XX Programming Guide”

✧ Application Digram



Mechanical Data

The device is currently available in a 24-pin-QPN pachage.

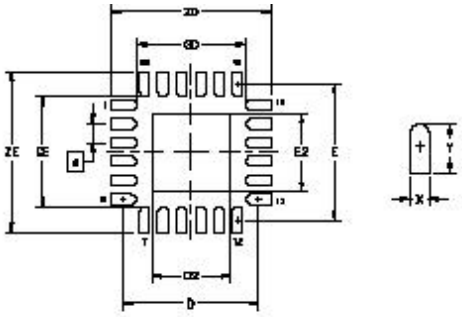


Figure 26. PCB Land Pattern

Table 20. Dimensions for PCB Land Pattern

Dimension	Min	Max
e	0.50 BSC.	
E	3.62 REF.	
D	3.62 REF.	
E2	2.00	2.20
D2	2.00	2.20

Dimension	Min	Max
GE	2.93	—
GD	2.93	—
X	—	0.28
Y	0.69 REF	
ZE	—	4.31
ZD	—	4.31

Notes: General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 2 x 2 array of 0.90 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Notes: Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.