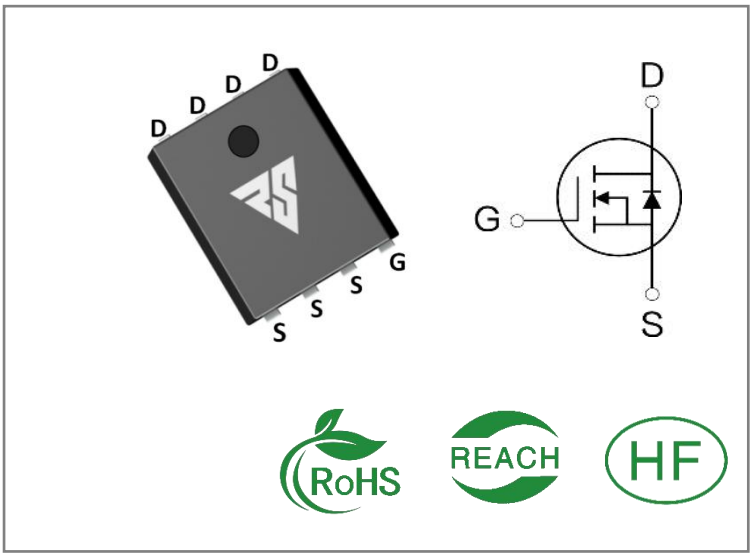
ID	R_{DS}(ON)(Typ)	VDSS
80A	4.6mΩ	30V



Applications:
- Load Switch
- PWM Applications
- Power Managment

Features:
- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS30N80K	PDFN3*3	RS30N80K	Tape&reel	5000 PCS

Absolute Maximun Ratings Tc= 2 5℃ unless otherwise specified

Symbol	Parameter	RS30N80K	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25℃	80	A
ID	Continuous Drain Current TC=100℃	50	
IDM	Pulsed Drain Current (Note*1)	300	
PD	Power Dissipation	29	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH, VDD = 25V, RG = 25 Ω,TC=25℃	169	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	℃
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature
Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

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Thermal Resistance

Symbol	Parameter	RS30N80K	Units	Test Conditions
RθJC	Junction-to-Case	4.3	℃/ W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 ℃
RθJA	Junction-to-Ambient	50		1 cubic foot chamber,free air.

OFF Characteristics TJ= 25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30	--	--	V	VGS=0V, ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=30V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V , VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V , VDS=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	4.6	6	mΩ	VGS=10V,ID=30A
		--	7.5	9.5	mΩ	VGS=4.5V,ID=20A
VGS (TH)	Gate Threshold Voltage	1.0	1.6	2.5	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	7	--	nS	VDS=15V ID=30A RG=3Ω
trise	Rise Time	--	14	--		
td(OFF)	Turn- OFF Delay Time	--	33	--		
tfall	Fall Time	--	11	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	1780	--	pF	VGS=0V VDS=15V f=1.0MHz
Coss	Output Capacitance	--	220	--		
Crss	Reverse Transfer Capacitance	--	178	--		
Qg	Total Gate Charge	--	34	--	nC	VDS=15V ID=30A VGS=10V
Qgs	Gate- to- Source Charge	--	7	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	7.5	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	80	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	300	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time	--	20	--	nS	VGS=0V IS=20A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	1.8	--	nC	

Notes:

* 1. Repetitive rating, pulse width limited by maximum junction temperature.
* 2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 0.5%

Typical Feature Curve

Figure 1: Output Characteristics

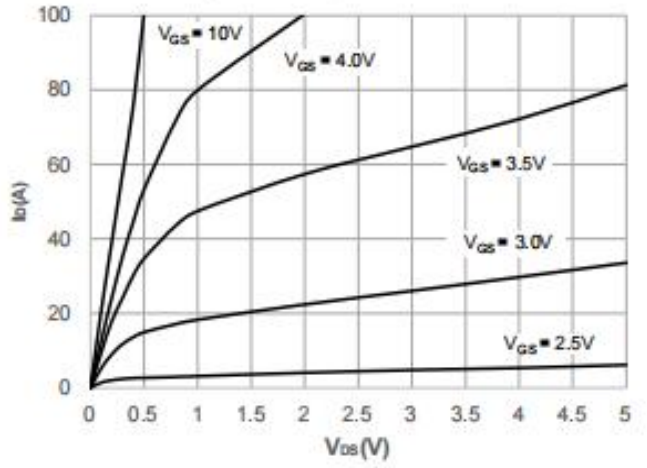

Figure 2: Typical Transfer Characteristics

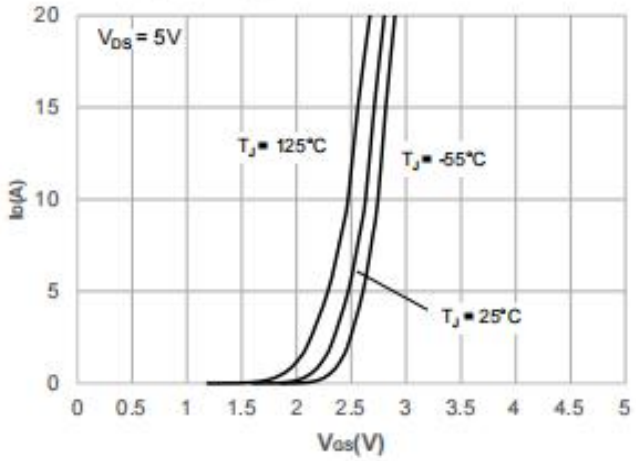

Figure 3: On-resistance vs. Drain Current

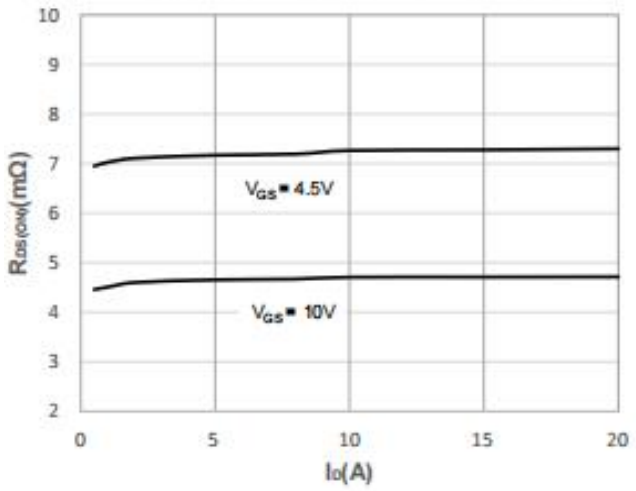

Figure 4: Body Diode Characteristics

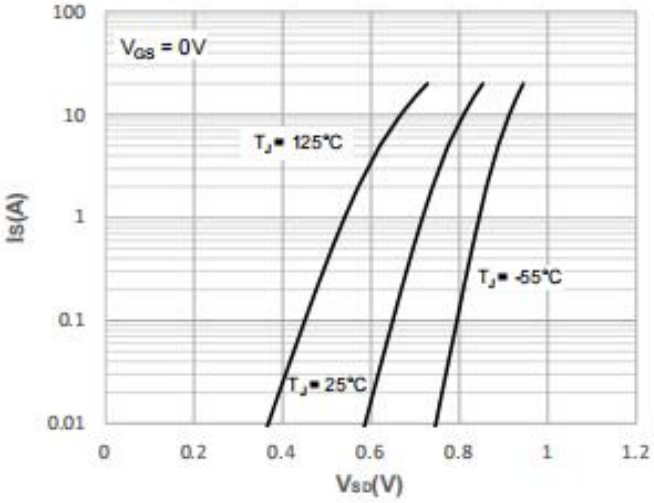

Figure 5: Gate Charge Characteristics

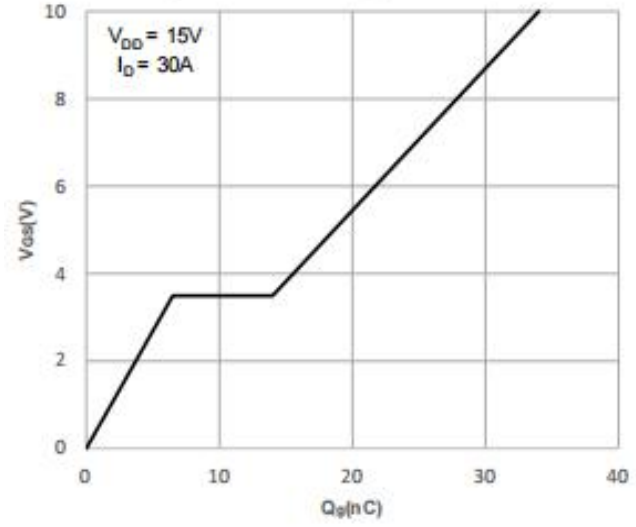

Figure 6: Capacitance Characteristics

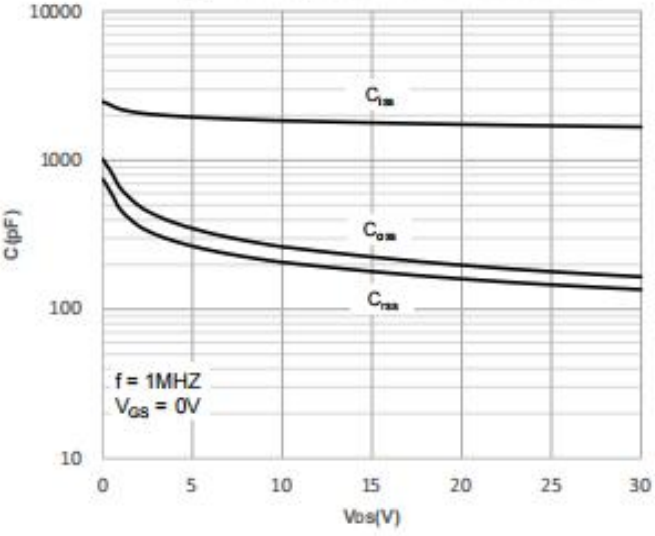

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Figure 7: Normalized Breakdown voltage vs. Junction Temperature

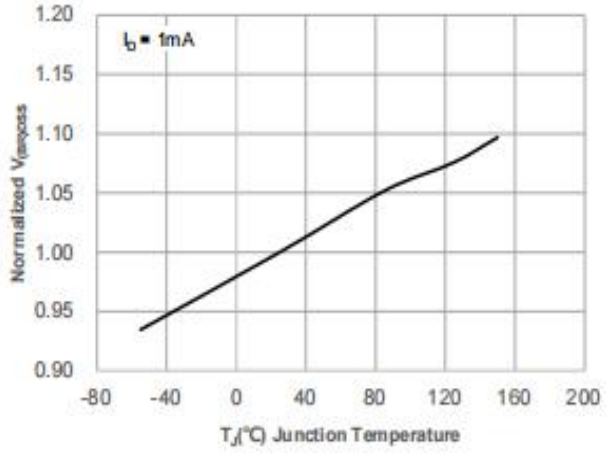


Figure 8: Normalized on Resistance vs. Junction Temperature

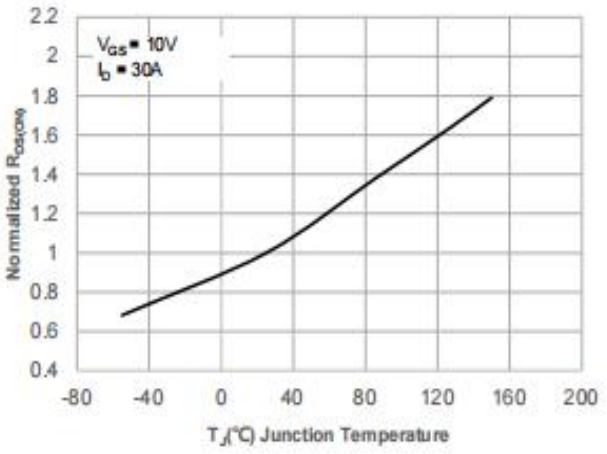


Figure 9: Maximum Safe Operating Area

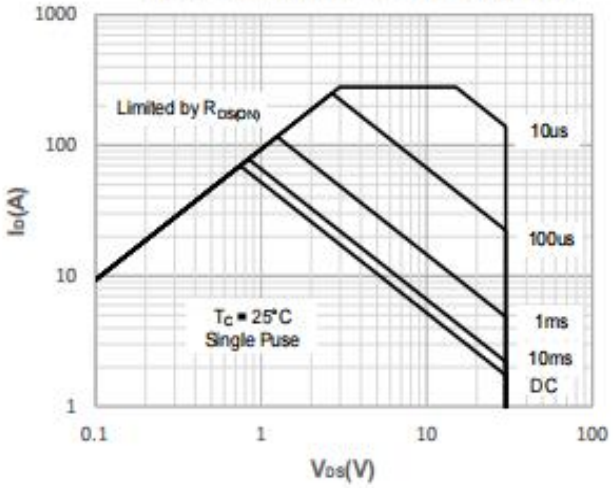


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

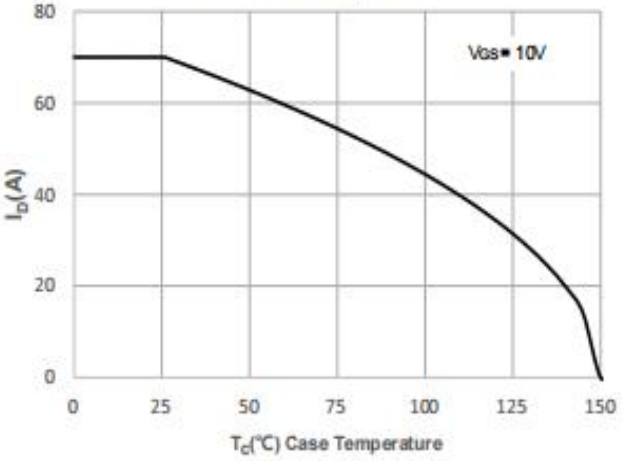


Figure 11: Normalized Maximum Transient Thermal Impedance

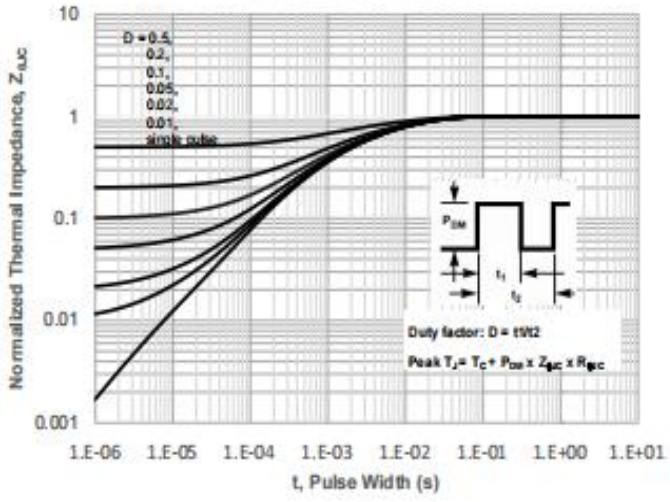
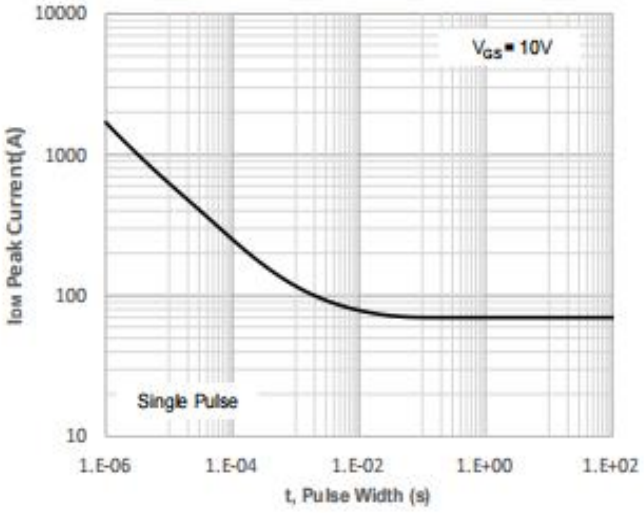


Figure 12: Peak Current Capacity



Test ircuits and Waveforms

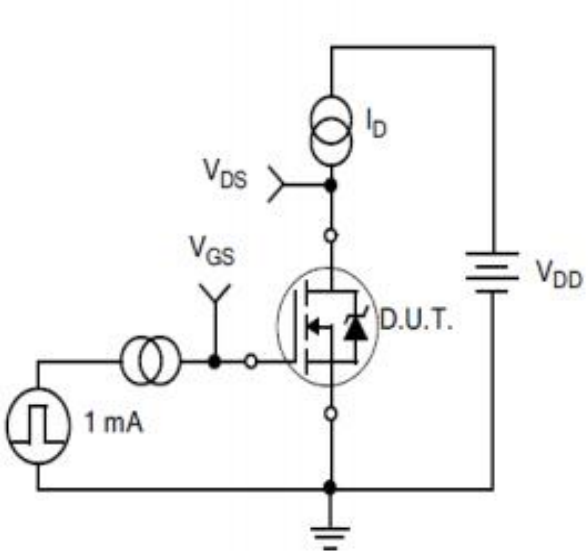


Figure A.
Gate Charge Test Circuit

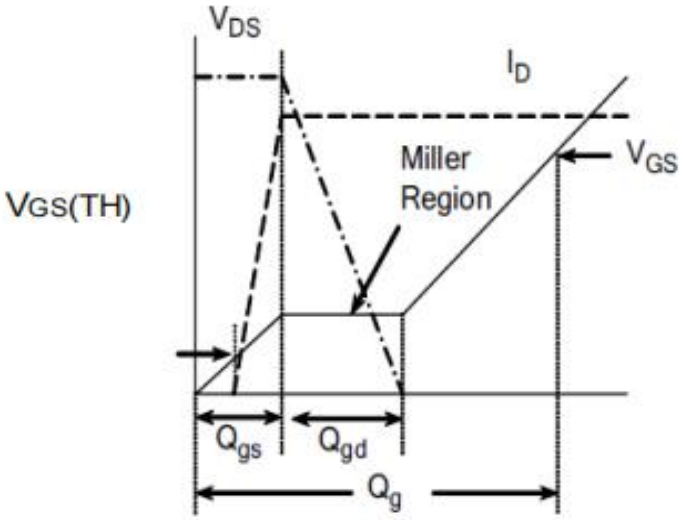


Figure B.
Gate Charge Waveform

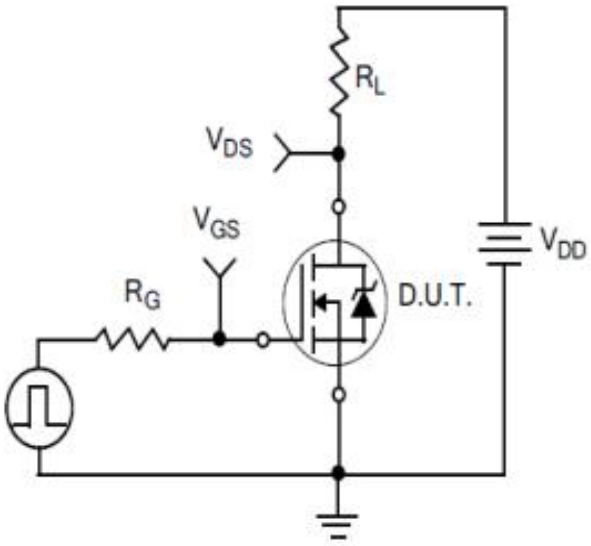


Figure C.
Resistive Switching Test Circuit

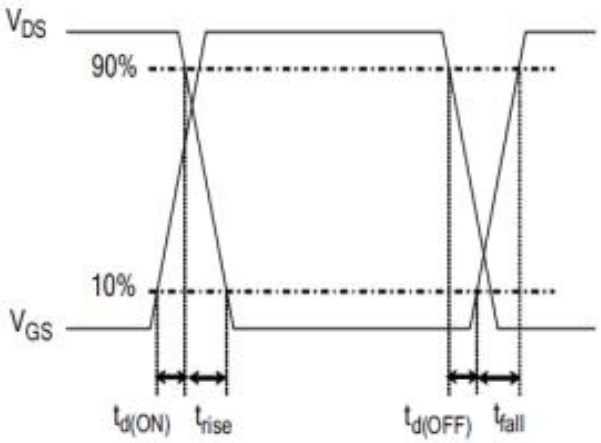


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

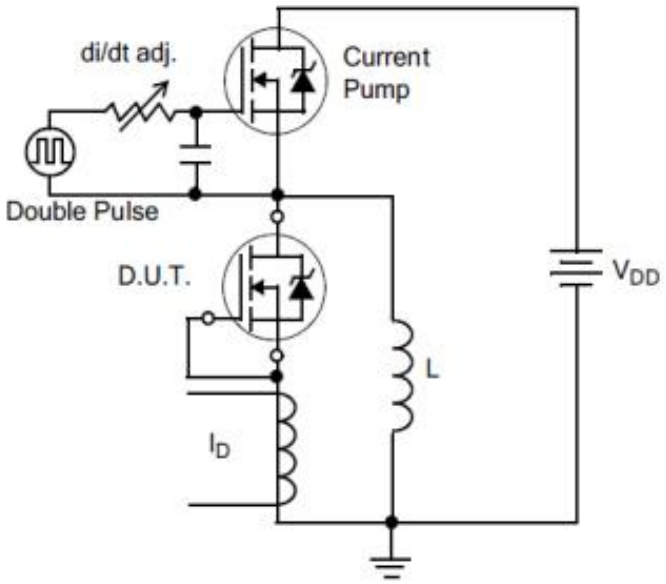


Figure E.Diode Reverse Recovery Test Circuit

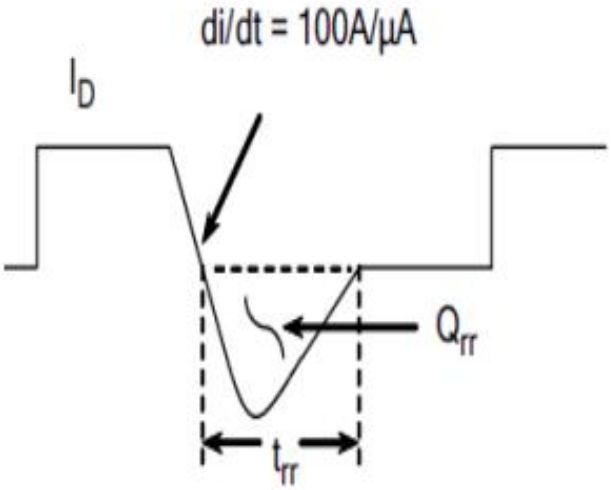


Figure F.Diode Reverse Recovery Waveform

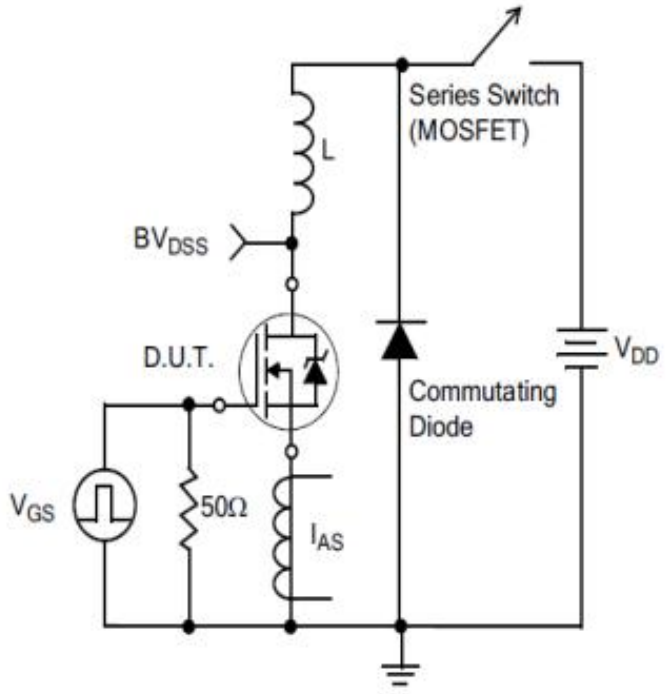
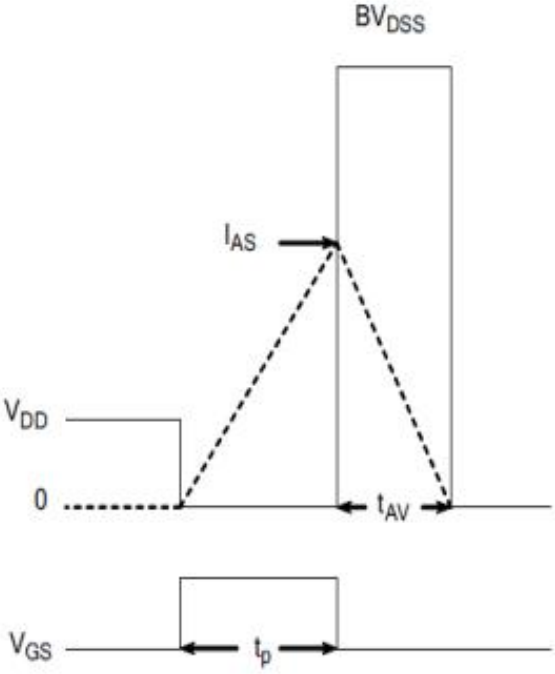


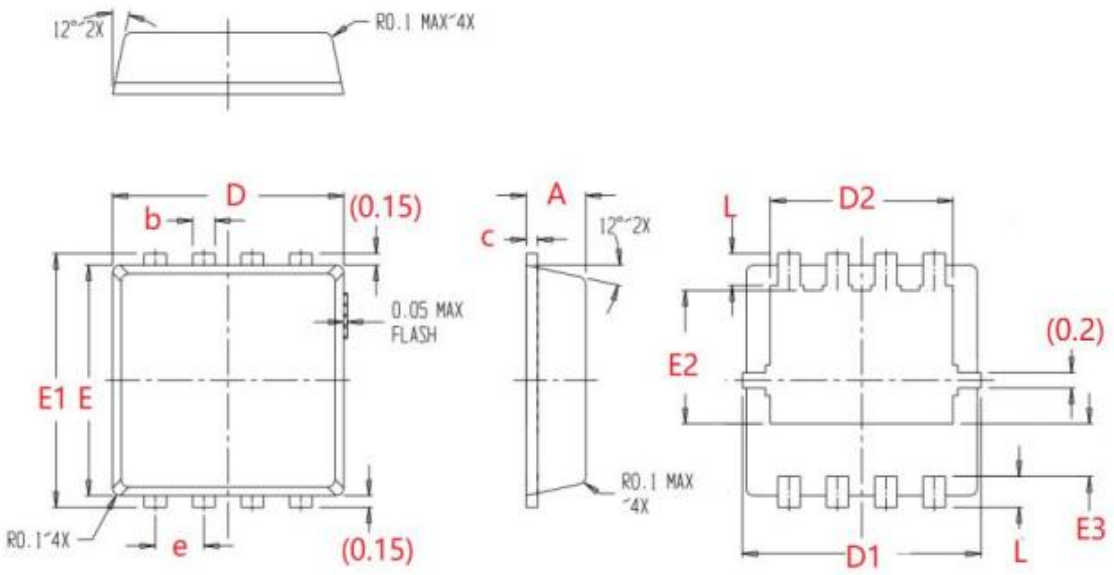
Figure G.Unclamped Inductive Switching Test Circuit



$$E_{AS}= \frac{I_{AS}^2 L}{2}$$

Figure H.Unclamped Inductive Switching Waveforms

Package outline drawing(PDFN3*3 Unit: mm)



（单位：mm）

符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
A	0.7	0.9	E	2.9	3.1	e	0.65TYP	
D	3.0	3.2	E1	3.1	3.5	b	0.25	0.35
D1	3.0	3.4	E2	1.55	1.95	c	0.1	0.2
D2	2.25	2.65	E3	0.5	0.8	L	0.3	0.55

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