1.0-7.2 GHz SPDT Switch

Features

- Broadband frequency range: 1.0 to 7.2 GHz
- Low insertion loss: 0.50dB typical @ 2.4 GHz
- Low insertion loss: 0.65dB typical @ 5.8 GHz
- High isolation: 40 dB @ 5.8 GHz
- High P0.1 dB of 32 dBm
- Integrated DC blocking capacitors
- DFN 1.0 mm x 1.0 mm x 0.45 mm-6L package

Applications

- IEEE 802.11a/b/g/n/ac WLAN Networks
- ISM band radios
- WLAN repeaters
- Low power transmit receive systems
- Smartphones

General Description

The AW13102DNR is a Silicon-On-Insulator(SOI) SPDT switch with low insertion loss, high isolation and high linearity at low supply voltage. It can be used to support mode switching in WLAN applications.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13102DNR has integrated DC blocking capacitors, so no external DC blocking capacitors are required.

The AW13102DNR is provided in a compact DFN 1.0 mm x 1.0 mm x 0.45 mm-6L package.

Typical Application Circuit

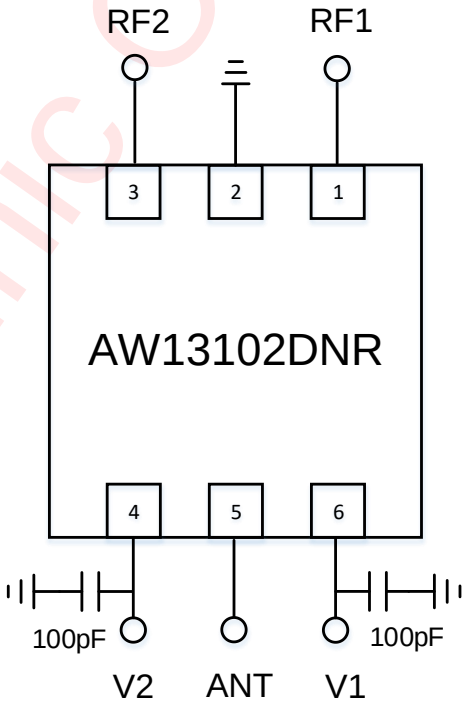
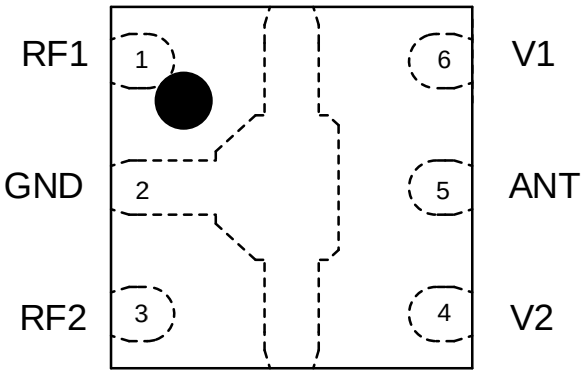


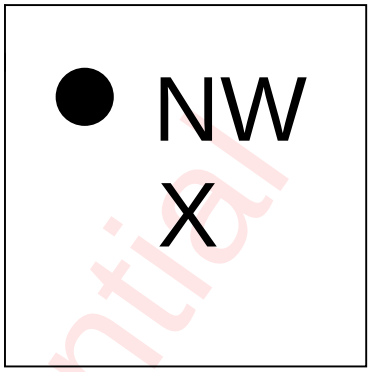
Figure 1 Typical Application Circuit of AW13102DNR

Pin Configuration And Top Mark

AW13102DNR
(Top View)



AW13102DNR Marking
(Top View)



NW – AW13102DNR
X – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	RF1	RF I/O path 1
2	GND	Ground
3	RF2	RF I/O path 2
4	V2	DC control voltage2
5	ANT	Antenna port
6	V1	DC control voltage1

Functional Block Diagram

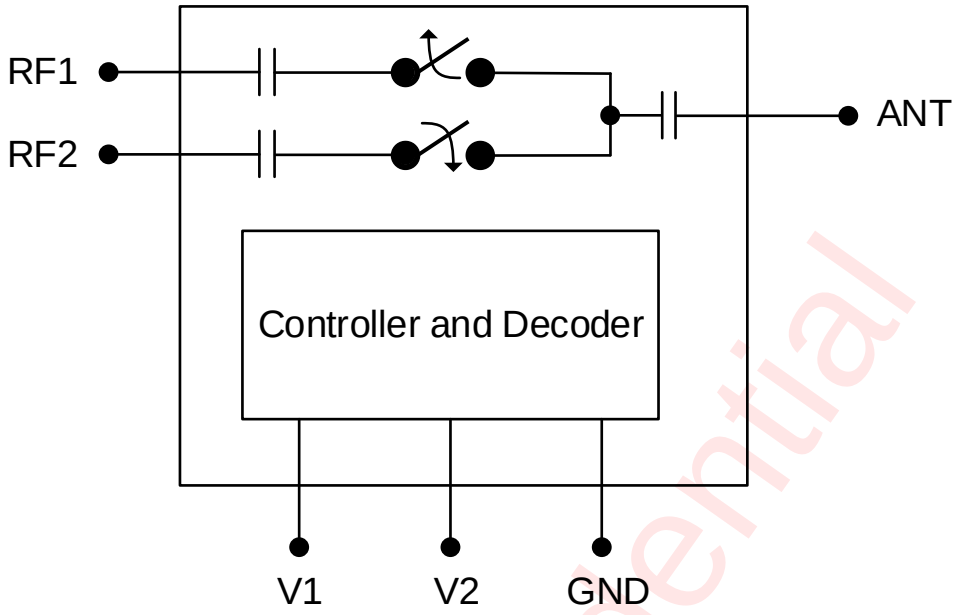


Figure 3 Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13102DNR	-40°C～85°C	DFN 1.0mmX1.0mm -6L	NW	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Control Voltage Range	V1,V2	0 V to 4.0 V
RF input power(RF1/RF2)		33 dBm
Operating Free-air Temperature Range		-40°C to 85°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD (NOTE 2)		
HBM (ESDA/JEDEC JS-001)		±1000V
CDM (ESDA/JEDEC JS-002)		500V

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001.*

Electrical Characteristics

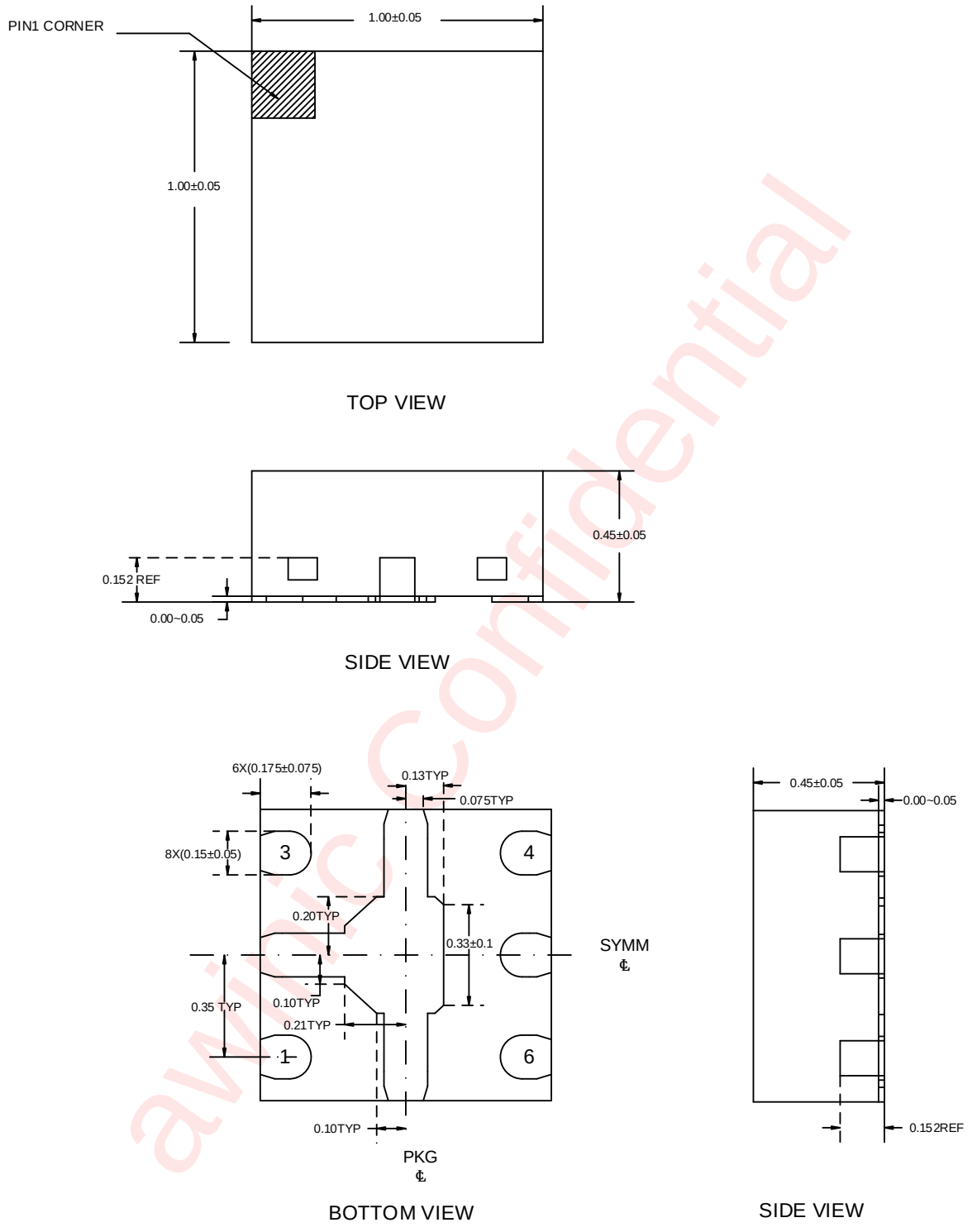
V1=3.3V/0V, V2=0V/3.3V, PIN=0dBm, T_A=+25℃, Z_0=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
VCTL_H VCTL_L	Control Voltage High Low		1.6 0	3.3 0	3.6 0.3	V
ICTL	Control Current	VCTL = 3.3V		4	10	μA
RF Specifications						
IL	Insertion loss(ANT pin to RF1/RF2)	1.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz		0.50 0.65 1.05	0.75 0.95 1.45	dB dB
ISO	Isolation (ANT pin to RF1/RF2)	1.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz	25 32 25	30 40 30		dB dB
RL	Input return loss (ANT pin to RF1/RF2)	1.0-3.0GHz 3.0-6.0GHz 6.0-7.2GHz	14 14 13	17 17 16		dB dB
$P_{0.1dB}$	0.1dB Compression Point (ANT pin to RF1/RF2)	1.0GHz–6GHz		32		dBm
2f0	Second Harmonics	f_0=2.4GHz, PIN=+24dBm,CW		-68		dBm
3f0	Third Harmonics	f_0=2.4GHz, PIN=+24dBm,CW		-58		dBm
tON	Turn-on Switching Time	50% of final control voltage to 90% of final RF power, switching between RF1/2		250	300	nS

CONTROL LOGIC

State	Active Path	V1	V2
0	**ANT to RF1**	**0**	**1**
1	**ANT to RF2**	**1**	**0**

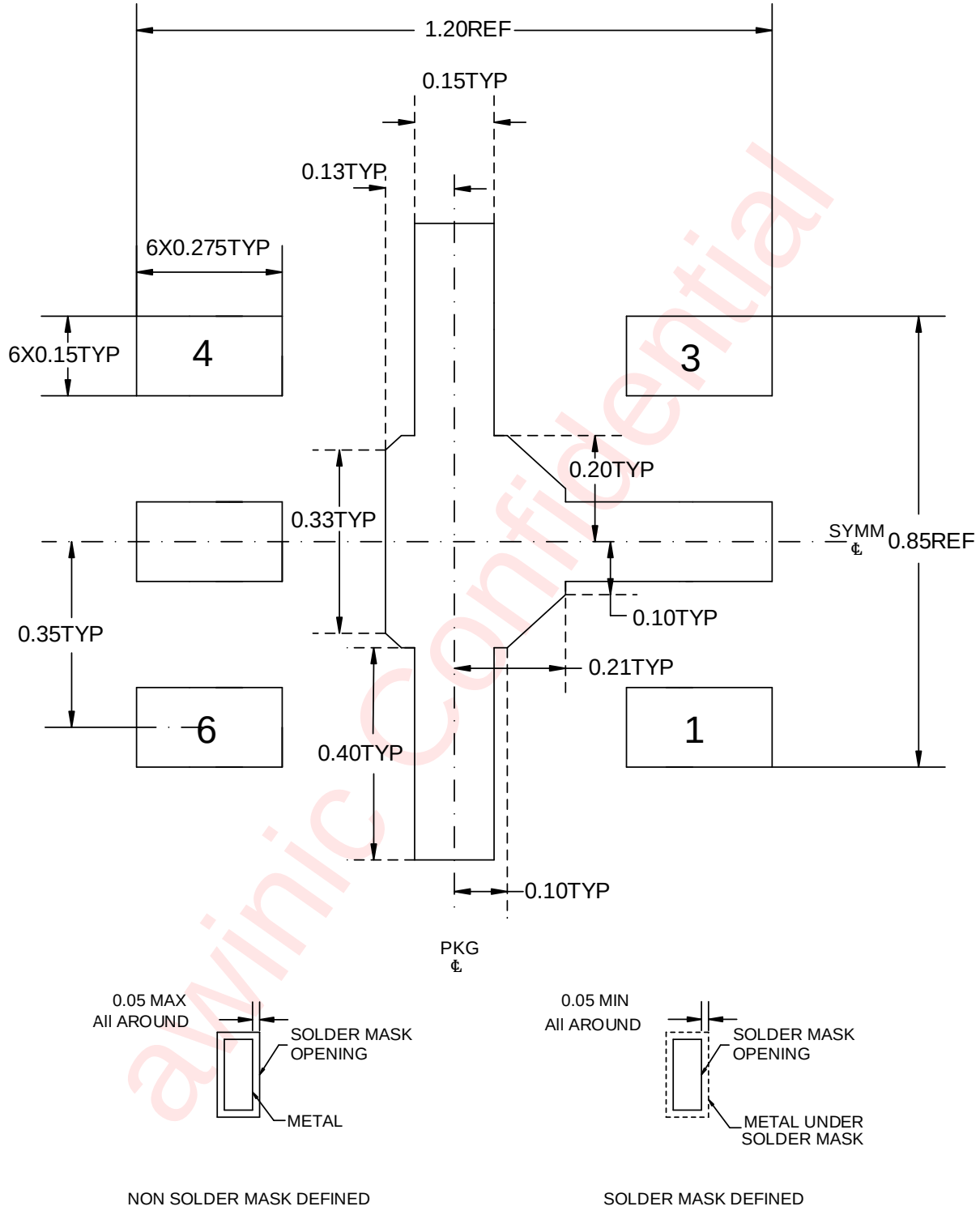
Package Outline Dimensions



Unit: mm

Figure 4 Package Outline

Land Pattern Data

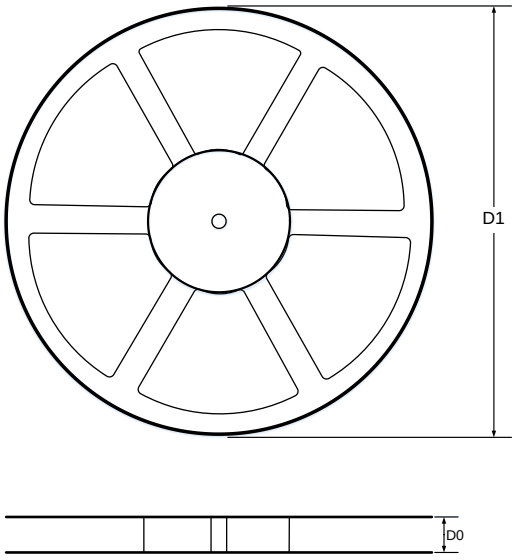


Unit: mm

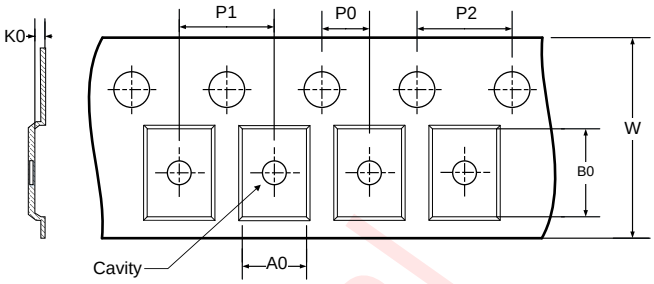
Figure 5 Land Pattern

Tape And Reel Information

REEL DIMENSIONS

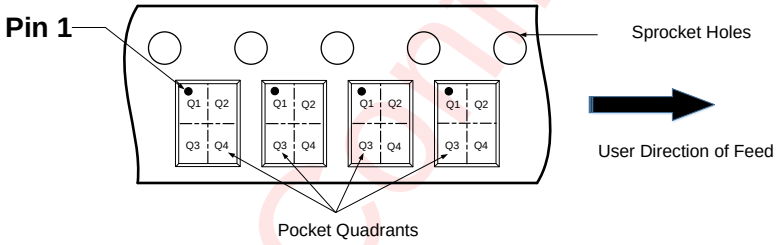


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

All dimensions are nominal

Figure 6 Tape and Reel

Revision History

Vision	Date	Change Record
V1.0	August 2020	Officially Released
V1.1	October 2020	Add the spec IL, ISO, RL and tON
V1.2	December 2020	Change minimum VCTL_H to 1.6 V

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