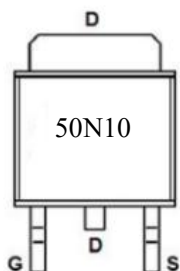
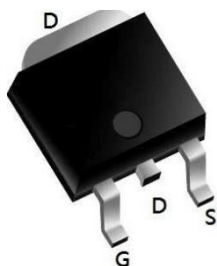


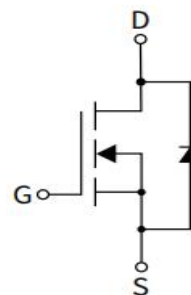
Features	<i>Bvdss</i>	<i>Rdson</i>	<i>ID</i>
	100V	14mΩ	50A
➤ Super Low Gate Charge ➤ Green Device Available ➤ Excellent CdV/dt effect decline ➤ Advanced high cell density Trench technology	Application ➤ PWM applications ➤ Load Switch ➤ Power management		

Package


Marking and pin assignment



TO-252 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
50N10	50N10L	TO-252	2500

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}@10\text{V}$	$T_C = 25^{\circ}\text{C}$	$I_{D1,6}$	50	A
	$T_C = 100^{\circ}\text{C}$		28	A
Pulsed Drain Current ²		I_{DM}	160	A
Single Pulsed Avalanche Energy ²		EAS	350	mJ
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	140	W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient ¹	$R_{\theta JA}$	--	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Case ¹	$R_{\theta JC}$	1.07	$^{\circ}\text{C}/\text{W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL50N10L	TO-252	1	2	3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_J=100^{\circ}\text{C}$	-	-	100	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	0.9	1.3	1.6	V
Static Drain-Source On-Resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	14	17	m Ω
		$V_{GS}=4.5V, I_D=20A$	-	15	18	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=20A$	32	-	-	S
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $f=1\text{MHz}$	-	4700	-	pF
Output Capacitance	C_{oss}		-	176	-	
Reverse Transfer Capacitance	C_{rss}		-	148	-	
Total Gate Charge	Q_g	$V_{DS}=50V, V_{GS}=10V,$ $I_D=20A$	-	119	-	nC
Gate-Source Charge	Q_{gs}		-	11.4	-	
Gate-Drain Charge	Q_{gd}		-	22.9	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=10A,$ $R_G=2.5\Omega, V_{GS}=10V$	-	15	-	ns
Rise Time	t_r		-	11	-	
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	
Fall Time	t_f		-	13	-	
Reverse Recovery Time	t_{rr}	$I_F=10A, dI/dt=100A/\mu s,$ $T_J=25^{\circ}\text{C}$	-	33	-	ns
Reverse Recovery Charge	Q_{rr}		-	54	-	nC
Diode Forward Voltage ²	V_{SD}	$V_{GS}=0V, I_S=20A, T_J=25^{\circ}\text{C}$	-	-	1.2	V
Maximum Continuous Drain to Source Diode Forward Current ^{1,4}	I_S	$V_G=V_D=0V, \text{Force Current}$	-	-	50	A

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $T_J = 25^\circ C$, $V_{DD} = 50V$, $V_{GS} = 10V$, $L = 5mH$
4. The power dissipation is limited by $150^\circ C$ junction temperature
5. The data is theoretically the same as I_p and low, in real applications, should be limited by total power dissipation

Typical Characteristics

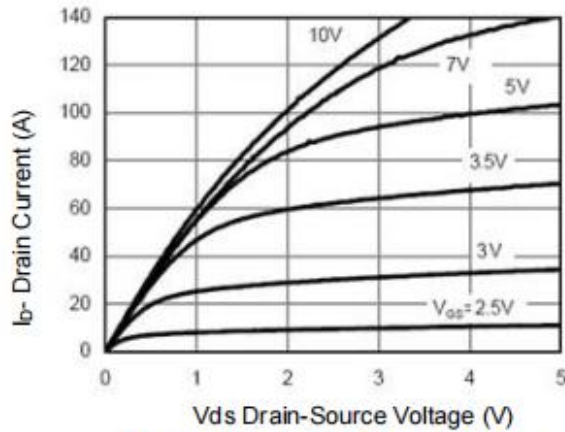


Figure 1 Output Characteristics

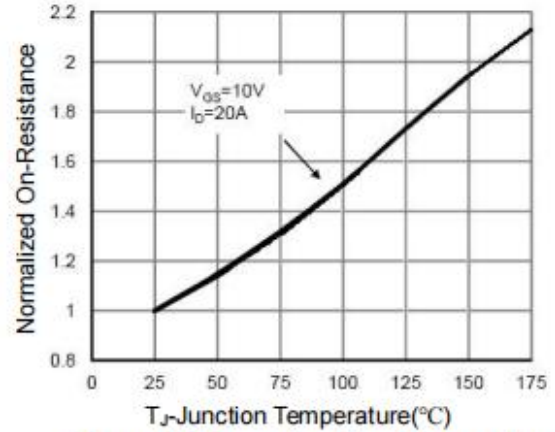


Figure 4 Rdson-Junction Temperature

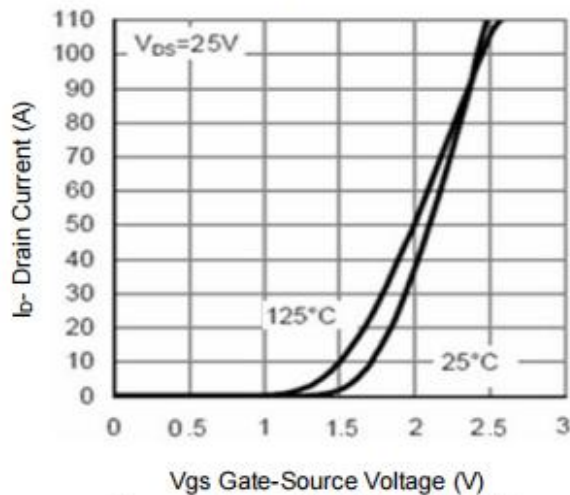


Figure 2 Transfer Characteristics

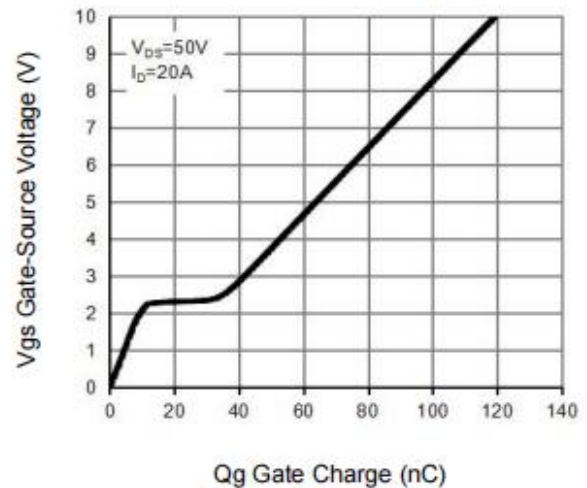


Figure 5 Gate Charge

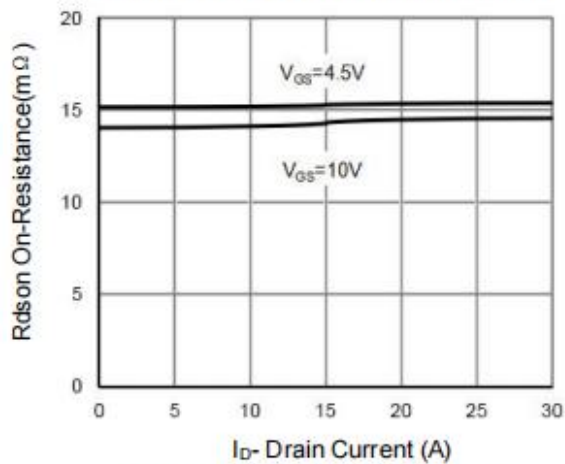


Figure 3 Rdson- Drain Current

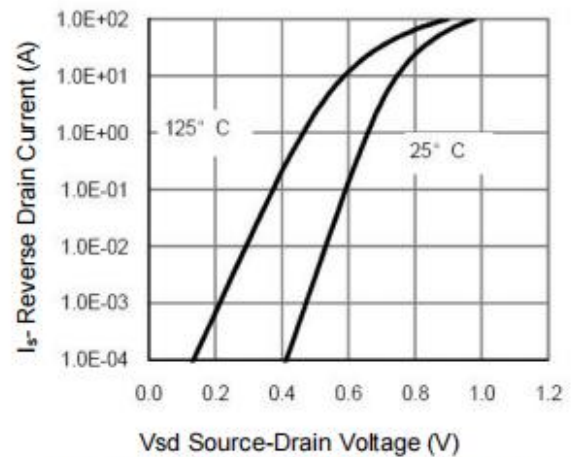


Figure 6 Source- Drain Diode Forward

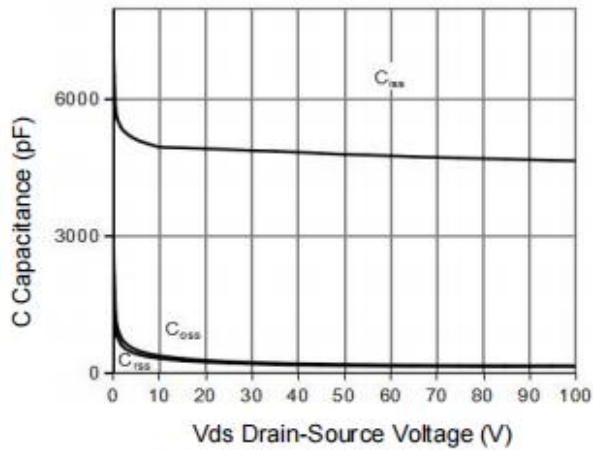


Figure 7 Capacitance vs Vds

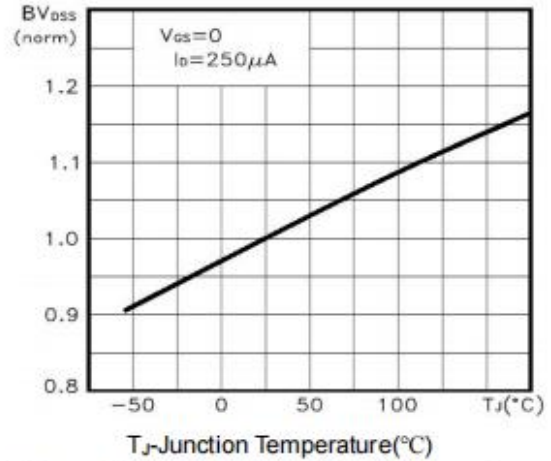


Figure 9 BV_{DSS} vs Junction Temperature

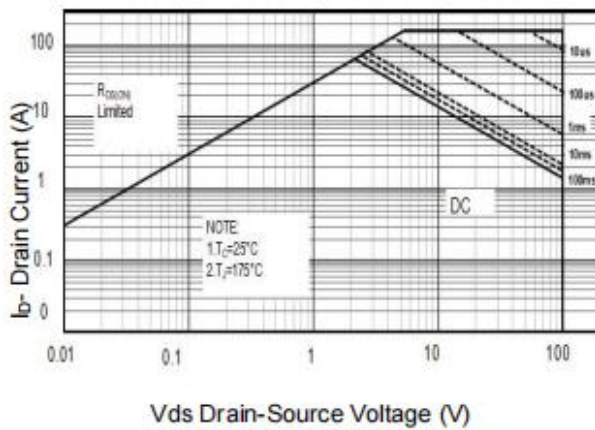


Figure 8 Safe Operation Area

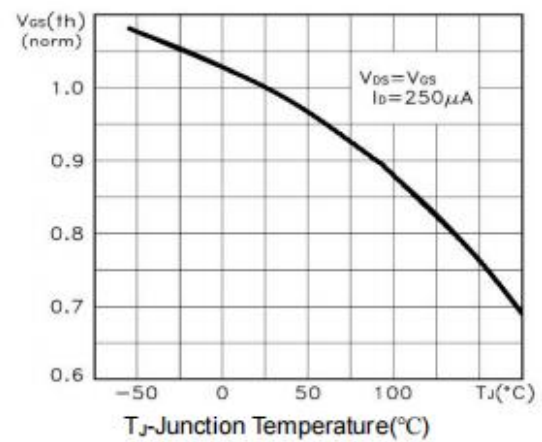


Figure 10 $V_{GS(th)}$ vs Junction Temperature

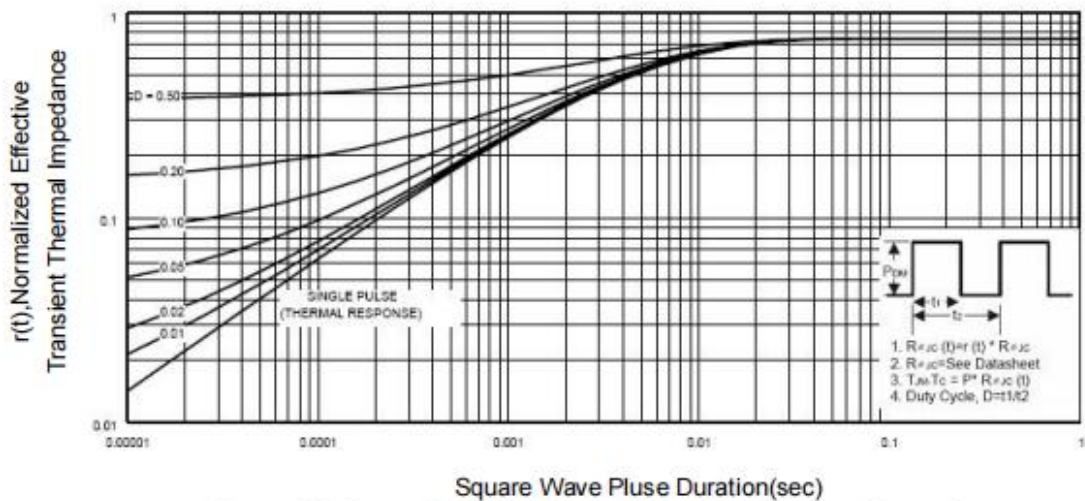
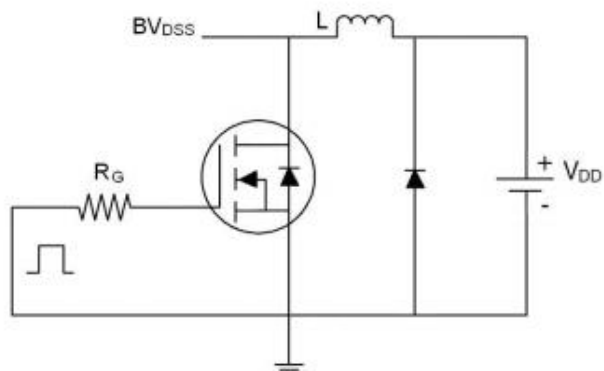


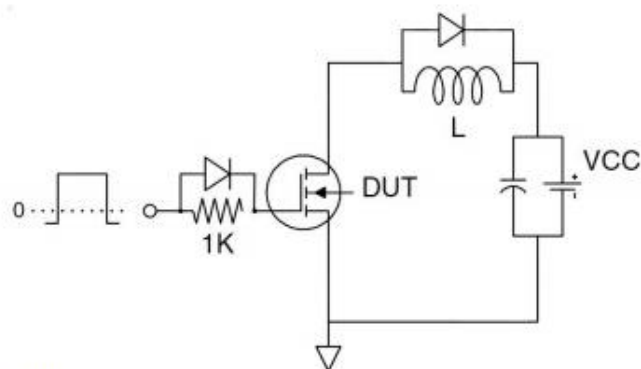
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit

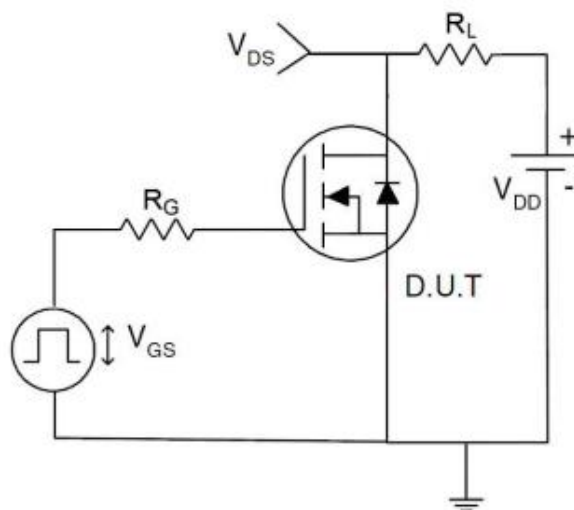
1) E_{AS} test Circuit

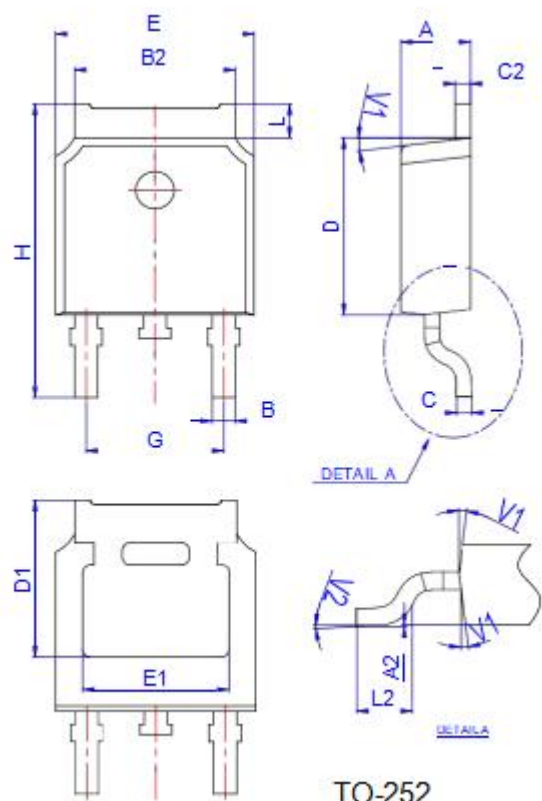


2) Gate charge test Circuit

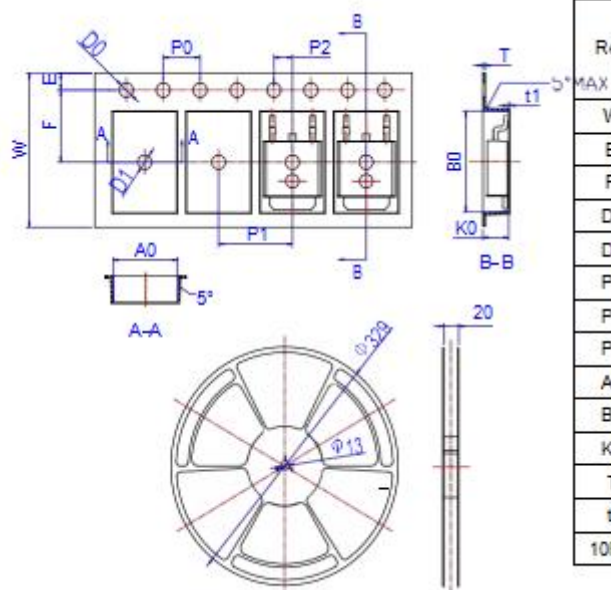


3) Switch Time Test Circuit



Package Mechanical Data TO-252


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583



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