

N- Channel 150V (D-S) MOSFET

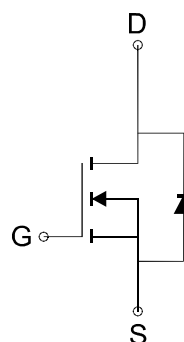
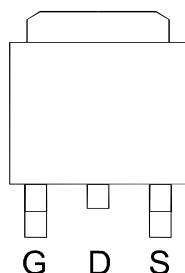
GENERAL DESCRIPTION

The ME12N15 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(TO-252-3L)

Top View



N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 150m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 250m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch

Ordering Information: ME12N15 (Pb-free)

ME12N15-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	Tc=25°C	I_D	13.6	A
	Tc=70°C		10.9	
Pulsed Drain Current		I_{DM}	54	A
Maximum Power Dissipation	Tc=25°C	P_D	44.6	W
	Tc=70°C		28.5	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2.8	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics (T_J=25°C Unless Otherwise Specified)

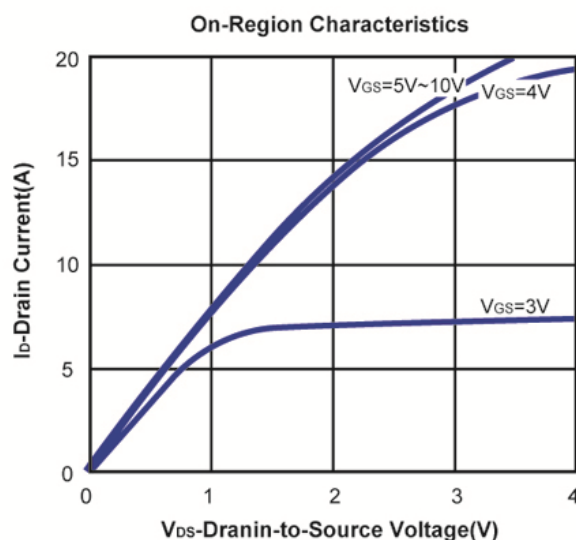
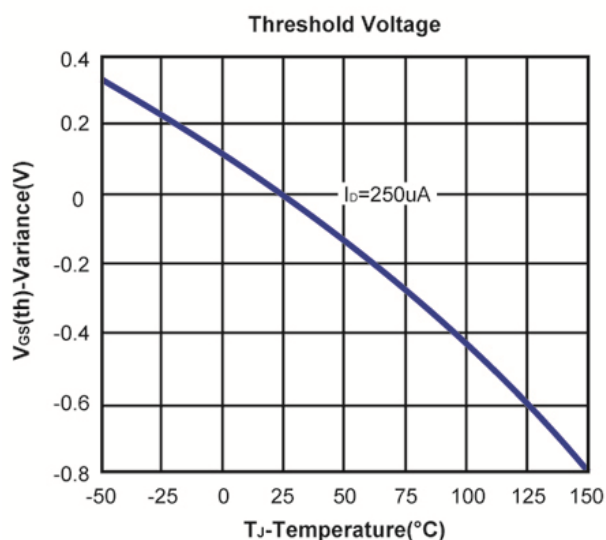
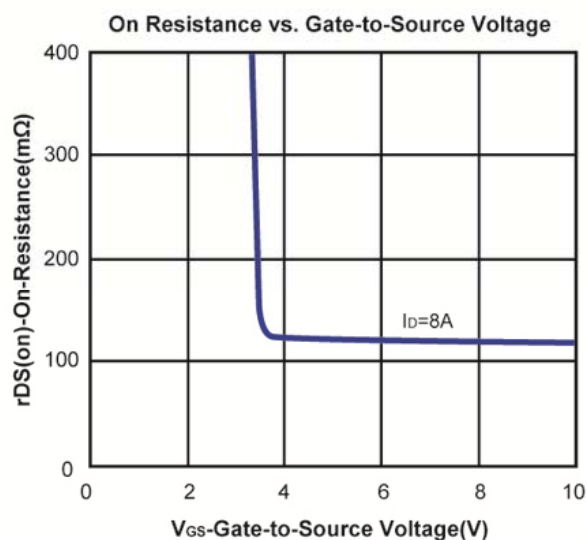
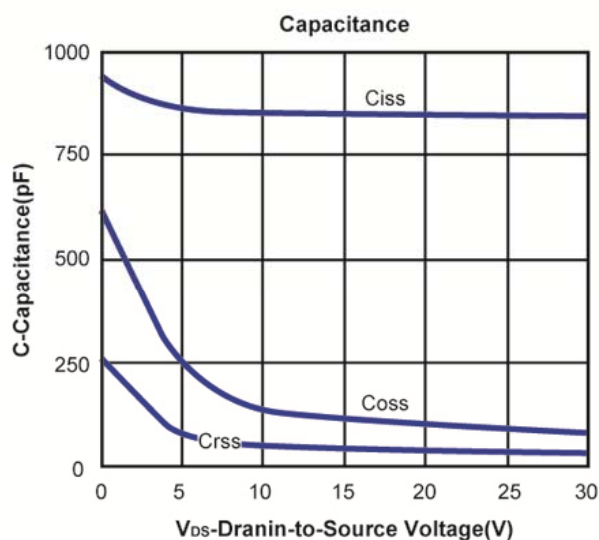
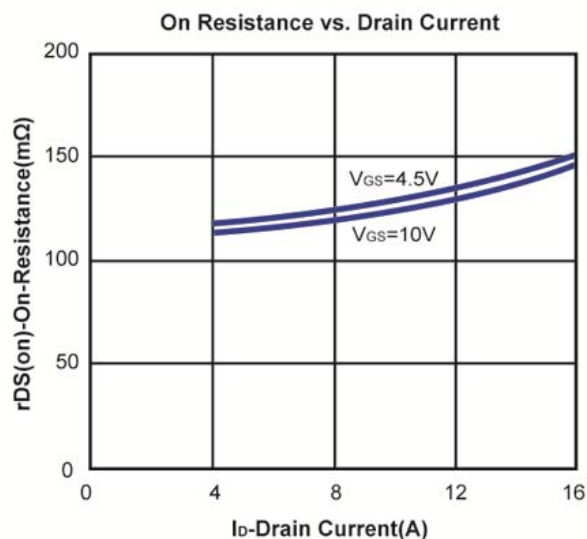
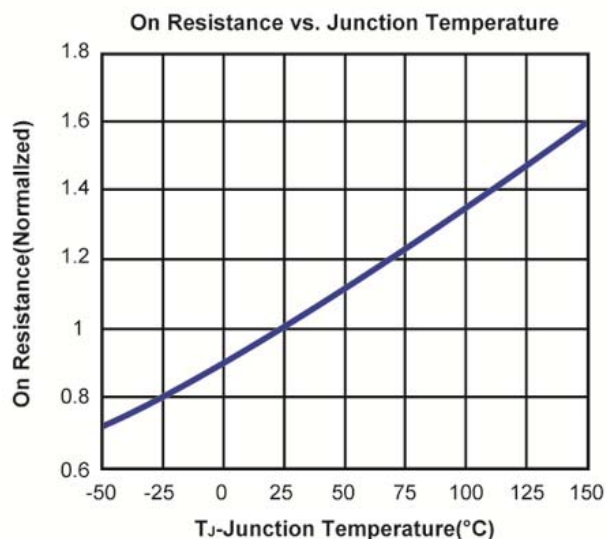
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	150			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	1		3	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} = $\pm$ 20V			$\pm$ 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =8A			150	m Ω
		V _{GS} =4.5V, I _D =5A			250	
V _{SD}	Diode Forward Voltage *	I _S =8A, V _{GS} =0V			1.3	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =120V, V _{GS} =10V, I _D =8A		31.8		nC
Q _{gs}	Gate-Source Charge			5.8		
Q _{gd}	Gate-Drain Charge			9.2		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		839		pF
C _{oss}	Output Capacitance			78		
C _{rss}	Reverse Transfer Capacitance			29		
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DD} =75V, R _G =1 Ω , I _D =8A		13.6		ns
t _r	Turn-On Rise Time			6.2		
t _{d(off)}	Turn-Off Delay Time			36.7		
t _f	Turn-Off Fall Time			3.2		

Notes: a. pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

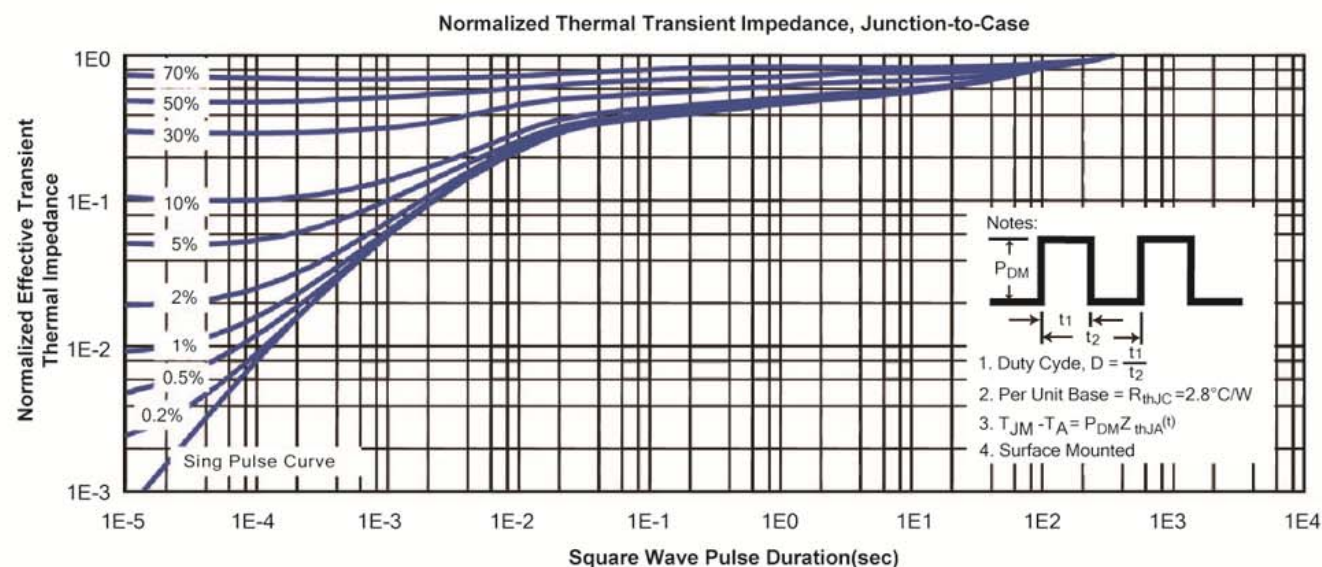
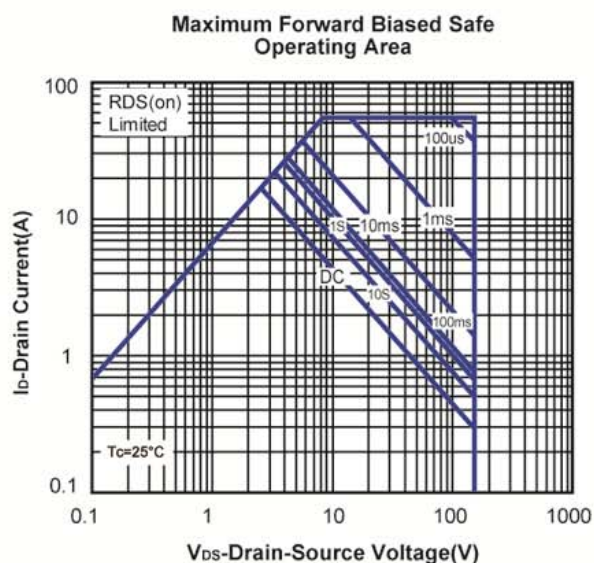
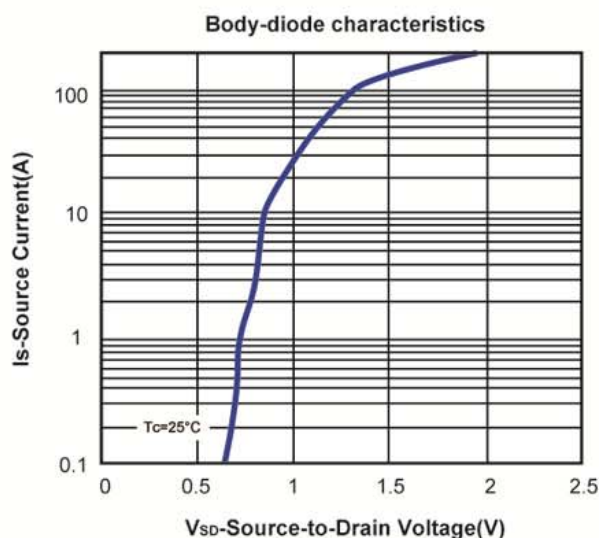
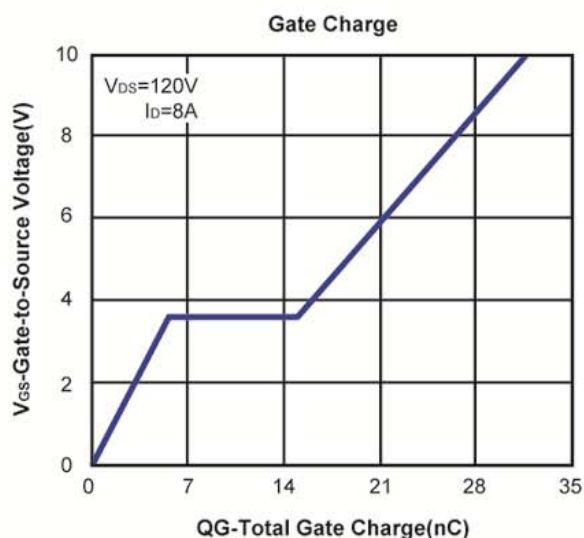
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Typical Characteristics (T_J =25°C Noted)

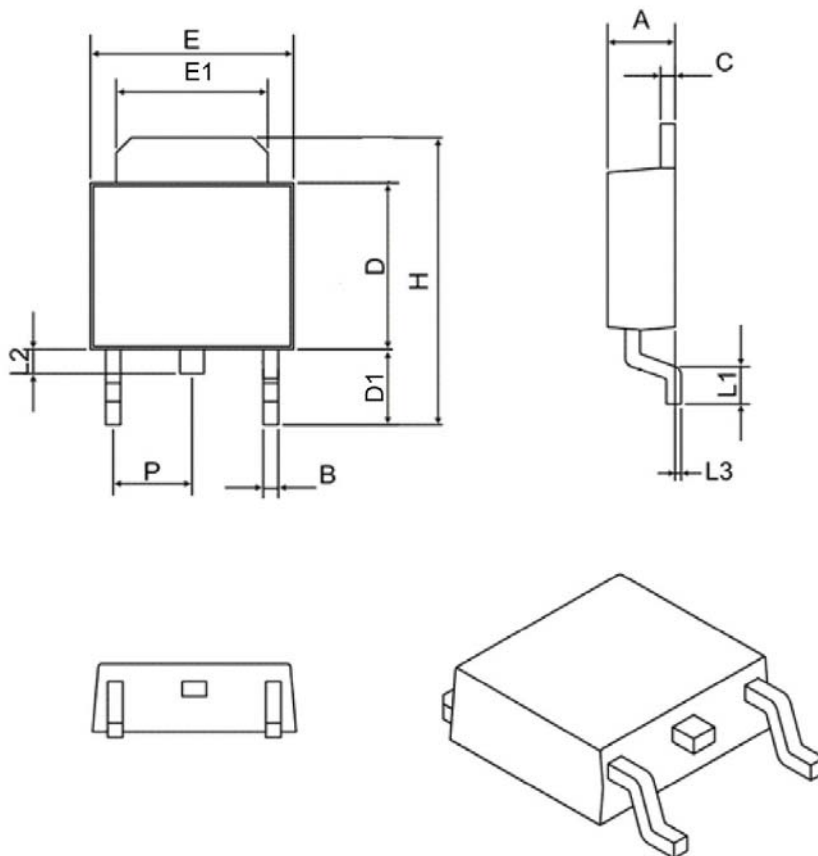


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TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	