Truesemi®

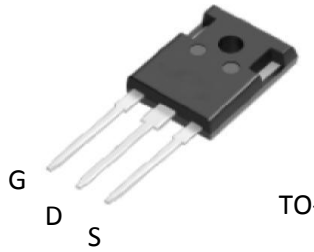
TSK50N50MZ

500V N-Channel MOSFET

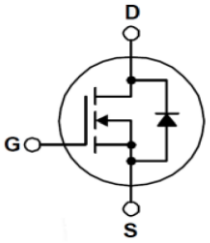
Features

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

- 50A,500V,Max.RDS(on)=0.18Ω @ VGS =10V
- Ultra fast recovery body diode
- 100% avalanche tested
- RoHS compliant device



TO-247



Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		500	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain current (DC) (Note 1)	T_C = 25℃	50	A
		T_C = 100℃	29	A
I_{DM}	Pulsed Drain Current (Note 1)		138	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		6805	mJ
I_{AS}	Single avalanche current (Note 1)		35	A
P_D	Power Dissipation (T_C = 25℃)		568	W
T_J	Junction temperature		150	℃
T_{stg}	Storage temperature range		-55~150	℃

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case	--	0.22	℃/W
$R_{\theta JA}$	Thermal Resistance,Junction-to-Ambient	--	40	℃/W

Electrical Characteristics T_C=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 23A	--	150	180	mΩ
R_g	Internal gate resistance	f=1MHz, Open drain	--	0.75	--	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	25	uA
I_{GSS}	Gate leakage current	V_{DS}=0V, V_{GS}=±20V	--	--	±100	Na
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz (Note 3)	--	8814	--	pF
C_{oss}	Output Capacitance		--	652	--	pF
C_{rss}	Reverse Transfer Capacitance		--	67	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS}= 250 V, I_D = 23 A, R_G = 5 Ω , VGS=10V (Note 3,4)	--	68	--	ns
t_r	Turn-On Rise Time		--	26	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	188	--	ns
t_f	Turn-Off Fall Time		--	26	--	ns
Q_g	Total Gate Charge	V_{DS} =250 V, I_D = 23A, V_{GS} = 10 V (Note 3，4)	--	180	--	nC
Q_{gs}	Gate-Source Charge		--	38	--	nC
Q_{gd}	Gate-Drain Charge		--	56	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	46	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	138	
V_{SD}	Source-Drain Diode Forward Voltage	I_S = 50A, V_{GS} = 0 V	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_S = 50A, V_{GS} = 0 V, dI_S/dt=100A/us (Note 3，4)	--	88	200	ns
Q_{rr}	Reverse Recovery Charge		--	0.27	--	uC

NOTES:

1.Calculated continuous current based on maximum allowable junction temperature

2.L=10mH, I_{AS}=35A, V_{DD}=50V, Starting TJ=25 C

3.Guaranteed by design, not subject to production testing

4. Pulse test: Pulse width≤300us, Duty cycle≤2%

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

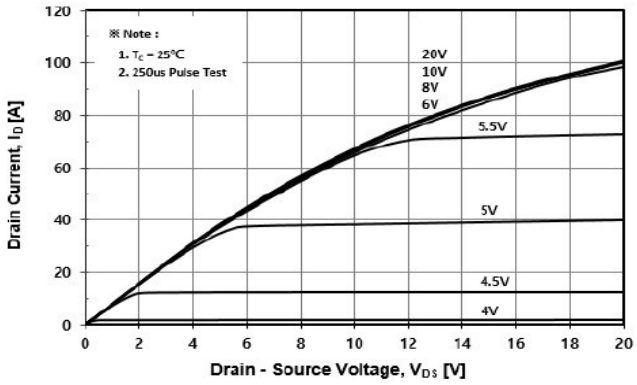


Fig. 2 Typical Transfer Characteristics

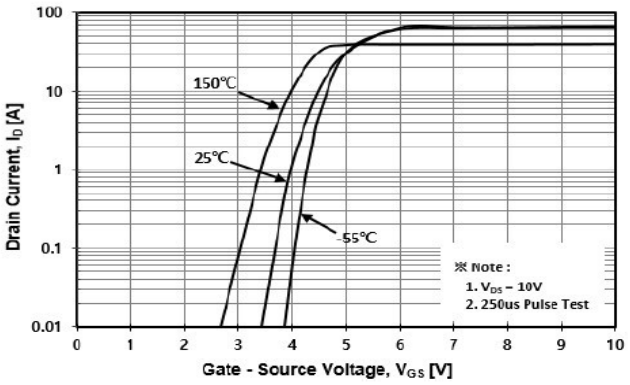


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

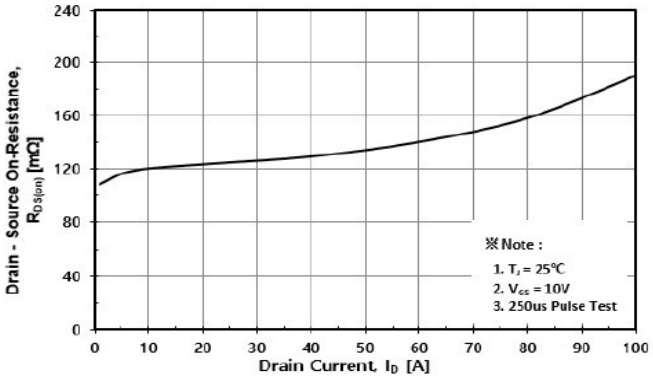


Fig. 4 Body Diode Forward Voltage Variation with Source Current

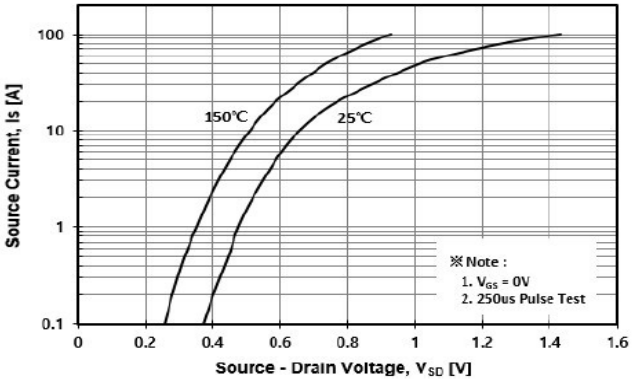


Fig. 5 Typical Capacitance Characteristics

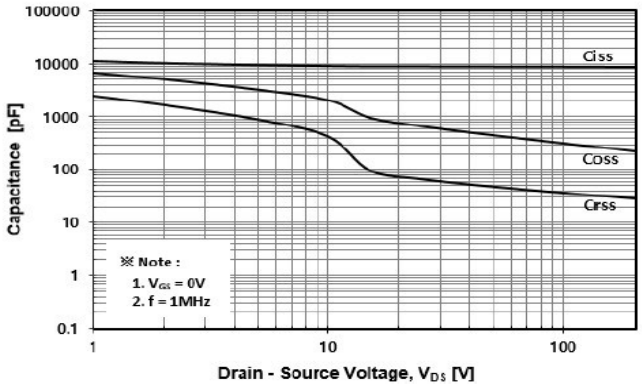
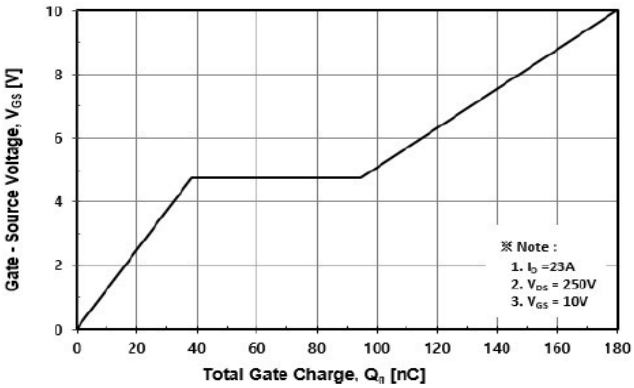


Fig. 6 Typical Total Gate Charge Characteristics



Typical Electrical Characteristics Curves

Fig. 7 Breakdown Voltage Variation vs. Temperature

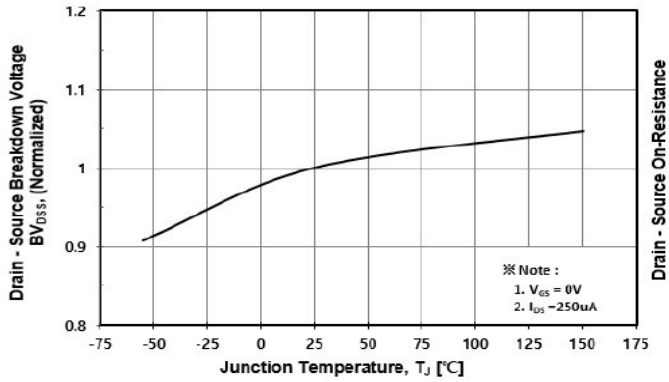


Fig. 8 On-Resistance Variation vs. Temperature

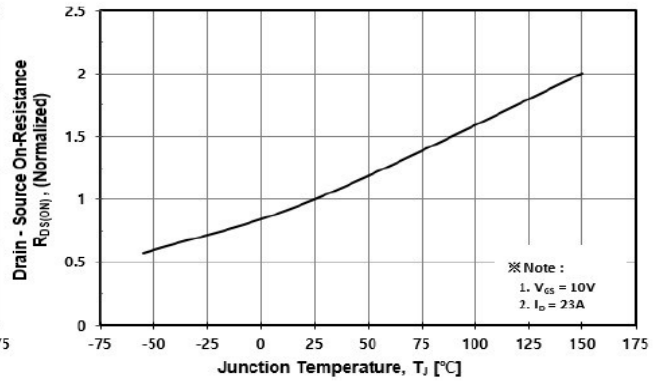


Fig. 9 Maximum Drain Current vs. Case Temperature

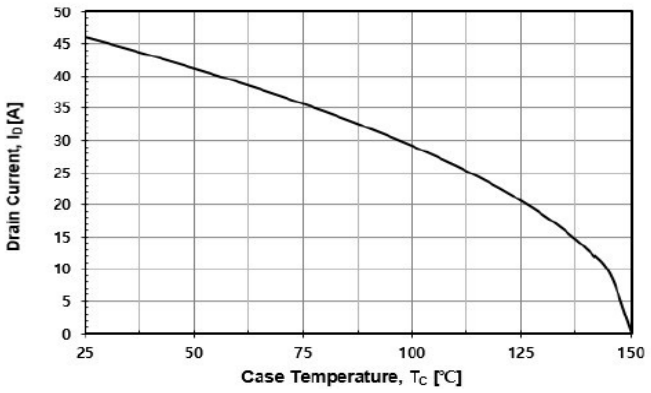


Fig. 10 Maximum Safe Operating Area

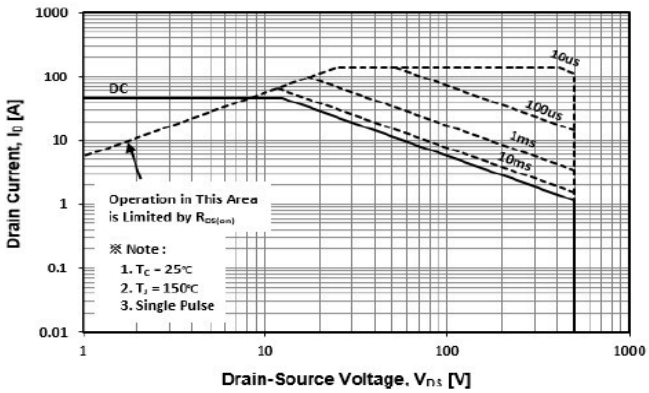


Fig. 11 Transient Thermal Impedance

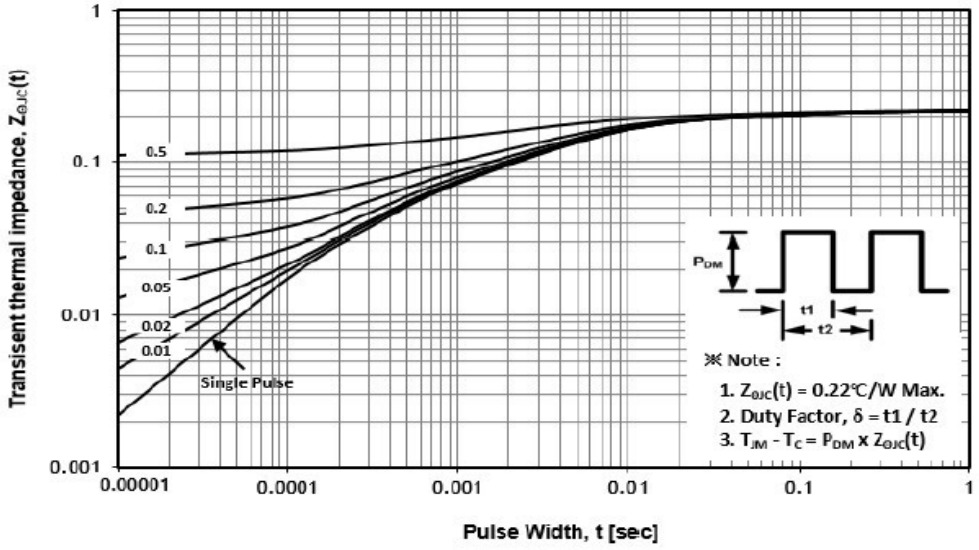
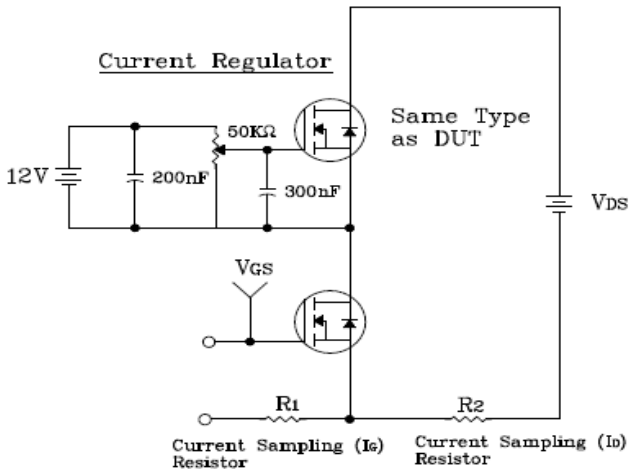


Fig. 12 Gate Charge Test Circuit & Waveform



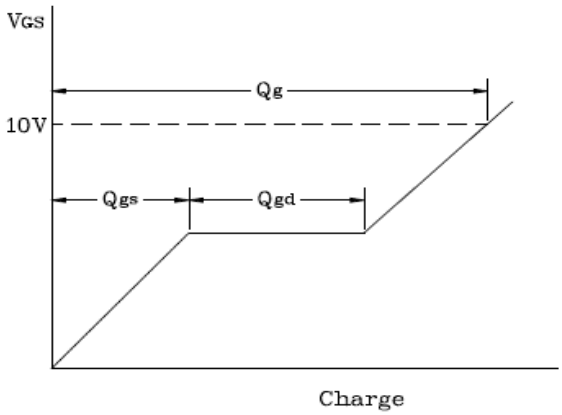
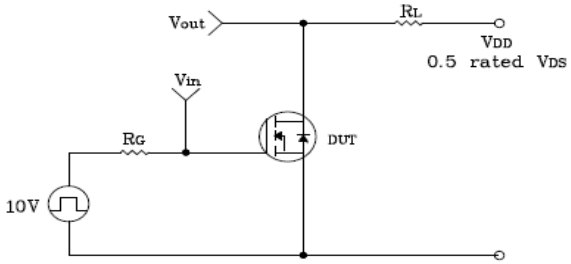


Fig. 13 Resistive Switching Test Circuit & Waveform



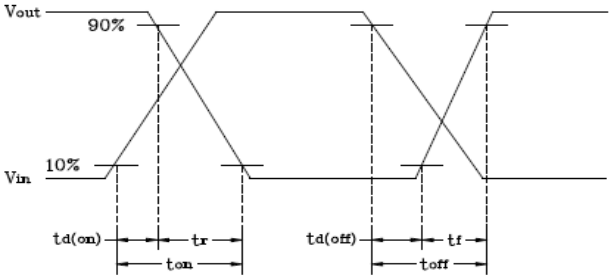
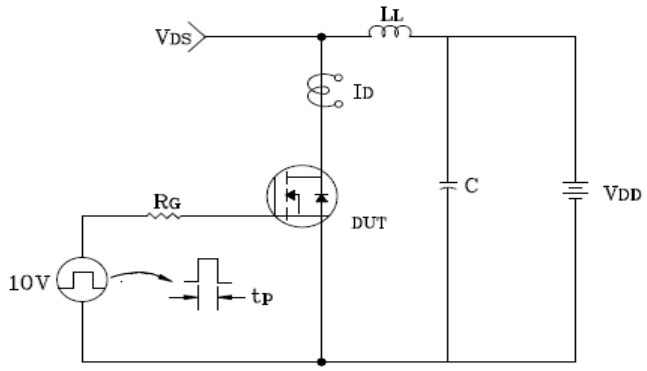


Fig. 14 E_{AS} Test Circuit & Waveform



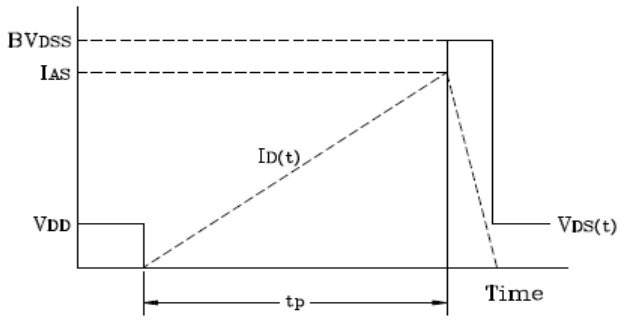


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform