5-Channel Capacitive Touch and Proximity Controller

FEATURES

- 5-channel capacitive sensing
  - Self-capacitive sensing techniques
  - Auto-Calibration
  - Capacitance resolution down to 4aF
  - With range of parasitic capacitance: 0~220pF
  - Independent configurations per channel
- 400kHz I²C interface
  - Default address: 0x12
  - Address can be modified through CS2 pin
- External interrupt pin, open-drain output
- Built-in brown-out reset(BOR)
- Low power consumption
  - Active mode: 26 uA
  - Doze mode: 9uA
  - Deep sleep mode: 4 uA
- 1.7V~3.6V power supply
- Operation temperature range:-25°C~85°C
- DFN 2.1mm×1.8mm×0.55mm-10L package

APPLICATIONS

Mobile phones

Wearable Devices

GENERAL DESCRIPTION

AW96105 is a 5-channel low power capacitive touch and proximity controller. Each channel can be independently configured as sensor input, shield output.

Advanced self-capacitance technology is adopted in AW96105, which supports parasitic capacitance compensation for each channel up to 220pF. For the device has a high resolution ADC, the minimal capacitance that can be detected is as low as 4aF.

AW96105 integrates a low power MCU, by executing the algorithm program in the ROM, it is capable to perform the basic operations such as signal filtering, baseline calculation, automatic compensation for environmental drift, RF noise suppression, proximity judgment, etc..

One or two sensor channels can be configured as reference channel. The reference channel and internal temperature sensor can be used to correct the detected result. With the help of auto calibration, the device is able to track slow environmental variations(such as temperature, humidity, etc.) and maintain high performance operation.

TYPICAL APPLICATION CIRCUIT

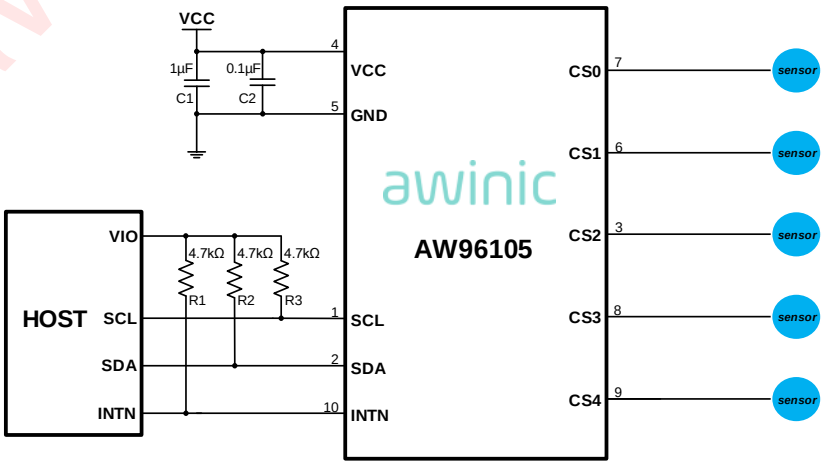
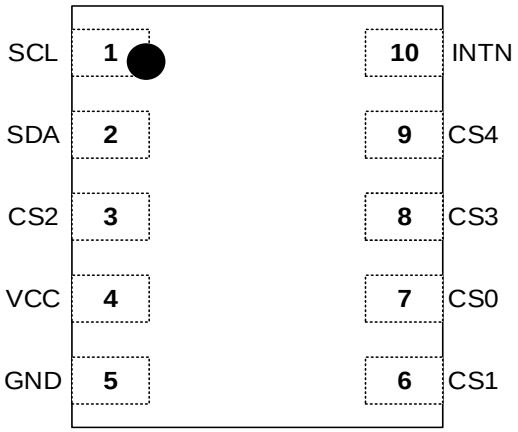


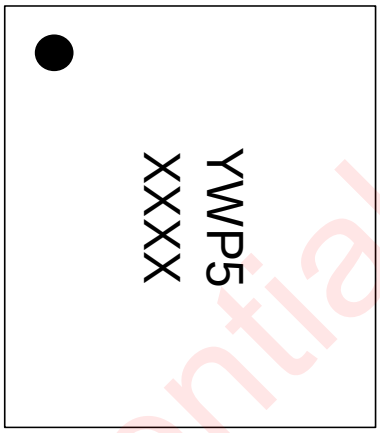
Figure 1 AW96105 Typical Application Circuit

PIN CONFIGURATION AND TOP MARK

AW96105DNR
(TOP View)



AW96105DNR Marking
(TOP View)



YWP5 - AW96105DNR
XXXX - Product Tracing Code

PIN DEFINITION

No.	NAME	DESCRIPTION
1	SCL	I^2C clock, requires pull-up resistor
2	SDA	I^2C data, requires pull-up resistor
3	CS2	Capacitive Sensor input/shield or I^2C address select Input (Floating:0x12, GND:0x13, VCC:0x14)
4	VCC	Power supply（1.7V~3.6V）, requires decoupling capacitor
5	GND	Ground
6	CS1	Capacitive sensor input/shield
7	CS0	Capacitive sensor input/shield
8	CS3	Capacitive sensor input/shield
9	CS4	Capacitive sensor input/shield
10	INTN	Interrupt output, requires pull-up resistor

FUNCTIONAL BLOCK DIAGRAM

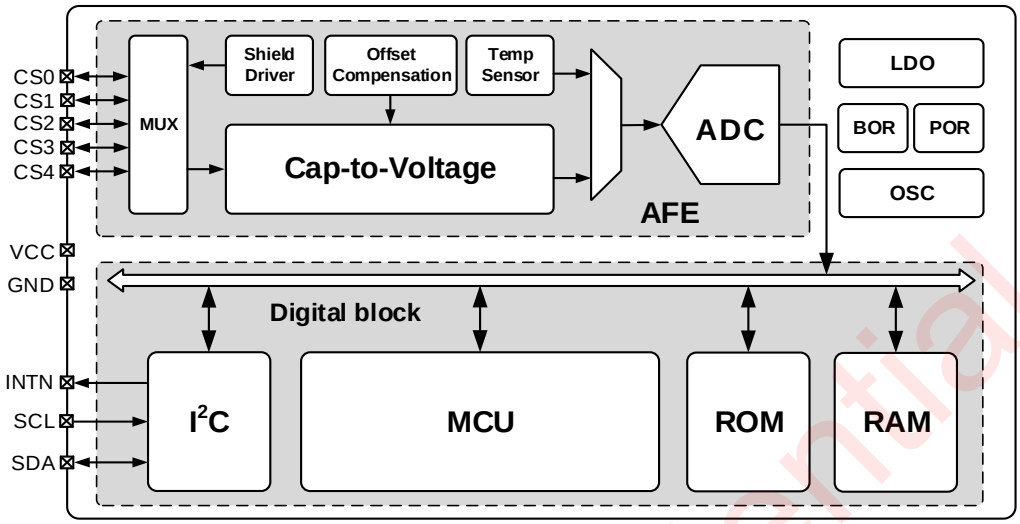


Figure 2 Functional Block Diagram

Notes: AFE means Analog Front-End.

TYPICAL APPLICATION CIRCUITS

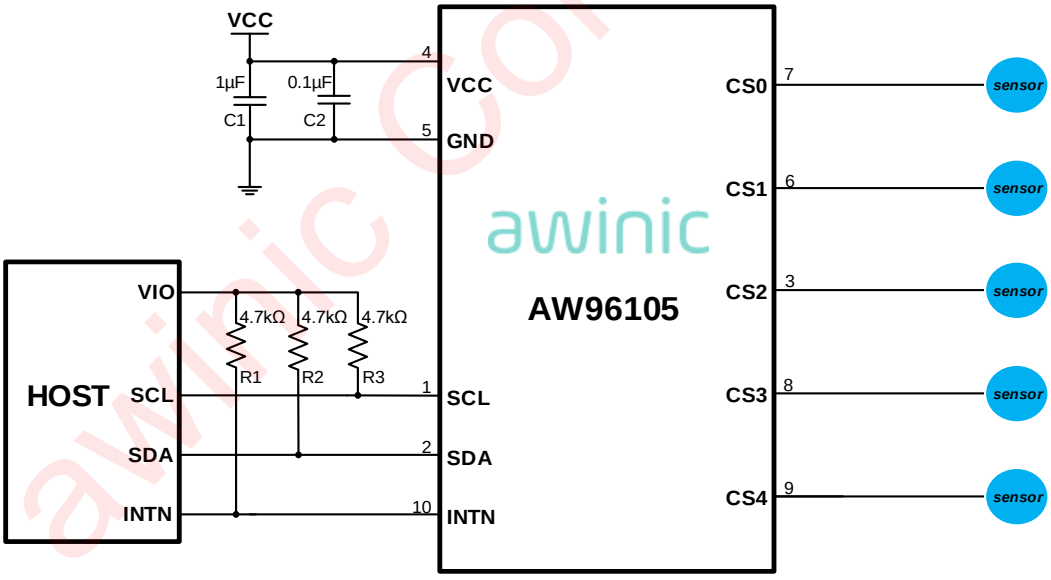


Figure 3 AW96105 Typical Application Circuit (for Touch Key)

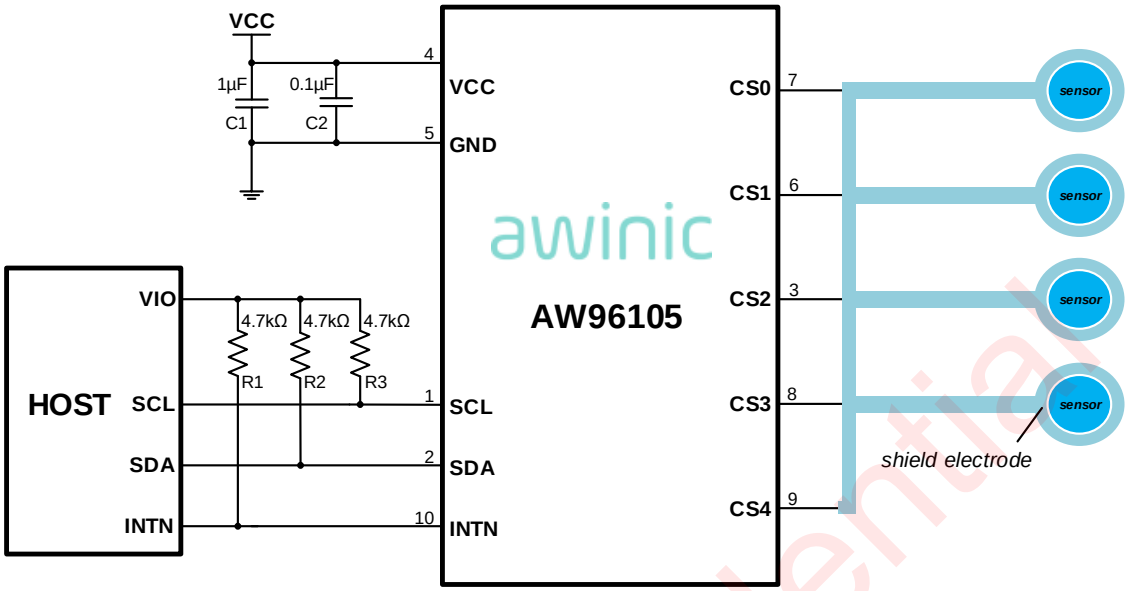


Figure 4 AW96105 Typical Application Circuit (for Touch Key)

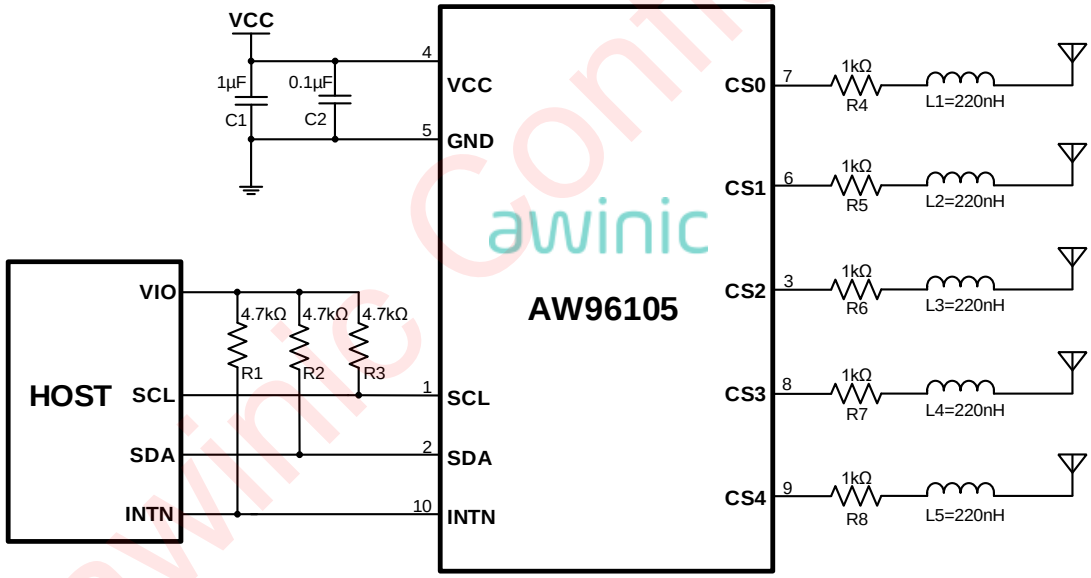


Figure 5 AW96105 Typical Application Circuit (for SAR Sensor)

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW96105DNR	-25℃～85℃	DFN 2.1mmX1.8mm-10L	YWP5	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.5V to 3.6V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Junction-to-ambient thermal resistance θ_{JA}		
Operating free-air temperature range		-25°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM MM)(NOTE 2)		
HBM		±4kV
CDM		±1.5kV
Latch-Up		
Test condition: according to JESD78E		+IT：350mA -IT：-350mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: MIL MIL-STDSTDSTD-883J ,the CDM test method: ANSI/ESDA/JEDEC JS-002-2018.

ELECTRICAL CHARACTERISTICS

Note:Typical values are given for T_A = +25°C, VCC=2.8V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS						
$I_{DEEPSLEEP}$	Deep Sleep Mode Current	LDO on, OSC off, I²C listening.	-	4	8	μA
I_{DOZE}	Doze Mode Current	SCANPERIOD=400ms; FREQ =100kHz; RESOLUTION=64; SSEN=1;ADC filt. and Adv. features/engines OFF. I²C listening. No load.	-	9	16	μA
I_{ACTIVE}	Active Mode Current	SCANPERIOD=30ms; FREQ=100kHz; RESOLUTION=64; SSEN=1; ADC filt. and Adv. features/engines OFF. I²C listening. No load.	-	26	48	μA
CAPACITANCE SENSING						
C_{RANGE}	Measurement Range		±0.55	±2.2	±9.9	pF
N_{BIT}	Measurement Resolution		-	20	-	bits
C_{RES}			-	4	-	aF
F_{OSC}	Nominal OSC Frequency		-	4	-	MHz
F_{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C,VCC=2.8V	-4	-	4	%
F_{Temp}	OSC Temp. Dependency	Around Nominal Value, Ta=25°C,VCC=2.8V		±1	-	%
F_{VCC}	OSC VCC Dependency	Around Nominal Value, Ta=25°C,VCC=2.8V	-	±0.6	-	%
Fs	Nominal Sampling Freq	Programmable with FREQ	-	-	250	kHz
C_{DCEXT}	External DC Cap.to GND per Measurement Phase	One CSx as measured input	-	-	220	pF
$R_{FILTINUNIT}$	Pre-Charge Input Res		0	-	30	kΩ
$R_{INTUNIT}$	Compensation Res		0	-	8	kΩ
TEMPERATURE SENSING						
$T_{INRANGE}$	Input Range	Ambient Temperature(T_A)	-25	-	85	°C
$T_{OUTRANGE}$	Output Range		0	-	32767	LSB
I²C INTERFACE						
I_{OL} （SDA，INTN）	Output low current	VOL≤0.4	8			mA
V_{IH}	Input high level	SCL, SDA	1.35		3.6	V
V_{IL}	Input low level	SCL, SDA	-0.5		0.45	V
t_{DEG_SDA}	SDA deglitch time	SDA		110		ns
t_{DEG_SCL}	SCL deglitch time	SCL		95		ns

I²C INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency	-		400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	μs
T_{LOW}	Low level width of SCL	1.3		-	μs
T_{HIGH}	High level width of SCL	0.6		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	μs
$T_{HD:DAT}$	Data hold time	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	μs
T_R	Rising time of SDA and SCL	-		0.3	μs
T_F	Falling time of SDA and SCL	-		0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	μs

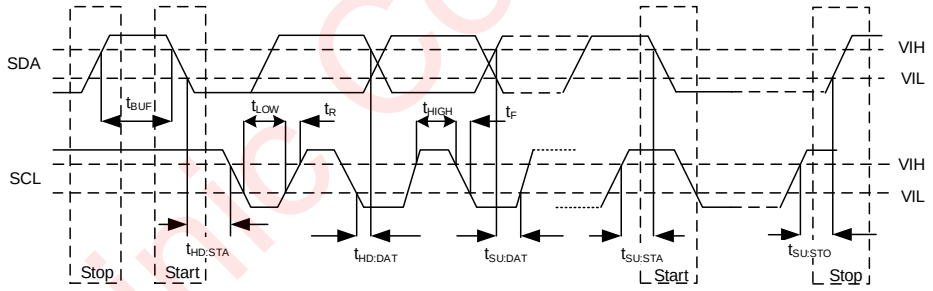


Figure 6 I²C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

AW96105 is a capacitive touch and proximity controller with built-in a low power MCU. It's based on self-capacitive sensing technology, and mainly includes AFE, MCU, ROM, RAM, OSC, I²C, etc.. AFE is mainly used to drive the sensor and shield electrode, and convert the capacitance of sensor to digital data. MCU executes the algorithm program in the ROM, and perform basic operations such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity judgment, etc..

CAPACITIVE SENSOR INTRODUCTION

Self-capacitive sensing technology detects the change in the capacitance of a touch or proximity sensor when a target object approaches the sensor. The target object can be a human finger, face, or any conductive object. The figure below shows the basic structure and equivalent model of a capacitance sensor. The top layer is the overlay, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance(C_{PARA}).

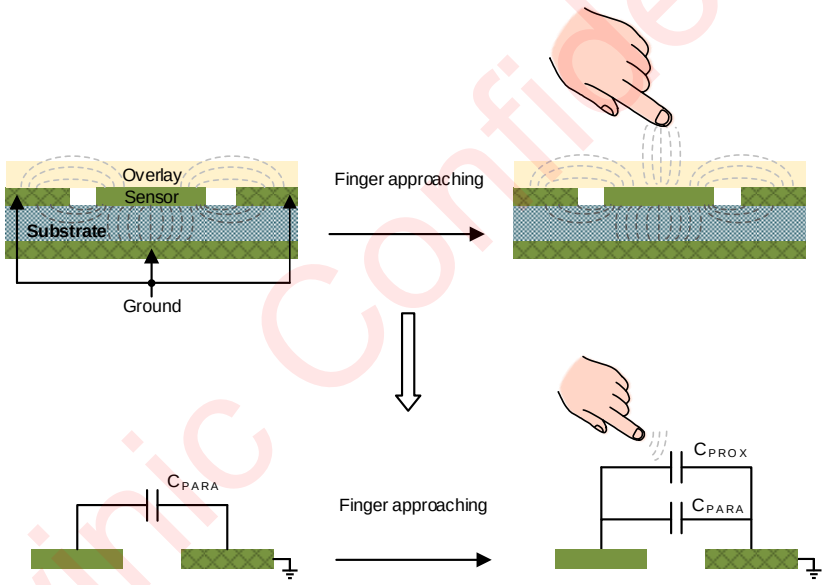


Figure 7 Capacitive sensor structure

An electric field is created around the sensor when it is working. As the target object approaches the electrode, some of the electric field lines couples to the target object and add a small amount of finger capacitance (C_{PROX}) to the existing C_{PARA}. This feature can be used to detect proximity or touch action.

CAPACITIVE SENSING TECHNIQUES

The proximity sensing system consists of three parts, capacitive sensor, AFE and DSP. The sensor capacitance will change when the target object is approaching or moving away. AFE drives the capacitive sensors and shield electrodes, and converts the sensor capacitance to digital data. DSP deals with the data from AFE, and passes sensor capacitor value(CapDiff, CapValid) and proximity status(Status) to the host.

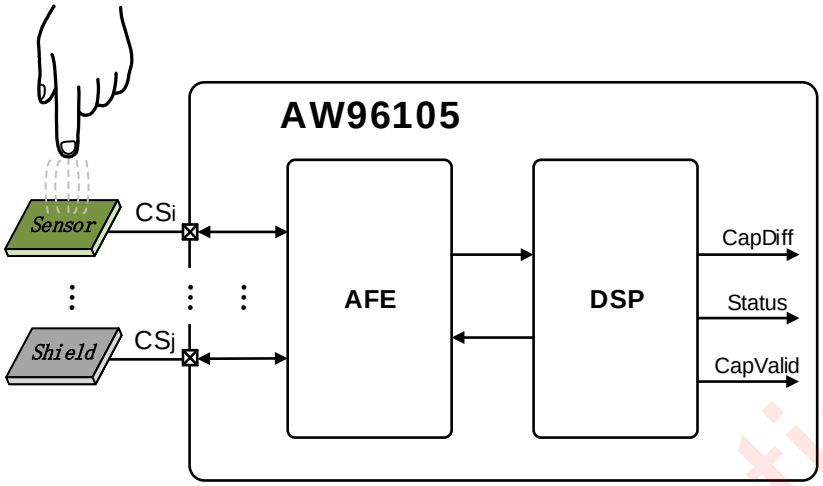


Figure 8 Proximity Sensor Operation Overview

AFE DESCRIPTION

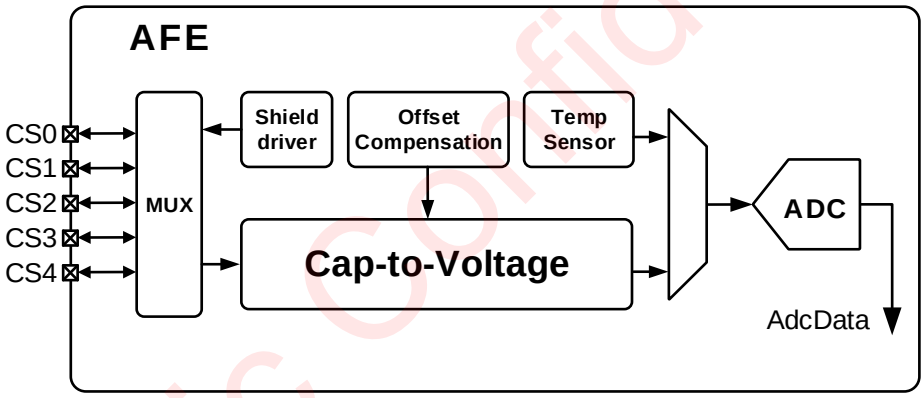


Figure 9 AFE Block Diagram

※ MUX selects CSx as capacitance measurement input or shield output

※ If CSx is used as shield electrode, it is excited by shield driver. The driven shield signal is a replica of the sensor signal. Shield electrode around can protect the sensor from noisy environment，and reduce the parasitical capacitance.

※ Cap-to-Voltage integrates a charge amplifier, it detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of ADC.

※ Offset Compensation measures parasitic capacitance(C_{PARA}), and C_{PARA} is compensated in the process of charge transferring of Cap-to-Voltage. Thus, the input capacitance of Cap-to-Voltage is almost only C_{PROX}.

※ Temp Sensor measures the temperature of the chip, and the output is converted by ADC to digital data. The temperature data can be used as reference to correct the capacitance measurement result.

※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.

DSP DESCRIPTION

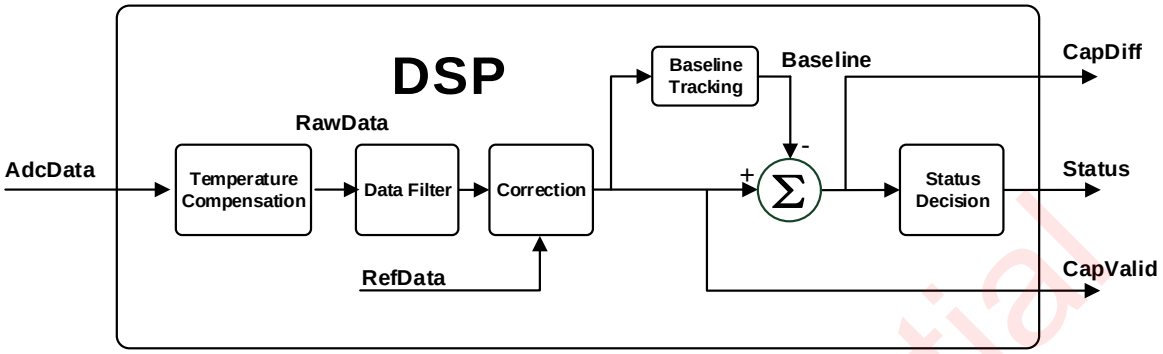


Figure 10 Digital signal processing diagram

※ DSP mainly processes the data from the AFE to judge whether a target object is approaching.

※ Temperature Compensation is mainly used to reduce the effect of temperature drift.

When set AFECFG3_CHx.TEMPCOMPEN_CHx = 1 (Addr: 001Ch), the temperature compensation is performed for Channel x (x=0~4). The RawData after compensation can be expressed as follows,

RawData = AdcData(1+ TEMPGAIN *DeltaT) + CAPTEMPCOEF *TEMPGAIN *DeltaT*

Where, TEMPGAIN is defined in register TEMPCOMP(Addr: 000Ch), DeltaT is the AdcData change corresponding to the temperature change sensing by temperature channel, CAPTEMPCOEF is decided by the register AFECFG3_CHx.CAPTEMPCOEF_CHx(Addr: 001Ch). And the temperature channel can be configured as CH0~CH5 through the register TEMPCOMP. TEMPCH.

※ Data Filter filters the input RawData, and high-frequency noise is filtered out, then the output data shows a higher signal-to-noise ratio(SNR).

※ In order to further eliminate data fluctuations due to the noise source, the data from Data Filter will be corrected by the RefData. RefData is from reference channel or internal temperature sensor.

※ Baseline Tracking provides a baseline that follows undesired variations caused by environmental changes(such as temperature, humidity, etc.)

※ The calculation of data change due to human proximity is

CapDiff = CapValid - Baseline

※ Status Decision uses CapDiff to decide whether a target object is approaching.

SCAN PERIOD

A scan period is divided into 3 segments. In first segment, AFE scan the sensor channels to get the RawData. Then, AFE is off and DSP starts processing the RawData. The chip will be in idle state in the last segment during which MCU sleeps.

The figure above shows the scanning period of active mode and doze mode. The scan period of active mode can be configured by register SCANCTRL1(Address: 0x004H). Scan period of doze mode is N times of active mode. And N can be configured through the register SCANCTRL0(Address: 0x000H). Thus, doze mode consumes much lower power than active mode. Scan period can be configured independently for each channel.

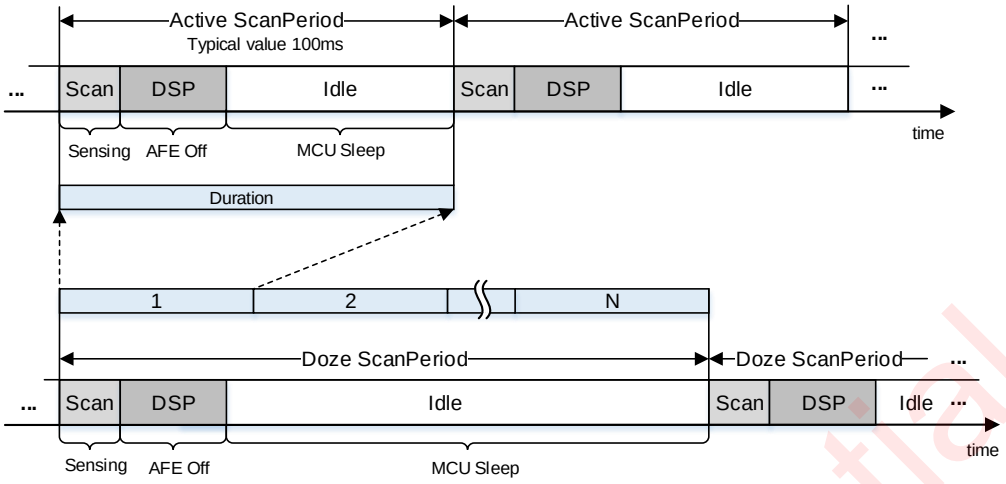


Figure 11 Active mode and Doze mode scan period

CLOCK

OSC is built in the chip, so no external clock is needed. It generates a 4MHz clock to the digital circuit.

RESET

POWER ON RESET (POR)

Reset operation is triggered during power up. When nRST released, the initialization process starts to perform and it will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.

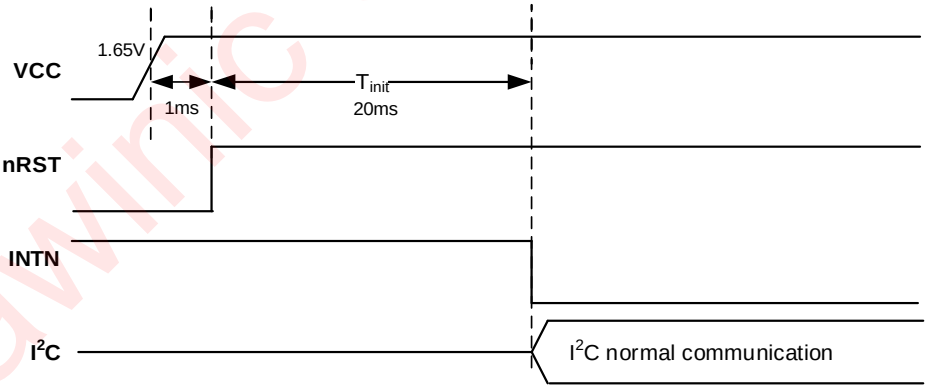


Figure 12 Power On Timing

BROWN OUT RESET (BOR)

Reset operation is triggered when VCC drop to the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

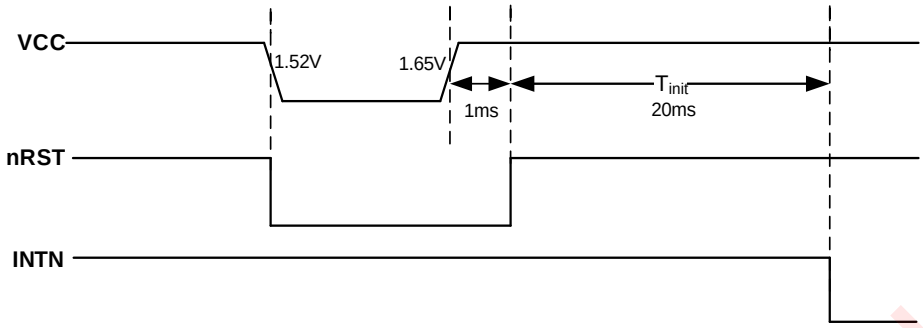


Figure 13 Brown Out Timing

SOFT RESET

The soft reset operation can be triggered by writing the soft reset register (Address: 0xFF0F). After the reset operation, all the registers will be reset to the default value.

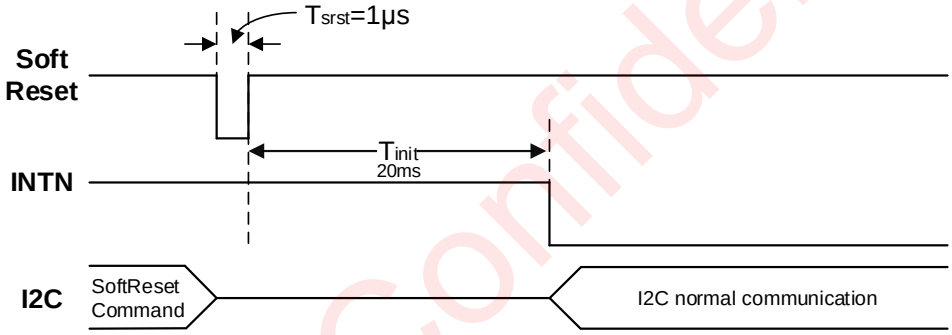


Figure 14 Soft Reset Timing

INITIALIZATION

After power on, OSC runs normally, and MCU starts to execute the initialization program in ROM. It performs the following operations.

- Read information from NVM
- Set I²C device address according to CS2 pin status
- Complete high-resolution ADC calibration
- Set interrupt for initialization completion and enter sleep state

OPERATION MODE

There are four operation modes in the chip: DeepSleep, Sleep, Active and Doze. When a certain condition is met, it will change from one operation mode to another.

DEEPSLEEP

The device consumes the lowest power. OSC and AFE are off, CPU is sleeping, only I²C interface is active.

SLEEP

The device is in a low power state. OSC is on, AFE is off, and MCU is sleeping, waiting for interrupt to wake up.

ACTIVE

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no detection has occurred for some time, it will automatically switch to Doze mode. In this mode the external HOST can send SLEEP command to switch the device to sleep mode.

DOZE

The scan period is long, MCU and AFE work intermittently. During the large part of period, most modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send SLEEP command to switch the device to sleep mode.

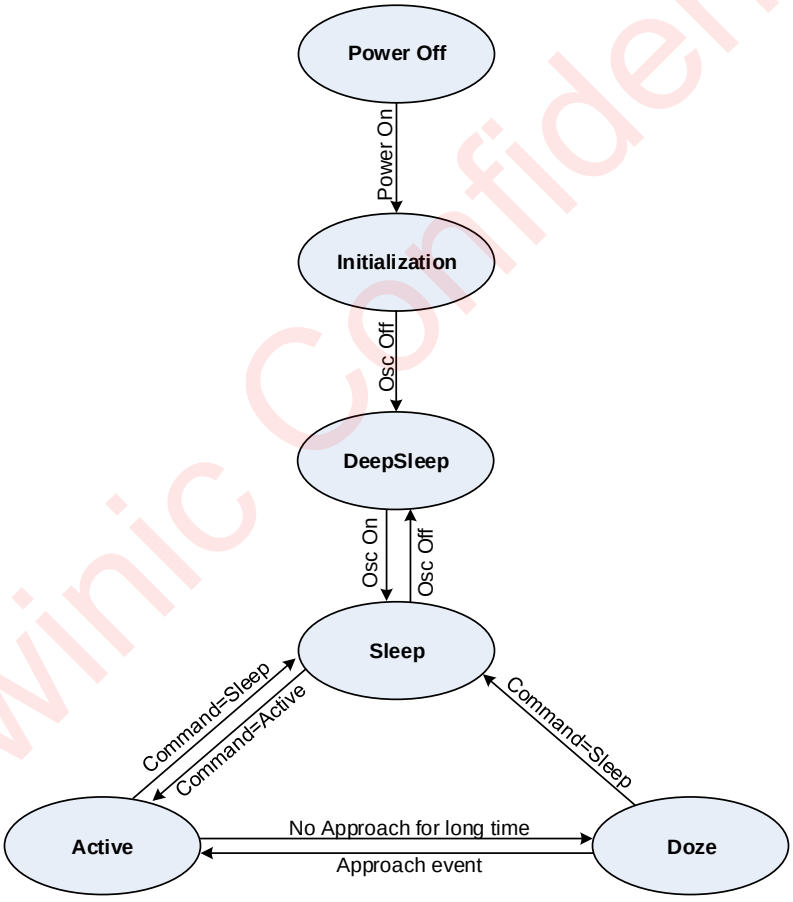


Figure 15 Operation Mode Switching

INTERRUPT

The chip reports the interrupt signal to the host through the INTN pin. Register HOSTIRQSRC(Address: 0xF080) stores interrupt information, including the completion of parasitic capacitance calibration, scan cycle completion, and so on. Register HOSTIRQSRC is cleared after reading. By configuring HOSTIRQEN(Address: 0xF084), you can mask the specified interrupt signal.

I²C INTERFACE

AW96105 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW96105 can support different high level (1.8V~3.3V) of the I²C interface. Additionally, the I²C device supports continuous read and write operations. I²C Register address is 16-bit and register data is 32-bit,transfer of data is big-endian mode.

DEVICE ADDRESS

I²C device address configuration

CS2 Connection	Device Address
Floating	0x12
GND	0x13
VCC	0x14

The I²C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW96105 depends on the CS2 pin status. The default value of I²C device address is 0x12, connecting pad CS2 to GND or VCC will change the device address as showed in table above. Note that when pad CS2 is connected to GND or VCC, it can't be used as sensor pad.

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

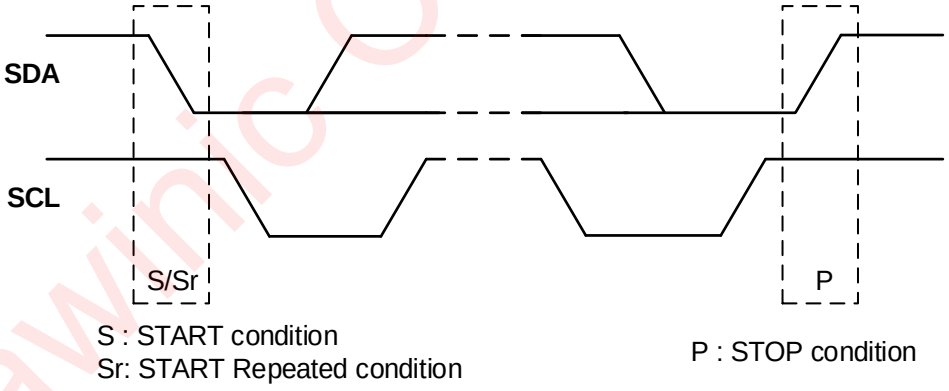


Figure 16 I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

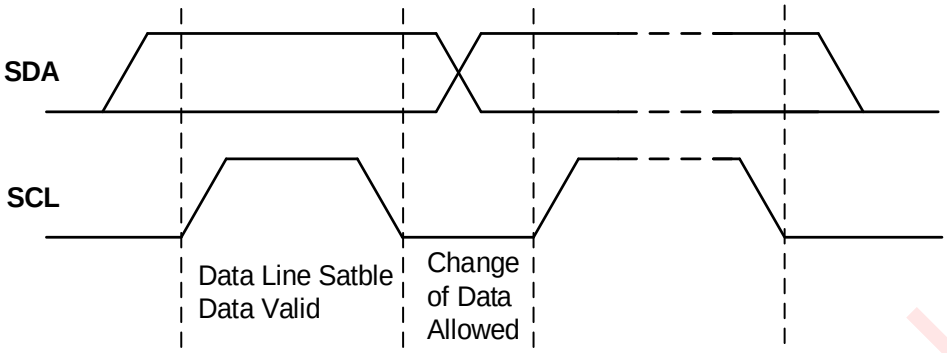


Figure 17 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

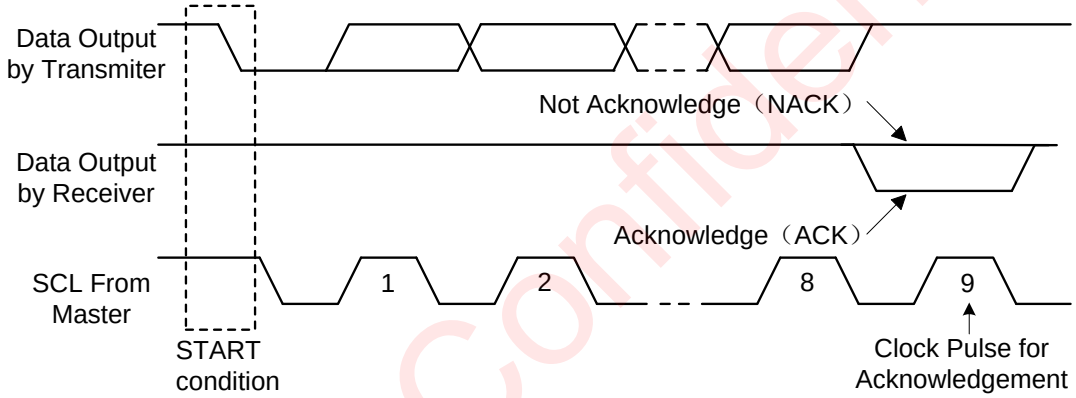


Figure 18 I²C ACK Timing

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing process of I²C is showed as below picture.

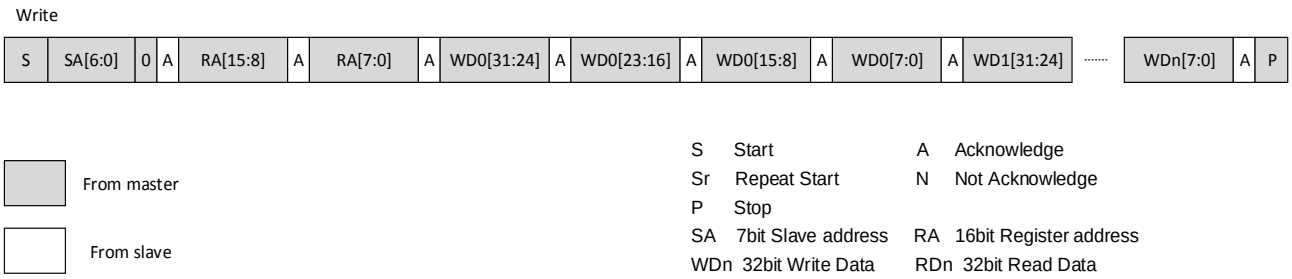


Figure 19 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture.

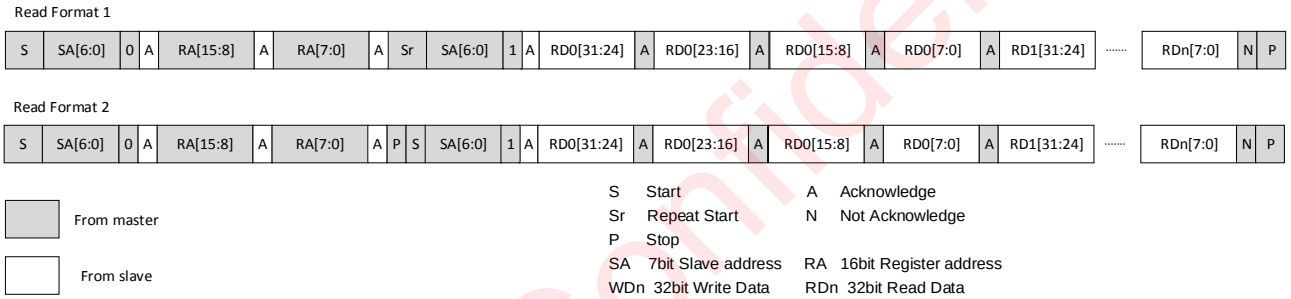


Figure 20 I²C Read Byte Cycle

REGISTER CONFIGURATION

Register List

ADDR	NAME	R/W	Description	Default
0x0000	SCANCTRL0	RW	Scan Control Register 0	0x00000000
0x0004	SCANCTRL1	RW	Scan Control Register 1	0x03F00032
0x000C	TEMPCOMP	RW	Temperature Compensation Register	0x05000000
0x0010	AFECFG0_CH0	RW	AFE Configure Register 0 for CH0	0x00050000
0x0014	AFECFG1_CH0	RW	AFE Configure Register 1 for CH0	0x00000009
0x001C	AFECFG3_CH0	RW	AFE Configure Register 3 for CH0	0xFF000000
0x0020	AFECFG4_CH0	RW	AFE Configure Register 4 for CH0	0x00000000
0x0024	AFECFG0_CH1	RW	AFE Configure Register 0 for CH1	0x00050000
0x0028	AFECFG1_CH1	RW	AFE Configure Register 1 for CH1	0x00000009
0x0030	AFECFG3_CH1	RW	AFE Configure Register 3 for CH1	0xFF000000
0x0034	AFECFG4_CH1	RW	AFE Configure Register 4 for CH1	0x00000000
0x0038	AFECFG0_CH2	RW	AFE Configure Register 0 for CH2	0x00050000
0x003C	AFECFG1_CH2	RW	AFE Configure Register 1 for CH2	0x00000009
0x0044	AFECFG3_CH2	RW	AFE Configure Register 3 for CH2	0xFF000000
0x0048	AFECFG4_CH2	RW	AFE Configure Register 4 for CH2	0x00000000
0x004C	AFECFG0_CH3	RW	AFE Configure Register 0 for CH3	0x00050000
0x0050	AFECFG1_CH3	RW	AFE Configure Register 1 for CH3	0x00000009
0x0058	AFECFG3_CH3	RW	AFE Configure Register 3 for CH3	0xFF000000
0x005C	AFECFG4_CH3	RW	AFE Configure Register 4 for CH3	0x00000000
0x0060	AFECFG0_CH4	RW	AFE Configure Register 0 for CH4	0x00050000
0x0064	AFECFG1_CH4	RW	AFE Configure Register 1 for CH4	0x00000009
0x006C	AFECFG3_CH4	RW	AFE Configure Register 3 for CH4	0xFF000000
0x0070	AFECFG4_CH4	RW	AFE Configure Register 4 for CH4	0x00000000
0x0074	AFECFG0_CH5	RW	AFE Configure Register 0 for CH5	0x00050000
0x0078	AFECFG1_CH5	RW	AFE Configure Register 1 for CH5	0x00000009
0x0080	AFECFG3_CH5	RW	AFE Configure Register 3 for CH5	0xFF000000
0x0084	AFECFG4_CH5	RW	AFE Configure Register 4 for CH5	0x00000000
0x0088	FWVER	RO	Firmware Version Register	0x02001000
0x008C	PST	RO	Program Status Register	0x00000003
0x0090	STAT0	RO	Status Register 0	0x00000000
0x0094	STAT1	RO	Status Register 1	0x00000000
0x0098	STAT2	RO	Status Register 2	0x00000000
0x009C	PROXINTEN	RW	Proximity Interrupt Enable Register	0x3F3F3F3F
0x00A0	FILTREF0_CH0	RW	Filter and Reference Channel Configure Register 0 for CH0	0xE0400000
0x00A4	FILTREF1_CH0	RW	Filter and Reference Channel Configure Register 1 for CH0	0x00000000
0x00A8	BLFILT1_CH0	RW	Baseline Filter 1 Configure Register for CH0	0x000008D2
0x00B0	PROXCTRL_CH0	RW	Proximity Control Register for CH0	0x00000000
0x00B8	PROXTH0_CH0	RW	Proximity Threshold 0 Control Register for CH0	0x00000000
0x00BC	PROXTH1_CH0	RW	Proximity Threshold 1 Control Register for CH0	0x00000000

ADDR	NAME	R/W	Description	Default
0x00C0	PROXTH2_CH0	RW	Proximity Threshold 2 Control Register for CH0	0x00000000
0x00C4	PROXTH3_CH0	RW	Proximity Threshold 3 Control Register for CH0	0x00000000
0x00C8	STDDET_CH0	RW	Steady Detection Configure Register for CH0	0x00000000
0x00CC	INITPROX0_CH0	RW	Start-up Proximity Detection Register 0 for CH0	0x00000000
0x00D0	INITPROX1_CH0	RW	Start-up Proximity Detection Register 1 for CH0	0x00000000
0x00D4	DATAOFFSET_CH0	RW	Data Offset Control Register for CH0	0x00000000
0x00D8	CORRTARDATA_CH0	RW	Target Data Setting for Offset Compensation for CH0	0x00000000
0x00DC	FILTREF0_CH1	RW	Filter and Reference Channel Configure Register 0 for CH1	0xE0400000
0x00E0	FILTREF1_CH1	RW	Filter and Reference Channel Configure Register 1 for CH1	0x00000000
0x00E4	BLFILT1_CH1	RW	Baseline Filter 1 Configure Register for CH1	0x000008D2
0x00EC	PROXCTRL_CH1	RW	Proximity Control Register for CH1	0x00000000
0x00F4	PROXTH0_CH1	RW	Proximity Threshold 0 Control Register for CH1	0x00000000
0x00F8	PROXTH1_CH1	RW	Proximity Threshold 1 Control Register for CH1	0x00000000
0x00FC	PROXTH2_CH1	RW	Proximity Threshold 2 Control Register for CH1	0x00000000
0x0100	PROXTH3_CH1	RW	Proximity Threshold 3 Control Register for CH1	0x00000000
0x0104	STDDET_CH1	RW	Steady Detection Configure Register for CH1	0x00000000
0x0108	INITPROX0_CH1	RW	Start-up Proximity Detection Register 0 for CH1	0x00000000
0x010C	INITPROX1_CH1	RW	Start-up Proximity Detection Register 1 for CH1	0x00000000
0x0110	DATAOFFSET_CH1	RW	Data Offset Control Register for CH1	0x00000000
0x0114	CORRTARDATA_CH1	RW	Target Data Setting for Offset Compensation for CH1	0x00000000
0x0118	FILTREF0_CH2	RW	Filter and Reference Channel Configure Register 0 for CH2	0xE0400000
0x011C	FILTREF1_CH2	RW	Filter and Reference Channel Configure Register 1 for CH2	0x00000000
0x0120	BLFILT1_CH2	RW	Baseline Filter 1 Configure Register for CH2	0x000008D2
0x0128	PROXCTRL_CH2	RW	Proximity Control Register for CH2	0x00000000
0x0130	PROXTH0_CH2	RW	Proximity Threshold 0 Control Register for CH2	0x00000000
0x0134	PROXTH1_CH2	RW	Proximity Threshold 1 Control Register for CH2	0x00000000
0x0138	PROXTH2_CH2	RW	Proximity Threshold 2 Control Register for CH2	0x00000000
0x013C	PROXTH3_CH2	RW	Proximity Threshold 3 Control Register for CH2	0x00000000
0x0140	STDDET_CH2	RW	Steady Detection Configure Register for CH2	0x00000000
0x0144	INITPROX0_CH2	RW	Start-up Proximity Detection Register 0 for CH2	0x00000000
0x0148	INITPROX1_CH2	RW	Start-up Proximity Detection Register 1 for CH2	0x00000000
0x014C	DATAOFFSET_CH2	RW	Data Offset Control Register for CH2	0x00000000

ADDR	NAME	R/W	Description	Default
0x0150	CORRTARDATA_CH2	RW	Target Data Setting for Offset Compensation for CH2	0x00000000
0x0154	FILTREF0_CH3	RW	Filter and Reference Channel Configure Register 0 for CH3	0xE0400000
0x0158	FILTREF1_CH3	RW	Filter and Reference Channel Configure Register 1 for CH3	0x00000000
0x015C	BLFILT1_CH3	RW	Baseline Filter 1 Configure Register for CH3	0x000008D2
0x0164	PROXCTRL_CH3	RW	Proximity Control Register for CH3	0x00000000
0x016C	PROXTH0_CH3	RW	Proximity Threshold 0 Control Register for CH3	0x00000000
0x0170	PROXTH1_CH3	RW	Proximity Threshold 1 Control Register for CH3	0x00000000
0x0174	PROXTH2_CH3	RW	Proximity Threshold 2 Control Register for CH3	0x00000000
0x0178	PROXTH3_CH3	RW	Proximity Threshold 3 Control Register for CH3	0x00000000
0x017C	STDDET_CH3	RW	Steady Detection Configure Register for CH3	0x00000000
0x0180	INITPROX0_CH3	RW	Start-up Proximity Detection Register 0 for CH3	0x00000000
0x0184	INITPROX1_CH3	RW	Start-up Proximity Detection Register 1 for CH3	0x00000000
0x0188	DATAOFFSET_CH3	RW	Data Offset Control Register for CH3	0x00000000
0x018C	CORRTARDATA_CH3	RW	Target Data Setting for Offset Compensation for CH3	0x00000000
0x0190	FILTREF0_CH4	RW	Filter and Reference Channel Configure Register 0 for CH4	0xE0400000
0x0194	FILTREF1_CH4	RW	Filter and Reference Channel Configure Register 1 for CH4	0x00000000
0x0198	BLFILT1_CH4	RW	Baseline Filter 1 Configure Register for CH4	0x000008D2
0x01A0	PROXCTRL_CH4	RW	Proximity Control Register for CH4	0x00000000
0x01A8	PROXTH0_CH4	RW	Proximity Threshold 0 Control Register for CH4	0x00000000
0x01AC	PROXTH1_CH4	RW	Proximity Threshold 1 Control Register for CH4	0x00000000
0x01B0	PROXTH2_CH4	RW	Proximity Threshold 2 Control Register for CH4	0x00000000
0x01B4	PROXTH3_CH4	RW	Proximity Threshold 3 Control Register for CH4	0x00000000
0x01B8	STDDET_CH4	RW	Steady Detection Configure Register for CH4	0x00000000
0x01BC	INITPROX0_CH4	RW	Start-up Proximity Detection Register 0 for CH4	0x00000000
0x01C0	INITPROX1_CH4	RW	Start-up Proximity Detection Register 1 for CH4	0x00000000
0x01C4	DATAOFFSET_CH4	RW	Data Offset Control Register for CH4	0x00000000
0x01C8	CORRTARDATA_CH4	RW	Target Data Setting for Offset Compensation for CH4	0x00000000
0x01CC	FILTREF0_CH5	RW	Filter and Reference Channel Configure Register 0 for CH5	0xE0400000
0x01D0	FILTREF1_CH5	RW	Filter and Reference Channel Configure Register 1 for CH5	0x00000000
0x01D4	BLFILT1_CH5	RW	Baseline Filter 1 Configure Register for CH5	0x000008D2
0x01DC	PROXCTRL_CH5	RW	Proximity Control Register for CH5	0x00000000
0x01E4	PROXTH0_CH5	RW	Proximity Threshold 0 Control Register for CH5	0x00000000

ADDR	NAME	R/W	Description	Default
0x01E8	PROXTH1_CH5	RW	Proximity Threshold 1 Control Register for CH5	0x00000000
0x01EC	PROXTH2_CH5	RW	Proximity Threshold 2 Control Register for CH5	0x00000000
0x01F0	PROXTH3_CH5	RW	Proximity Threshold 3 Control Register for CH5	0x00000000
0x01F4	STDDET_CH5	RW	Steady Detection Configure Register for CH5	0x00000000
0x01F8	INITPROX0_CH5	RW	Start-up Proximity Detection Register 0 for CH5	0x00000000
0x01FC	INITPROX1_CH5	RW	Start-up Proximity Detection Register 1 for CH5	0x00000000
0x0200	DATAOFFSET_CH5	RW	Data Offset Control Register for CH5	0x00000000
0x0204	CORRTARDATA_CH5	RW	Target Data Setting for Offset Compensation for CH5	0x00000000
0x0208	REF1CFG	RW	Reference 1 Configure Register	0x00000005
0x020C	REF2CFG	RW	Reference 2 Configure Register	0x00000005
0x0210	VALID_CH0	RO	Valid Data Register of CH0	0x00000000
0x0214	VALID_CH1	RO	Valid Data Register of CH1	0x00000000
0x0218	VALID_CH2	RO	Valid Data Register of CH2	0x00000000
0x021C	VALID_CH3	RO	Valid Data Register of CH3	0x00000000
0x0220	VALID_CH4	RO	Valid Data Register of CH4	0x00000000
0x0224	VALID_CH5	RO	Valid Data Register of CH5	0x00000000
0x0228	BASELINE_CH0	RO	Baseline Data Register of CH0	0x00000000
0x022C	BASELINE_CH1	RO	Baseline Data Register of CH1	0x00000000
0x0230	BASELINE_CH2	RO	Baseline Data Register of CH2	0x00000000
0x0234	BASELINE_CH3	RO	Baseline Data Register of CH3	0x00000000
0x0238	BASELINE_CH4	RO	Baseline Data Register of CH4	0x00000000
0x023C	BASELINE_CH5	RO	Baseline Data Register of CH5	0x00000000
0x0240	DIFF_CH0	RO	Difference Value Register of CH0	0x00000000
0x0244	DIFF_CH1	RO	Difference Value Register of CH1	0x00000000
0x0248	DIFF_CH2	RO	Difference Value Register of CH2	0x00000000
0x024C	DIFF_CH3	RO	Difference Value Register of CH3	0x00000000
0x0250	DIFF_CH4	RO	Difference Value Register of CH4	0x00000000
0x0254	DIFF_CH5	RO	Difference Value Register of CH5	0x00000000
0x0258	ADCMIN_CH0	RO	ADC Min Data Register of CH0	0x00000000
0x025C	ADCMIN_CH1	RO	ADC Min Data Register of CH1	0x00000000
0x0260	ADCMIN_CH2	RO	ADC Min Data Register of CH2	0x00000000
0x0264	ADCMIN_CH3	RO	ADC Min Data Register of CH3	0x00000000
0x0268	ADCMIN_CH4	RO	ADC Min Data Register of CH4	0x00000000
0x026C	ADCMIN_CH5	RO	ADC Min Data Register of CH5	0x00000000
0x0270	ADCMAX_CH0	RO	ADC Max Data Register of CH0	0x00000000
0x0274	ADCMAX_CH1	RO	ADC Max Data Register of CH1	0x00000000
0x0278	ADCMAX_CH2	RO	ADC Max Data Register of CH2	0x00000000
0x027C	ADCMAX_CH3	RO	ADC Max Data Register of CH3	0x00000000
0x0280	ADCMAX_CH4	RO	ADC Max Data Register of CH4	0x00000000
0x0284	ADCMAX_CH5	RO	ADC Max Data Register of CH5	0x00000000
0x0288	ADCAVG_CH0	RO	ADC Average Data Register of CH0	0x00000000

ADDR	NAME	R/W	Description	Default
0x028C	ADCAVG_CH1	RO	ADC Average Data Register of CH1	0x00000000
0x0290	ADCAVG_CH2	RO	ADC Average Data Register of CH2	0x00000000
0x0294	ADCAVG_CH3	RO	ADC Average Data Register of CH3	0x00000000
0x0298	ADCAVG_CH4	RO	ADC Average Data Register of CH4	0x00000000
0x029C	ADCAVG_CH5	RO	ADC Average Data of CH5	0x00000000
0x02A0	STDMIN_CH0	RO	Steady Min Data Register of CH0	0x00000000
0x02A4	STDMIN_CH1	RO	Steady Min Data Register of CH1	0x00000000
0x02A8	STDMIN_CH2	RO	Steady Min Data Register of CH2	0x00000000
0x02AC	STDMIN_CH3	RO	Steady Min Data Register of CH3	0x00000000
0x02B0	STDMIN_CH4	RO	Steady Min Data Register of CH4	0x00000000
0x02B4	STDMIN_CH5	RO	Steady Min Data Register of CH5	0x00000000
0x02B8	STDMAX_CH0	RO	Steady Max Data Register of CH0	0x00000000
0x02BC	STDMAX_CH1	RO	Steady Max Data Register of CH1	0x00000000
0x02C0	STDMAX_CH2	RO	Steady Max Data Register of CH2	0x00000000
0x02C4	STDMAX_CH3	RO	Steady Max Data Register of CH3	0x00000000
0x02C8	STDMAX_CH4	RO	Steady Max Data Register of CH4	0x00000000
0x02CC	STDMAX_CH5	RO	Steady Max Data Register of CH5	0x00000000
0x02D0	RAW_CH0	RO	Raw Data Register of CH0	0x00000000
0x02D4	RAW_CH1	RO	Raw Data Register of CH1	0x00000000
0x02D8	RAW_CH2	RO	Raw Data Register of CH2	0x00000000
0x02DC	RAW_CH3	RO	Raw Data Register of CH3	0x00000000
0x02E0	RAW_CH4	RO	Raw Data Register of CH4	0x00000000
0x02E4	RAW_CH5	RO	Raw Data Register of CH5	0x00000000
0x02E8	LPF_CH0	RO	LPF Data Register of CH0	0x00000000
0x02EC	LPF_CH1	RO	LPF Data Register of CH1	0x00000000
0x02F0	LPF_CH2	RO	LPF Data Register of CH2	0x00000000
0x02F4	LPF_CH3	RO	LPF Data Register of CH3	0x00000000
0x02F8	LPF_CH4	RO	LPF Data Register of CH4	0x00000000
0x02FC	LPF_CH5	RO	LPF Data Register of CH5	0x00000000
0xF008	CMD	WO	Command Register	0x00000000
0xF080	HOSTIRQSRC	RC	IC To Host Interrupt Source Register	0x00000000
0xF084	HOSTIRQEN	RW	CPU to Host Interrupt Enable Register	0x00000FFF
0xF0F0	I2CADDR	RO	I2C Device Address Register	0x00000012
0xFF00	HOSTCTRL	R/W	Host Control Register	0x00000101
0xFF0C	HOSTCTRL2	R/W	Host Control Register 2	0x01000000
0xFF10	CHIP_ID	RO	CHIP ID Register	0xA9610B00
0xFFF4	ACESS_APB_EN	RO	Host Access APB Peripheral Enable Register	0x0000E39F

Register Detailed Description

SCANCTRL0: Scan Control Register 0 (Address 0000h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:20	Reserved	RO	Reserved	b00

19	WDTEN	RW	Watchdog timer enable. b0: Disable b1: Enable. When the watchdog overflows, the whole chip except IIC will be reset automatically.	b0
18:16	DOZEFACTOR	RW	Scan period in doze mode. T_{scan} (doze) = 2^DOZEFACTOR x T_{scan}(active) Where T_{scan}(active) is scan period in active mode defined by register SCANCTRL1 (Address 0004h).	b000
15:14	Reserved	RO	Reserved	b00
13:8	COMPEN	WC	Defines which channels need auto offset tuning (AOT). And after the offset compensation, the corresponding bit will be cleared to “0”. b0: Doesn't need AOT b1: Need AOT Bit[13:8] = [CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00
5:0	CHEN	RW	Enable the measurement channel. b0: Disable b1: Enable Bit[5:0] = [CH5, CH4, CH3, CH2, CH1, CH0]	b000000

SCANCTRL1: Scan Control Register 1 (Address 0004h)

Bit	Symbol	R/W	Description	Default
31:26	Reserved	RO	Reserved	b000000
25:20	DOZEEN	RO	Doze mode enable. 0: Disable 1: Enable Bit[5:0] = [CH5, CH4, CH3, CH2, CH1, CH0]	h3F
19:16	Reserved	RO	Reserved	b0000
15:11	DOZEDEB	RW	Debounce times setting for entering into doze mode. b00000: Never enter into doze mode Others: In active mode, it none proximity has been detected continuously for 4×DOZEDEB times, the chip will enter into doze mode automatically.	b00000
10:0	SCANPERIOD	RW	Setting basic scan period for active mode: h000: Reserved other: T_{scan}(active) = SCANPERIOD * 2 ms	h032

TEMPCOMP: Temperature Compensation Register (Address 000Ch)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RO	Reserved	b00000
26:24	TEMPCH	RW	Temperature sensor channel selection. b000: CH0 b001: CH1 b010: CH2 b011: CH3 b100: CH4 b101: CH5 other: Reserved	b101
23:22	Reserved	RO	Reserved	b00

21:0	TEMPGAIN	RW	Temperature gain coefficient. TEMPGAIN = S.21 format. RawData=AdcData*(1+ TEMPGAIN *DeltaT) + CAPTEMPCOEF_CHx *TEMPGAIN *DeltaT Where, CAPTEMPCOEF_CHx is defined in register AFECFG3_CHx(Addr: 001Ch), DeltaT is the data corresponding to the temperature change from temperature sensor.	h000000

AFECFG0_CH0: AFE Configure Register 0 for CH0 (Address 0010h)
AFECFG0_CH1: AFE Configure Register 0 for CH1 (Address 0024h)
AFECFG0_CH2: AFE Configure Register 0 for CH2 (Address 0038h)
AFECFG0_CH3: AFE Configure Register 0 for CH3 (Address 004Ch)
AFECFG0_CH4: AFE Configure Register 0 for CH4 (Address 0060h)
AFECFG0_CH5: AFE Configure Register 0 for CH5 (Address 0074h)

Bit	Symbol	R/W	Description	Default
31:30	MEASMOD_CHx	RW	Measurement mode selection of CHx (x = 0, 1, …, 5). b00: Capacitance b10: Temperature other: Reserved	b00
29:26	RDRV_CHx	RW	Driving resistance setting of sensing electrode for CHx. Resistance = 2kΩ * RDRV_CHx	b0000
25:23	RSHLD_CHx	RW	Driving resistance setting of shield electrode for CHx. Resistance = 8kΩ * RSHLD_CHx	b000
22:20	ROFF_CHx	RW	Driving resistance setting of offset capacitance for CHx. b000: 125 Ω b001: 250 Ω b010: 500 Ω b011: 1 kΩ b100: 2 kΩ b101: 4 kΩ b110: 6 kΩ b111: 8 kΩ	b000
19:16	CDCRES_CHx	RW	Capacitance-digital-conversion resolution setting for CHx. Resolution = 15bit + CDCRES_CHx Higher resolution achieves higher SNR, but takes longer measurement time.	b0101
15:12	CRANGE_CHx	RW	Capacitance measurement range of CHx. b0000: 1.1 pF b0001: 2.2 pF b0010: 3.3 pF b0011: 4.4 pF b0100: 6.6 pF b0101: 7.7 pF b0110: 8.8 pF b0111: 9.9 pF b1000: 11 pF b1001: 12.1 pF b1010: 13.2 pF b1011: 14.3 pF b1100: 16.5 pF	b0000

			b1101: 17.6 pF b1110: 18.7 pF b1111: 19.8 pF	
11:10	Reserved	RO	Reserved	h00
9:8	CS4SEL_CHx	RW	CS4 connection setting for CHx. b00: HZ b01: Measured input b10: Shield b11: GND	b00
7:6	CS3SEL_CHx	RW	Same as CS4SEL_CHx for pad CS1.	b00
5:4	CS2SEL_CHx	RW	Same as CS4SEL_CHx for pad CS1.	b00
3:2	CS1SEL_CHx	RW	Same as CS4SEL_CHx for pad CS1.	b00
1:0	CS0SEL_CHx	RW	Same as CS4SEL_CHx for pad CS0.	b00

AFECFG1_CH0: AFE Configure Register 1 for CH0 (Address 0014h)
AFECFG1_CH1: AFE Configure Register 1 for CH1 (Address 0028h)
AFECFG1_CH2: AFE Configure Register 1 for CH2 (Address 003Ch)
AFECFG1_CH3: AFE Configure Register 1 for CH3 (Address 0050h)
AFECFG1_CH4: AFE Configure Register 1 for CH4 (Address 0064h)
AFECFG1_CH5: AFE Configure Register 1 for CH5 (Address 0078h)

Bit	Symbol	R/W	Description	Default
31:16	COFF_CHx	RW	Current offset capacitance setting for CHx (x = 0, 1, …, 5).	h0000
15:8	Reserved	RO	Reserved	b0
7:0	FREQ_CHx	RW	Frequency setting for Cx drive signal of CHx. $F_{smpl} = F_{afe}/(2*FREQ\_CHx+2)/2$ Where F_{afe} = 4MHz.	h09

AFECFG3_CH0: AFE Configure Register 3 for CH0 (Address 001Ch, not open)
AFECFG3_CH1: AFE Configure Register 3 for CH1 (Address 0030h, not open)
AFECFG3_CH2: AFE Configure Register 3 for CH2 (Address 0044h, not open)
AFECFG3_CH3: AFE Configure Register 3 for CH3 (Address 0058h, not open)
AFECFG3_CH4: AFE Configure Register 3 for CH4 (Address 006Ch, not open)
AFECFG3_CH5: AFE Configure Register 3 for CH5 (Address 0080h, not open)

Bit	Symbol	R/W	Description	Default
31:24	Reserved	RO	Reserved	h00
23:16	SCANMULTACT_CHx	RW	Scan period in active mode for CHx. 0: 1x T_{scan}(active) Else: SCANMULTACT x T_{scan}(active)	h00
15	TEMPCOMPEN_CHx	RW	Temperature compensation enable. 0: Disable 1: Enable	b0
14:0	CAPTEMPCOEF_CHx	RW	Linear coefficient for temperature compensation. RawData(temp comp)=AdcData(1+ TEMPGAIN *DeltaT) + CAPTEMPCOEF_CHx *TEMPGAIN *DeltaT Where, TEMPGAIN is defined in register TEMPGAIN(Addr: 000Ch), DeltaT is the data corresponding to the temperature change from temperature sensor.	h0000

AFECFG4_CH0: AFE Configure Register 4 for CH0 (Address 0020h)
AFECFG4_CH1: AFE Configure Register 4 for CH1 (Address 0034h)
AFECFG4_CH2: AFE Configure Register 4 for CH2 (Address 0048h)
AFECFG4_CH3: AFE Configure Register 4 for CH3 (Address 005Ch)

AFECFG4_CH4: AFE Configure Register 4 for CH4 (Address 0070h) AFECFG4_CH5: AFE Configure Register 4 for CH5 (Address 0084h)				
31:25	SCANMULTDOZE	RW	Scan period in dozen mode for CHx. 0: 1x Tscan(doze) Else: SCANMULTACT x Tscan(doze)	h00
24:0	Reserved	RO	Reserved	h000000

FWVER: Firmware Version Register (Address 0088h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	FWVER	RO	The firmware Information.	h02000C00

PST: Program Status Register (Address 008Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	SCANST	RO	Current work mode status. h00: Active mode h01: Doze mode Other: Reserved	h00
23:0	Reserved	RO	Reserved	h000000

STAT0: Status Register 0 (Address 0090h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	Reserved	RO	Reserved	b00
29:24	PROX0ST	RO	Level0 proximity status indication (decision with proximity threshold 0). Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
23:22	Reserved	RO	Reserved	b00
21:16	PROX1ST	RO	Level1 proximity status indication (decision with proximity threshold 1). Bit[21:16]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
15:14	Reserved	RO	Reserved	b00
13:8	PROX2ST	RO	Level2 proximity status indication (decision with proximity threshold 2). Bit[13:8]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00
5:0	PROX3ST	RO	Level3 proximity status indication (decision with proximity threshold 3). Bit[5:0]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000

STAT1: Status Register 1 (Address 0094h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	Reserved	RO	Reserved	b00
29:24	STDST	RO	Steady status indication. Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
23:22	Reserved	RO	Reserved	b00
21:16	COFFERRST	RO	Offset capacitance error status, indicating whether offset capacitance is out of the range defined by COFFMAX and COFFMIN. Bit[21:16]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
15:14	Reserved	RO	Reserved	b00
13:8	COMPST	RO	Indicates whether AOT is being performed Bit[13:8]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
7:6	Reserved	RO	Reserved	b00

5:0	SATST	RO	CDC data saturation status indication. Bit[5:0]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000

STAT2: Status Register 2 (Address 0098h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	Reserved	RW	Reserved	b00
29:24	RPTST	RW	Data report status. Indicates that current DIFF data is bigger than report threshold Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
23:22	Reserved	RO	Reserved	b00
21:16	INITPROXST	RW	Indicates if proximity has being detected when performing start-up offset compensation. Bit[21:16]=[CH5, CH4, CH3, CH2, CH1, CH0]	b000000
15:9	Reserved	RO	Reserved	b00
8	CSNUM	RO	Indicate IC channel number 0:5 channel 1:3 channel	b0
7:5	Reserved	RO	Reserved	b00
4	CONVST	RW	Indicates if any channel is being measured or processed. 0: Idle 1: Data is being measured or processed	b0
3	INITPROXSTANY	RW	Indicates if any INITPROXST is set to 1.	b0
2	ERRSTANY	RW	Indicates if any ERRST is set to 1.	b0
1	STDSTALL	RW	Indicates if all STDST bits are set to 1.	b0
0	PROXSTANY	RW	Indicates if any PROXST is set to 1.	b0

PROXINTEN : Proximity Interrupt Enable (Address 009Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:30	Reserved	RW	Reserved	0
29:24	PROXSTATINTEN	RW	Enable proximity interrupt when diff data > proximity threshold 0:disable 1:enable Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	h3F
23:22	Reserved	RO	Reserved	0
21:16	CLOSEINTEN	RW	Enable the interrupt when channel from far to close. b0: Disable b1: Enable Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	h3F
15:14	Reserved	RO	Reserved	0
13:8	FARINTEN	RO	Enable the interrupt when channel from close to far. b0: Disable b1: Enable Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	h3F
7:6	Reserved	RO	Reserved	0
5:0	SCANOVERINTEN	RW	Enable the interrupt when channel scan over. b0: Disable b1: Enable Bit[29:24]=[CH5, CH4, CH3, CH2, CH1, CH0]	h3F

FILTREF0_CH0: Filter and Reference Channel Configure Register 0 for CH0 (Address 00A0h)
FILTREF0_CH1: Filter and Reference Channel Configure Register 0 for CH1 (Address 00DCh)
FILTREF0_CH2: Filter and Reference Channel Configure Register 0 for CH2 (Address 0118h)
FILTREF0_CH3: Filter and Reference Channel Configure Register 0 for CH3 (Address 0154h)
FILTREF0_CH4: Filter and Reference Channel Configure Register 0 for CH4 (Address 0190h)
FILTREF0_CH5: Filter and Reference Channel Configure Register 0 for CH5 (Address 01CCh)

Bit	Symbol	R/W	Description	Default
31	RAWFILTSEL_CHx	RW	Filter type selection for raw data of CHx (x=0, 1, …, 5). b0: RawFilter1 b1: RawFilter2	b1
30:29	FILT2COEF1_CHx	RW	Coefficient A of RawFilter2 for CHx. b00: 1 (Bypass) b11: 0 (Keep last value) Other: 1/(2^ FILT2COEF1_CHx)	b11
28:27	FILT2COEF2_CHx	RW	Coefficient B of RawFilter2 for CHx. b00: 1 (Bypass) b11: 0 (Keep last value) Other: 1/(2^ FILT2COEF2_CHx)	b00
26:25	SMPLNUM_CHx	RW	The number of sample for CHx. Num = 2^ SMPLNUM_CHx	b00
24:22	LPFCOEF_CHx	RW	Coefficient of the low pass filter for CH0. Coef = 1/(2 ^ LPFCOEF_CHx)	b001
21:20	Reserved	RO	Reserved	b00
19:18	REFSEL_CHx	RW	Reference channel selection for CHx. b00: None b01: Use reference 1 (REFA) only b10: Use reference 2 (REFB) only b11: Use both REFA and REFB	b00
17	REFADIR_CHx	RW	Defines the correction direction of REFA for CHx. b0: Positive correct b1: Negative correct	b0
16	REFBDIR_CHx	RW	Defines the correction direction of REFB for CHx. b0: Positive correct b1: Negative correct	b0
15:8	REFAUPCOEF_CHx	RW	The coefficient of REFA for Positive correct to CHx. RefACoef = XXX.YYYYY (unsigned, format 3.5)	h00
7:0	REFBUPCOEF_CHx	RW	The coefficient of REFB for Positive correct to CHx. RefBCoef = XXX.YYYYY (unsigned, format 3.5)	h00

FILTREF1_CH0: Filter and Reference Channel Configure Register 1 for CH0 (Address 00A4h)
FILTREF1_CH1: Filter and Reference Channel Configure Register 1 for CH1 (Address 00E0h)
FILTREF1_CH2: Filter and Reference Channel Configure Register 1 for CH2 (Address 011Ch)
FILTREF1_CH3: Filter and Reference Channel Configure Register 1 for CH3 (Address 0158h)
FILTREF1_CH4: Filter and Reference Channel Configure Register 1 for CH4 (Address 0194h)
FILTREF1_CH5: Filter and Reference Channel Configure Register 1 for CH5 (Address 01E0h)

Bit	Symbol	R/W	Description	Default
31:24	REFADOWNCOEF_CHx	RW	The coefficient of REFA for Negative correct to CHx. Ref1Coef = XXX.YYYYY (unsigned, format 3.5)	h00

23:16	REFBDOWNCOEF_CHx	RW	The coefficient of REFB for Negative correct to CHx. Ref2Coef = XXX.YYYYY (unsigned, format 3.5)	h00
15:8	RELEASETOUCHCNT_CHx	RW	Defines the times proximity state has been continuous detected before release proximity state 00: Disable Others: 4* RELEASETOUCHCNT times	h00
7:4	BASERSTCNT_CHx	RW	Defines the times diff data < negative proximity threshold before reset baseline. 00: Disable Others: BASERSTCNT times	h00
3:2	VALIDSATDOWNEN_CHx	RW	Valid data negative saturation detect enable 0:disable 1:enable	b00
1:0	VALIDSATDOWNTH_CHx	RW	Valid data negative saturation threshold b00：- 0x09A000 b01：- 0x0BA000 b10：- 0x0DA000 b11：- 0x0EF000	b00

BLFILT1_CH0: Baseline Filter 1 Configure Register for CH0 (Address 00A8h)
BLFILT1_CH1: Baseline Filter 1 Configure Register for CH1 (Address 00E4h)
BLFILT1_CH2: Baseline Filter 1 Configure Register for CH2 (Address 0120h)
BLFILT1_CH3: Baseline Filter 1 Configure Register for CH3 (Address 015Ch)
BLFILT1_CH4: Baseline Filter 1 Configure Register for CH4 (Address 0190h)
BLFILT1_CH5: Baseline Filter 1 Configure Register for CH5 (Address 01D4h)

Bit	Symbol	R/W	Description	Default
31:30	SATJUDG_CHx	RW	Positive saturation judgment and process method setting for CHx (x=0, 1, …, 5). b00: Disable saturation judgment for VALID data b01: Only judge saturation status b10: Enable the saturation judgment, and when saturation detected, capacitance offset compensation will be performed automatically. b11: Reserved	b00
29:28	SATUPTH_CHx	RW	Positive saturation threshold of CHx. b00：0x09A000 b01：0x0BA000 b10：0x0DA000 b11：0x0EF000	b00
27:26	SATDEB_CHx	RW	The debouncer applied to set the saturation status for CHx. Deb = 2^ VALIDSATDEB	b00
25	BLERRACT_CHx	RW	The action when baseline error occurs of CHx. 0: Trig all channels to perform offset compensation 1: Only trig current channel to perform offset compensation	b0
24:19	BLMAX_CHx	RW	Defines the max threshold of baseline that will trig offset compensation for CHx. 0: Disable baseline up threshold judge Other: Max threshold = (BLMAX_CHx << 14)	h00

18:13	BLMIN_CHx	RW	Defines the min threshold of baseline that will trig offset compensation for CHx. Min threshold = -(BLMIN_CHx << 14)	h00
12:11	BLERRDEB_CHx	RW	The debouncer applied to baseline error judgment. Deb = (2^ BLERRDEB_CHx)	b01
10:9	BLTSDOZE_CHx	RW	Baseline tracing speed factor in doze mode for CHx. When the baseline upward tracing: Factor = (2^BLTSDOZE_CHx)*BLFUPCOEF_CHx Other: Factor=(2^BLTSDOZE_CHx)*BLFDOWNCOEF_CHx	b00
8:5	BLFUPCOEF_CHx	RW	Coefficient of baseline upward tracing for CHx. b0000: 1 (Baseline = Valid) b1111: 0 (Baseline frozen, keep last value) Other: Coef = (2^ BLFUPCOEF_CHx)	h6
4:2	BLFDOWNCOEF_CHx	RW	Coefficient of baseline downward tracing for CHx. b000: 1 (Baseline = Valid) b111: 0 (Baseline frozen, keep last value) Other: Coef = (2^ BLFDOWNCOEF_CHx)	h4
1	BLFRZEN_CHx	RW	Defines whether the baseline is frozen when proximity is detected for CHx. b0: Baseline keeps frozen for 4* BLABNORMALDEB times when proximity is detected, and then tracing the VALID data. b1: Baseline keeps frozen all the time when proximity is detected. BLFRZEN_CHx just used in filter BLFILT1. Usually, BLFRZEN_CHx = 0 is used when FARCOND = 1.	b1
0	BLFILTSEL_CHx	RW	Baseline filter selection for CH0. b0: Baseline filter 1 (BLFilt1) b1: Baseline filter 2 (BLFilt2)	b0

PROXCTRL0_SS0: Proximity Control Register for SS0 (Address 00B0h)
PROXCTRL0_SS1: Proximity Control Register for SS1 (Address 00ECh)
PROXCTRL0_SS2: Proximity Control Register for SS2 (Address 0128h)
PROXCTRL0_SS3: Proximity Control Register for SS3 (Address 0164h)
PROXCTRL0_SS4: Proximity Control Register for SS4 (Address 0198h)
PROXCTRL0_SS5: Proximity Control Register for SS5 (Address 01DCh)

Bit	Symbol	R/W	Description	Default
31:14	Reserved	RO	Reserved	b0000
13:12	THHYST_CHx	RW	Defines the hysteresis of REPORTTH/PROXTH0 /PROXTH1/PROXTH2/PROXTH3/STEADYTH for CH0. 00: Hyst = 0 01: Hyst = Th/16 10: Hyst = Th/8 11: Hyst = Th/4	b00

11:10	INDEB	RW	The debouncer applied to enter into report/proximity status for CHx. Deb = (2^ INDEB)	b00
9:8	OUTDEB	RW	The debouncer applied to exit report/proximity status for CHx. Deb = (2^ OUTDEB)	b00
7:0	Reserved	RO	Reserved	h00

PROXTH0_CH0: Proximity Threshold 0 Control Register for CH0 (Address 00B8h)
PROXTH0_CH1: Proximity Threshold 0 Control Register for CH1 (Address 00F4h)
PROXTH0_CH2: Proximity Threshold 0 Control Register for CH2 (Address 0130h)
PROXTH0_CH3: Proximity Threshold 0 Control Register for CH3 (Address 016Ch)
PROXTH0_CH4: Proximity Threshold 0 Control Register for CH4 (Address 01A8h)
PROXTH0_CH5: Proximity Threshold 0 Control Register for CH5 (Address 01E4h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h00
20:0	PROXTH0_CHx	RW	Defines the proximity threshold 0 of CHx: Th0 = PROXTH0	h00

PROXTH1_CH0: Proximity Threshold 1 Control Register for CH0 (Address 00BCh)
PROXTH1_CH1: Proximity Threshold 1 Control Register for CH1 (Address 00F8h)
PROXTH1_CH2: Proximity Threshold 1 Control Register for CH2 (Address 0134h)
PROXTH1_CH3: Proximity Threshold 1 Control Register for CH3 (Address 0170h)
PROXTH1_CH4: Proximity Threshold 1 Control Register for CH4 (Address 01ACh)
PROXTH1_CH5: Proximity Threshold 1 Control Register for CH5 (Address 01E8h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h00
20:0	PROXTH1_CHx	RW	Defines the proximity threshold 1 of CHx: Th1 = PROXTH1	h00

PROXTH2_CH0: Proximity Threshold 2 Control Register for CH0 (Address 00C0h)
PROXTH2_CH1: Proximity Threshold 2 Control Register for CH1 (Address 00FCh)
PROXTH2_CH2: Proximity Threshold 2 Control Register for CH2 (Address 0138h)
PROXTH2_CH3: Proximity Threshold 2 Control Register for CH3 (Address 0174h)
PROXTH2_CH4: Proximity Threshold 2 Control Register for CH4 (Address 01B0h)
PROXTH2_CH5: Proximity Threshold 2 Control Register for CH5 (Address 01ECh)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h00
20:0	PROXTH2_CHx	RW	Defines the proximity threshold 2 of CHx: Th2 = PROXTH2	h00

PROXTH3_CH0: Proximity Threshold 3 Control Register for CH0 (Address 00C4h)
PROXTH3_CH1: Proximity Threshold 3 Control Register for CH1 (Address 0100h)
PROXTH3_CH2: Proximity Threshold 3 Control Register for CH2 (Address 013Ch)
PROXTH3_CH3: Proximity Threshold 3 Control Register for CH3 (Address 0178h)
PROXTH3_CH4: Proximity Threshold 3 Control Register for CH4 (Address 01B4h)
PROXTH3_CH5: Proximity Threshold 3 Control Register for CH5 (Address 01F0h)

Bit	Symbol	R/W	Description	Default
31:21	Reserved	RO	Reserved	h00
20:0	PROXTH3_CHx	RW	Defines the proximity threshold 3 of CHx: Th3 = PROXTH3	h00

STDDET_CH0: Steady Detection Configure Register for CH0 (Address 00C8h)
STDDET_CH1: Steady Detection Configure Register for CH1 (Address 0104h)
STDDET_CH2: Steady Detection Configure Register for CH2 (Address 0140h)
STDDET_CH3: Steady Detection Configure Register for CH3 (Address 017Ch)
STDDET_CH4: Steady Detection Configure Register for CH4 (Address 01B8h)
STDDET_CH5: Steady Detection Configure Register for CH5 (Address 01F4h)

Bit	Symbol	R/W	Description	Default
31:16	STDTH_CHx	RW	The steady threshold for CHx. Th = STDTH_CHx * (2^STDTHMUL_CHx)	b0000
15:14	STDTHMUL_CHx	RW	Steady threshold multiply factor:	b00
13:11	STDSAMPLES_CHx	RW	The number of data to be compared with steady threshold for CHx. Samples = (2^(STDSAMPLES_CHx +1))	b000
10:9	STDJUDGEEN_CHx	RW	Data selection and steady check for CHx. b00: Disable data steady judge b01: Use ADCAVG as judgment data b10: Use VALID as judgment data b11: Use DIFF as judgment data Note: Judge data steady or not only when proximity is detected.	b00
9:2	STDINDEB_CHx	RW	The debouncer applied to enter steady status for CHx. Deb = STDINDEB_CHx	h00
1:0	STDOUTDEB_CHx	RW	The debouncer applied to exit steady status for CHx. Deb = (2^ STEADYOUTDEB_CHx)	b00

INITPROX0_CH0: Start-up Proximity Detection Register 0 for CH0 (Address 00CCh)
INITPROX0_CH1: Start-up Proximity Detection Register 0 for CH1 (Address 0108h)
INITPROX0_CH2: Start-up Proximity Detection Register 0 for CH2 (Address 0144h)
INITPROX0_CH3: Start-up Proximity Detection Register 0 for CH3 (Address 0180h)
INITPROX0_CH4: Start-up Proximity Detection Register 0 for CH4 (Address 01BCh)
INITPROX0_CH5: Start-up Proximity Detection Register 0 for CH5 (Address 01F8h)

Bit	Symbol	R/W	Description	Default
31:16	INITVALIDTH_CHx	RW	The initial valid threshold for start-up proximity detection for CHx. Th = (INITVALIDTH_CHx << 5) Signed value (2's complement)	h0000
15:0	INITCOFF_CHx	RW	The default value of offset compensation for CHx. if INITCOFF_CHx = 16'h0 ,disable start up proximity detect.	h0000

INITPROX1_CH0: Start-up Proximity Detection Register 1 for CH0 (Address 00D0)h)
INITPROX1_CH1: Start-up Proximity Detection Register 1 for CH1 (Address 010Ch)
INITPROX1_CH2: Start-up Proximity Detection Register 1 for CH2 (Address 0148h)
INITPROX1_CH3: Start-up Proximity Detection Register 1 for CH3 (Address 0184h)
INITPROX1_CH4: Start-up Proximity Detection Register 1 for CH4 (Address 01C0h)
INITPROX1_CH5: Start-up Proximity Detection Register 1 for CH5 (Address 01FCh)

Bit	Symbol	R/W	Description	Default

31	INITPROXMD_CHx	RW	Control whether performing start-up proximity detection during start up offset compensation or not. 0: not perform 1: perform	0
30:27	Reserved	RO	Reserved	h0
26:24	REFCOEFMULTS_CHx	RW	The factor applied to REF1STRENGTH_CHx and REF1STRENGTH_CHx for CHx. Factor = (2^ REFCOEFMULTS)	h0
23:17	Reserved	RO	Reserved	h00
16	COFFERREN_CHx	RW	Defines whether to set proximity status when offset compensation error detected for CHx. b0: Disable 1: Setting proximity status when error detected.	b0
15:8	COFFHTH_CHx	RW	The high threshold of capacitance offset compensation for CHx. h00: Disable error judgment for high threshold Other: Th = COFFHTH_CHx *128	h00
7:0	COFFLTH_CHx	RW	Defines the low threshold of parasitic capacitance for CHx. h00: Disable low parasitic error judge Other: Th = COFFLTH_CHx *128	h00

DATAOFFSET_CH0: Data Offset Control Register for CH0(Address 00D4h)
DATAOFFSET_CH1: Data Offset Control Register for CH1(Address 0110h)
DATAOFFSET_CH2: Data Offset Control Register for CH2(Address 014Ch)
DATAOFFSET_CH3: Data Offset Control Register for CH3(Address 0188h)
DATAOFFSET_CH4: Data Offset Control Register for CH4(Address 01C4h)
DATAOFFSET_CH5: Data Offset Control Register for CH5(Address 0200h)

Bit	Symbol	R/W	Description	Default
31:22	Reserved	RO	Reserved	h0
21:0	RAWOFFSETDATA	RW	Defines Raw data's offset value. Signed value (2's complement)	h0000

CORRTARDATA_CH0: Target Data Setting for Offset Compensation for CH0(Address 00D8h)
CORRTARDATA_CH1: Target Data Setting for Offset Compensation for CH0(Address 0114h)
CORRTARDATA_CH2: Target Data Setting for Offset Compensation for CH0(Address 0150h)
CORRTARDATA_CH3: Target Data Setting for Offset Compensation for CH0(Address 018Ch)
CORRTARDATA_CH4: Target Data Setting for Offset Compensation for CH0(Address 01C8h)
CORRTARDATA_CH5: Target Data Setting for Offset Compensation for CH0(Address 0204h)

Bit	Symbol	R/W	Description	Default
31:22	Reserved	RO	Reserved	h0
21:0	CORRTARDATA	RW	Defines target value when offset compensation. Signed value (2's complement)	h0000

REFACFG: Reference A Configure Register (Address 0208h)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RO	Reserved	b00000
26	REFAEN	RW	Reference 1 (REFA) enable. b0: Disable b1: Enable	b0
25:4	REFAINIT	RW	The initial value of REFA Signed value (2's complement)	h000

3	REFAINITSEL	RW	Initial value selection of REFA for calculating the variation data. b0: REFAINIT b1: Valid data of REF1 after offset compensation	b0
2:0	REFASEL	RW	Defines which channel is used as REFA. b000: CH0 b001: CH1 b010: CH2 b011: CH3 b100: CH4 b101: CH5 Other: Reserved	b101

REFBCFG: Reference B Configure Register (Address 020Ch)

Bit	Symbol	R/W	Description	Default
31:27	Reserved	RW	Reserved	b00000
26	REFBEN	RW	Reference 1 (REFB) enable. b0: Disable b1: Enable	b0
25:4	REFBINIT	RW	The initial value of REFB Signed value (2's complement)	h000
3	REFBINITSEL	RW	Initial value selection of REFA for calculating the variation data. b0: RefBInit b1: Valid data of REF1 after offset compensation	b0
2:0	REFBSEL	RW	Defines which channel is used as REFB. b000: CH0 b001: CH1 b010: CH2 b011: CH3 b100: CH4 b101: CH5 Other: Reserved	h101

VALID_CH0: Valid Data Register of CH0 (Address 0210h)
VALID_CH1: Valid Data Register of CH1 (Address 0214h)
VALID_CH2: Valid Data Register of CH2 (Address 0218h)
VALID_CH3: Valid Data Register of CH3 (Address 021Ch)
VALID_CH4: Valid Data Register of CH4 (Address 0220h)
VALID_CH5: Valid Data Register of CH5 (Address 0224h)

Bit	Symbol	R/W	Description	Default
31:0	VALID_CHx	RO	Current valid value (VALID) of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

BASELINE_CH0: Baseline Data Register of CH0 (Address 0228h)
BASELINE_CH1: Baseline Data Register of CH1 (Address 022Ch)
BASELINE_CH2: Baseline Data Register of CH2 (Address 0230h)
BASELINE_CH3: Baseline Data Register of CH3 (Address 0234h)
BASELINE_CH4: Baseline Data Register of CH4 (Address 0238h)
BASELINE_CH5: Baseline Data Register of CH5 (Address 023Ch)

Bit	Symbol	R/W	Description	Default
31:0	BASELINE_CHx	RO	Current baseline value (BASELINE) of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

DIFF_CH0: Difference Value Register of CH0 (Address 0240h)

DIFF_CH1: Difference Value Register of CH1 (Address 0244h)
DIFF_CH2: Difference Value Register of CH2 (Address 0248h)
DIFF_CH3: Difference Value Register of CH3 (Address 024Ch)
DIFF_CH4: Difference Value Register of CH4 (Address 0250h)
DIFF_CH5: Difference Value Register of CH5 (Address 0254h)

Bit	Symbol	R/W	Description	Default
31:0	DIFF_CHx	RO	Current different value (DIFF) of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

ADCMIN_CH0: ADC Min Data Register of CH0 (Address 0258h)
ADCMIN_CH1: ADC Min Data Register of CH1 (Address 025Ch)
ADCMIN_CH2: ADC Min Data Register of CH2 (Address 0260h)
ADCMIN_CH3: ADC Min Data Register of CH3 (Address 0264h)
ADCMIN_CH4: ADC Min Data Register of CH4 (Address 0268h)
ADCMIN_CH5: ADC Min Data Register of CH5 (Address 026Ch)

Bit	Symbol	R/W	Description	Default
31:0	ADCMIN_CHx	RO	Current ADC min value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

ADCMAX_CH0: ADC Max Data Register of CH0 (Address 0270h)
ADCMAX_CH1: ADC Max Data Register of CH1 (Address 0274h)
ADCMAX_CH2: ADC Max Data Register of CH2 (Address 0278h)
ADCMAX_CH3: ADC Max Data Register of CH3 (Address 027Ch)
ADCMAX_CH4: ADC Max Data Register of CH4 (Address 0280h)
ADCMAX_CH5: ADC Max Data Register of CH5 (Address 0284h)

Bit	Symbol	R/W	Description	Default
31:0	ADCMAX_CHx	RO	Current ADC max value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

ADCAVG_CH0: ADC Average Data of CH0 (Address 0288h)
ADCAVG_CH1: ADC Average Data of CH1 (Address 028Ch)
ADCAVG_CH2: ADC Average Data of CH2 (Address 0290h)
ADCAVG_CH3: ADC Average Data of CH3 (Address 0294h)
ADCAVG_CH4: ADC Average Data of CH4 (Address 0298h)
ADCAVG_CH5: ADC Average Data of CH5 (Address 029Ch)

Bit	Symbol	R/W	Description	Default
31:0	ADCAVG_CHx	RO	Current ADC average value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

STDMIN_CH0: Steady Min Data of CH0 (Address 02A0h)
STDMIN_CH1: Steady Min Data of CH1 (Address 02A4h)
STDMIN_CH2: Steady Min Data of CH2 (Address 02A8h)
STDMIN_CH3: Steady Min Data of CH3 (Address 02ACh)
STDMIN_CH4: Steady Min Data of CH4 (Address 02B0h)
STDMIN_CH5: Steady Min Data of CH5 (Address 02B4h)

Bit	Symbol	R/W	Description	Default
31:0	STDMIN_CHx	RO	Current steady min value of CHx. Signed value (2's complement, S21.10 format)	h00000000

			[31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	

STDMAX_CH0: Steady Maximum Data of CH0 (Address 02B8h) STDMAX_CH1: Steady Maximum Data of CH1 (Address 02BCh) STDMAX_CH2: Steady Maximum Data of CH2 (Address 02C0h) STDMAX_CH3: Steady Maximum Data of CH3 (Address 02C4h) STDMAX_CH4: Steady Maximum Data of CH4 (Address 02C8h) STDMAX_CH5: Steady Maximum Data of CH5 (Address 02CCh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	STDMAX_CHx	RO	Current steady max value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

RAW_CH0: Raw Data Register of CH0 (Address 02D0h) RAW_CH1: Raw Data Register of CH1 (Address 02D4h) RAW_CH2: Raw Data Register of CH2 (Address 02D8h) RAW_CH3: Raw Data Register of CH3 (Address 02DCh) RAW_CH4: Raw Data Register of CH4 (Address 02E0h) RAW_CH5: Raw Data Register of CH5 (Address 02E4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	RAW_CHx	RO	Current Raw value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

LPF_CH0: LPF Data of CH0 (Address 02E8h) LPF_CH1: LPF Data of CH1 (Address 02ECh) LPF_CH2: LPF Data of CH2 (Address 02F0h) LPF_CH3: LPF Data of CH3 (Address 02F4h) LPF_CH4: LPF Data of CH4 (Address 02F8h) LPF_CH5: LPF Data of CH5 (Address 02FCh)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	LPF_CHx	RO	Current LPF value of CHx. Signed value (2's complement, S21.10 format) [31:0]=XXXXXXXXXXXXXXXXXXXX.YYYYYYYYYY	h00000000

CMD: Command Register (Address F008h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:8	Reserved	RO	Reserved	h000000
7:0	CMD	WO	h00: Reserved h01: IC will enter active mode and start detection Other: IC will enter sleep mode when current scan period finish	h00

HOSTIRQSRC: Host Interrupt Source Register (Address F080h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:20	Reserved	RO	Reserved	h000000
19	GPIOIRQ	RC	GPIO Interrupt Source Status	b0

18	WDTIRQ	RC	WDT Interrupt Source Status	b0
17	TIMERIRQ	RC	TIMER Interrupt Source Status	b0
16	AFEIRQ	RC	AFE Interrupt Source Status	b0
15:12	Reserved	RO	Reserved	b0000
11	INITPROXIRQ	RW	Indicates if any of INITPROXST is set to 1. b0: All channels don't detect start-up proximity b1: At least one channel detects start-up proximity	b0
10	COFFERRIRQ	RW	Indicates if any of COFFERRST is set to 1. b0: All channel don't detect capacitance offset error b1: At least one channel detect parasitic capacitance error	b0
9	WDTOFIRQ	RW	Indicates if the WDT overflows. b0: Invalid b1: The WDT overflows	b0
8	CMDOVERIRQ	RW	Indicates if current command is executed over. b0: Invalid b1: Current command is executed over	b0
7	SATIRQ	RW	Indicates if any of SATST is set to 1. b0: All channels don't detect valid data saturation b1: At least one channel detect valid data saturation	b0
6	PROXSTATIRQ	RW	Indicates if any of PROXST is set to 1. b0: All channels don't detect proximity b1: At least one channel detect proximity	b0
5	RPTSTATIRQ	RW	Indicates if any of REPORTST is set to 1. b0: All channels don't detect DIFF data bigger than report threshold b1: At least one channel detect DIFF data bigger than report threshold	b0
4	CONVOVERIRQ	RW	Indicates if the data conversion over. b0: Scan conversion doesn't over b1: Scan conversion over	b0
3	CALDONEIRQ	RW	Indicates if parasitic capacitance compensation over. b0: Invalid b1: Offset compensation over	b0
2	FARANYIRQ	RW	Indicates if any channel from close to far. b0: Invalid b1: At least one channel from close to far	b0
1	CLOSEANYIRQ	RW	Indicates if any channel from far to close. b0: Invalid b1: At least one channel from far to close	b0
0	INITOVERIRQ	RW	Indicates if the chip initial over. b0: Invalid b1: The chip initial over	b0

HOSTIRQEN: Host Interrupt Enable Register (Address F084h)

Bit	Symbol	R/W	Description	Default
31:20	Reserved	RO	Reserved	b0

19	GPIOIRQEN	RW	GPIO Interrupt Enable b0: Disable b1: Enable	b0
18	WDTIRQEN	RW	WDT Interrupt Enable b0: Disable b1: Enable	b0
17	TIMERIRQEN	RW	TIMER Interrupt Enable b0: Disable b1: Enable	b0
16	AFEIRQEN	RW	AFE Interrupt Enable b0: Disable b1: Enable	b0
15:12	Reserved	RO	Reserved	b0
11	STARTPROXEN	RW	Enable start-up proximity interrupt (any). b0: Disable b1: Enable	b1
10	ERRSTATEN	RW	Enable parasitic capacitance error interrupt (any). b0: Disable b1: Enable	b1
9	WDTOFEN	RW	Enable WDT overflow interrupt. b0: Disable b1: Enable	b1
8	CMDOVEREN	RW	Enable current command executing over interrupt. b0: Disable b1: Enable	b1
7	SATSTATEN	RW	Enable the VALID data saturation interrupt (any). b0: Disable b1: Enable	b1
6	PROXSTATANYEN	RW	Enable proximity interrupt (any). b0: Disable b1: Enable	b1
5	REPORTSTATEN	RW	Enable report interrupt (any). b0: Disable b1: Enable	b1
4	CONVOVEREN	RW	Enable data conversion over interrupt. b0: Disable b1: Enable	b1
3	CALDONEEN	RW	Enable parasitic capacitance compensation over interrupt. b0: Disable b1: Enable	b1
2	FARANYEN	RW	Enable the interrupt when any channel from close to far. b0: Disable b1: Enable	b1
1	CLOSEANYEN	RW	Enable the interrupt when any channel from far to close. b0: Disable b1: Enable	b1
0	INITOVEREN	RW	Enable chip initial over interrupt. b0: Disable b1: Enable	b1

I2CADDR: I2C Address Register (Address F0F0h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:7	Reserved	RO	Reserved	h0000000
6:0	I2CADDR	RO	I2C device address.	b0100010

HOSTCTRL1: Clock Control Register (Address FF00h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:10	RESERVED	RO	Reserved	0
9	CPU_SLEEPING	RO	CPU deep sleep status indication. b0: Not in deep sleep mode b1: In deep sleep mode	b0
8	OSC_EN	RO	OSC status indication. b0: The OSC is turned off b1: The OSC is turned on	b1
7:1	RESERVED	RO	Reserved	0
0	HOST_OSC_EN	R/W	Enable OSC. b0: Turn off the OSC b1: Turn on the OSC	b1

HOSTCTRL2: HOST Control Register 2 (Address FF0Ch)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	SA_RSTNALL	W	Write “0” to reset the whole chip.	1
23	RESERVED	RO	Reserved	0
22	HOST_CLKEN_CPU	R/W	CPU clock Enable bit , write “1” to keep CPU clock running	0
21:0	RESERVED	RO	Reserved	0

CHIP_ID: CHIP ID Register(Address FF10h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:0	CHIP_ID	RO	CHIP ID of IC	hA9610B00

ACESS_APB_EN: Host Access APB Peripheral Enable Register (Address FFF4h)				
Bit	**Symbol**	**R/W**	**Description**	**Default**
31:24	WPRT_APB_EN	RW	Write protect byte of APB_ACCESS_EN register, password is 0x3C	h00
23:1	Reserved	RO	Reserved	h71CF
0	SRAM_EN	RW	HOST access SRAM enable 0：read only 1：enable both write and read	b1

APPLICATION INFORMATION

Inductor Selection

The recommended values of the Inductance L1~L5, which were applied in CS0~CS4 pins, respectively, are all 220nH.

Capacitors Selection

The recommended value of the capacitance C1 is 1μF and C2 is 0.1μF.

Resistor Selection

The recommended values of the resistor R1~R3 , which were applied in SCL,SDA and INTN pins, are 4.7kΩ.
The recommended values of the resistor R4~R8 , which were applied in CS0~CS4 pins, are 1kΩ.

RECOMMENDED COMPONENTS LIST

Component	Name	DESCRIPTION	TYP.	UNIT
L	L1,L2,L3,L4,L5	0402 package,20% resolution	220	nH
C	C1	0402 package,10% resolution	1	μF
	C2	0402 package,10% resolution	0.1	μF
R	R1,R2,R3	0402 package, 5% resolution	4.7	kΩ
	R4,R5,R6,R7,R8	0402 package, 5% resolution	1	kΩ

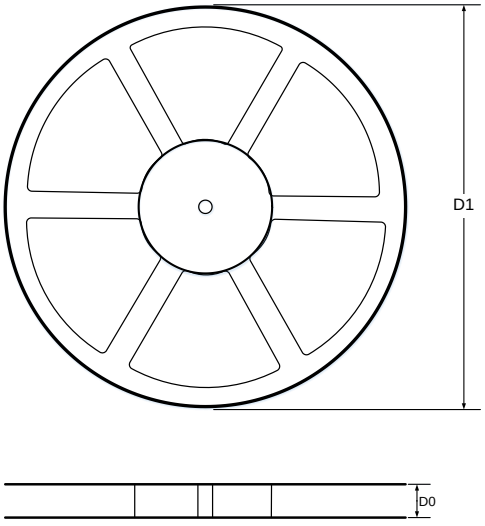
PCB LAYOUT CONSIDERATION

AW96105 is a 5-channel capacitive touch and proximity controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

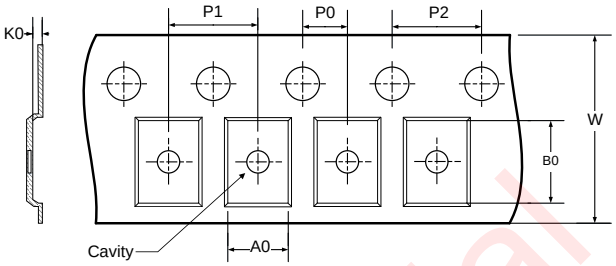
1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC. Avoid connecting peripheral devices and chip pins with two different layers of copper, use the same layer of copper instead.
2. Place the chip close to capacitive sensor and make trace as short as possible.
3. Make sure the sensor and traces be away from mic, earphone line. because capacitive sensor will disturb audio line.
4. Place reference channel along with sensor channel to get better performance.
5. Please using low noise power supply for SAR sensor.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

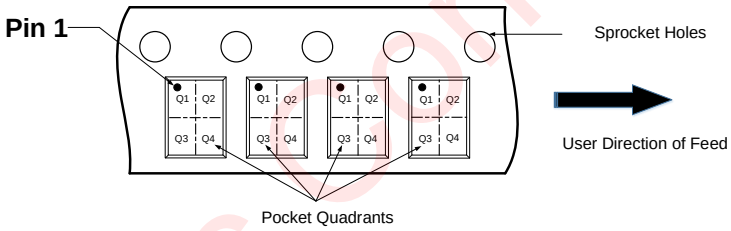


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

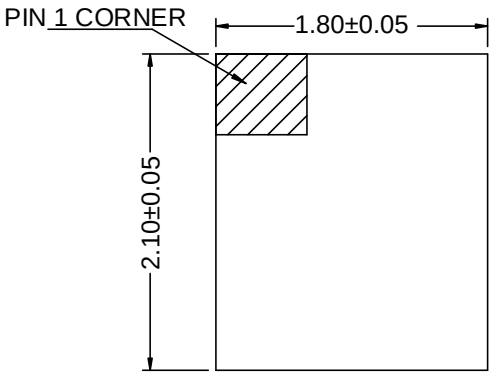


DIMENSIONS AND PIN1 ORIENTATION

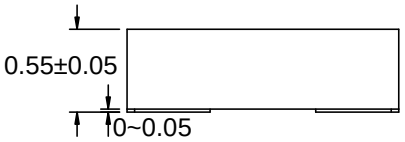
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2	2.3	0.75	2	4	4	8	Q1

All dimensions are nominal

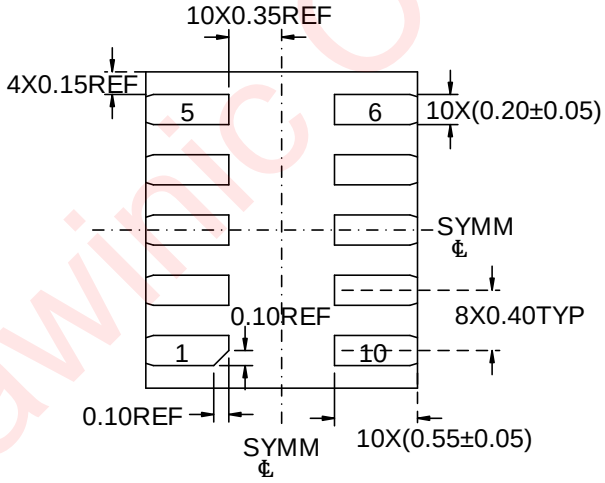
PACKAGE DESCRIPTION



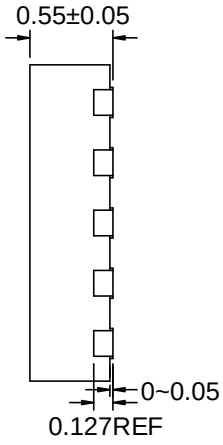
TOP VIEW



SIDE VIEW



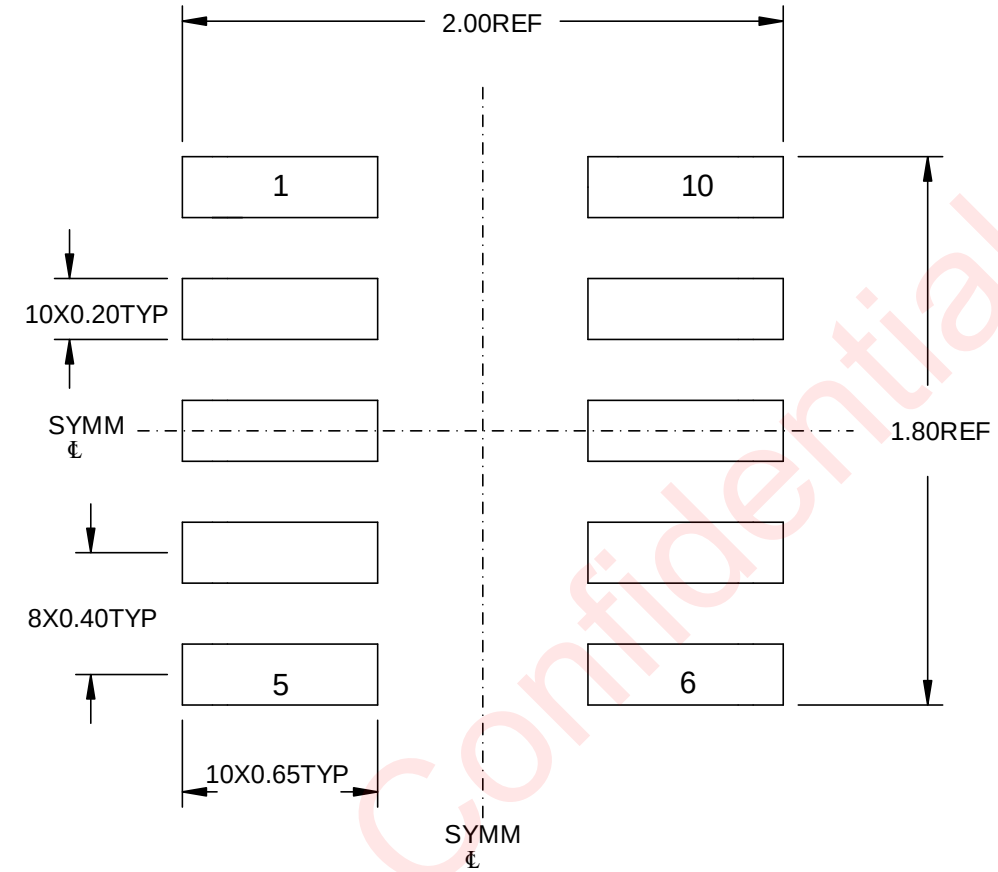
BOTTOM VIEW

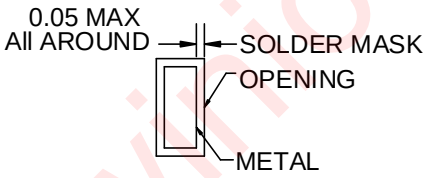


SIDE VIEW

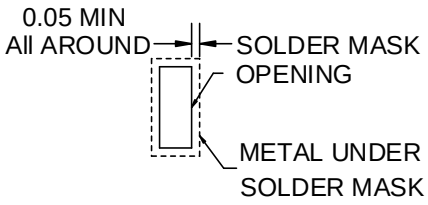
Unit：mm

LAND PATTERN DATA





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit：mm

Revision History

Version	Date	Change Record
V1.0	June.2020	Officially released

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