GX20MH01 Programmable 14-bit resolution single-bus high-precision temperature sensor

1. Fundamental characteristics

- A single port pin is required to communicate with a single bus interface
- Each chip has a globally unique 64-bit serial number
- With the multi-point distributed temperature measurement function
- No peripheral components are required
- Power can be supplied through the data line; the power supply voltage range is 2.5V~5.5V
- The measurement range is -55°C to +125°C (-67°F to +257°F)
- The accuracy was ± 0.1 C in the range from 0℃ to 50
- At the 14-bit accuracy, the temperature conversion speed is less than 1.6s
- With user-defined non-volatile temperature alarm settings
- The alarm search command identifies and identifies the device that exceeds the programmed temperature
- Super-static protection capability：HBM>8000V MM >800V
- The TO-92 package of the 3-feet

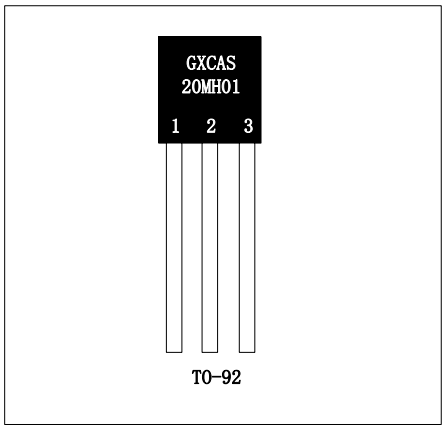
2. Application scenarios

- Body temperature measurement
- Drug storage
- Medical equipment and other fields

3. Chip overview

GX20MH01 Digital thermometer provides temperature measurement at 14bit resolution with a lower temperature limit through a programmable non-volatile storage unit and upper limit alarm. GX20MH01 Use the single bus protocol to communicate with the upper computer, requiring only one signal line and one ground line. It has a temperature measurement range ranging from-55℃ to + 125℃. Test accuracy in the range of 0℃ to + 50℃ can reach ± 0.1℃. In addition, it can work in parasitic mode, directly powering the chip through signal lines, thus without requiring additional power supply. Each GX20MH01 has a globally unique 64-bit serial number, which can network multiple GX20MH01 in series on the same documentary bus, and requires only one processor to control multiple GX20MH01 distributed in a large area. This networking mode is especially suitable for HVAC environmental control, construction, equipment, food situation temperature measurement, industrial temperature measurement, process monitoring and control and other application fields.

4. Pin configuration



Pipe foot description

Pipe foot position **TO-92**	**name**	**function**
3	VDD	Power supply pins; the VDC pins must be connected to the ground in the parasitic power supply mode
2	DQ	Data input and output pin that will power the chip in parasitic power supply mode (see the power supply description section of GX20MH01
1	GND	Ground pipe foot

Contents

5. Detailed information

5.1 General situation

Figure 1 is the structural block diagram of GX20MH01. The chip uses a unique chip serial number of a 64-bit read-only memory device. The chip internal temporary register contains two bytes of temperature registers used to store the data output by the temperature sensor. In addition, the chip provides a byte of temperature alarm threshold register (TH and TL) and a byte of configuration register. The configuration register allows the user to set the temperature measurement resolution to 9,10,11,12,13 or 14 bits, but in order to maintain accuracy the user is recommended to 12 bits. The TH, TL and configuration registers are non-volatile erasable registers (EEPROM), and the stored data will not disappear after the device fails.

GX20MH01 Adopt a single-bus protocol, and communicate through a single-line port. When all the devices are connected to the bus via a three-state port or an open leakage port, the control line needs to be connected to a weak pull-up resistance. In this bus system, the microprocessor (main device) relies on the 64-bit chip serial number unique to each device to identify the device on the bus and the device address on the recording bus. Since each device has a unique sheet serial number, the number of devices to which the bus can be connected is virtually infinite. Single bus protocol, including detailed explanation of instructions and "timing" are shown in the single bus system section.

Another function of the GX20MH01 is to work without an external power supply. When the bus is in a high level state, DQ and the pull-up resistance are connected to power the device through a single bus. At the same time, the bus signal in the high level state charges the internal capacitor (Cpp). When the bus is in the low level state, the capacitor provides energy to the device, and the way of providing energy becomes a "parasitic power supply". Of course, the GX20MH01 can be connected to the external power supply through the VDD pin.

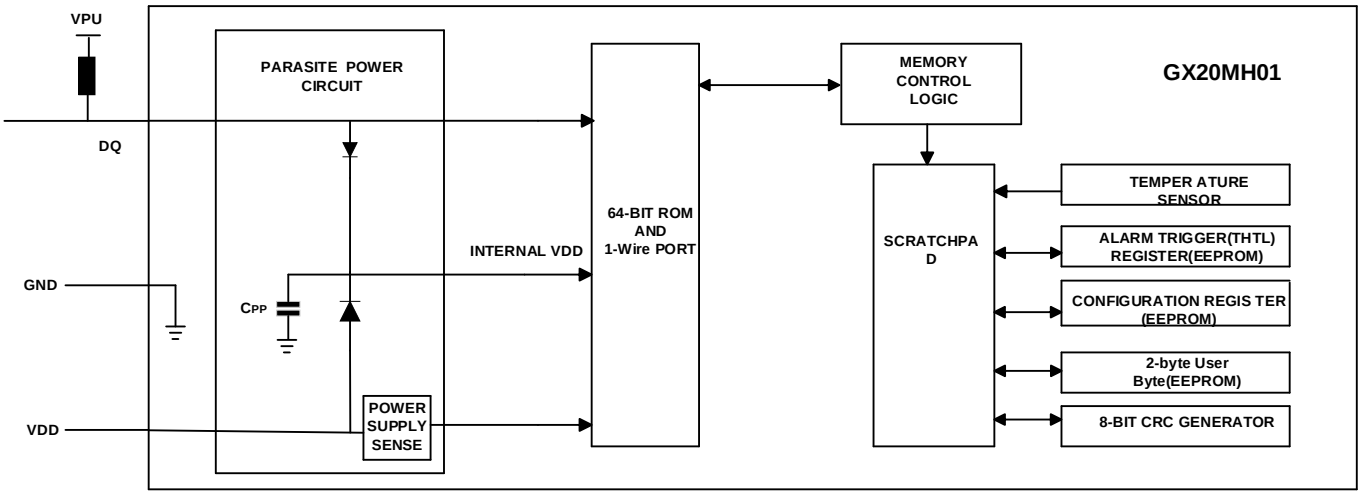


Figure 1. GX20MH01 structure block diagram

5.2 Temperature measurement operation

The core function of the GX20MH01 is its direct digital temperature sensor. The accuracy of the temperature sensor is user-programmable 9,10,11,12,13 and 14 bits. The temperature resolutions were 0.5℃, 0.25℃, 0.125℃, 0.0625℃, 0.03125℃, and 0.015625℃, respectively. The default precision is 12 bits in the power state. GX20MH01 Maintain low power waiting state after startup; for temperature measurement and AD conversion, the bus controller must issue [44h] command. After that, the resulting temperature data is stored in the temperature register in two bytes, with the GX20MH01 remaining in the waiting state. GX20MH01 When powered by external power supply, the bus controller initiates the "read sequence" after the temperature conversion instruction (see the single bus system section), GX20MH01 is returning 0 in the temperature conversion, and the conversion end return 1. If GX20MH01 is powered by parasitic power supply, unless the bus is pulled up during the temperature conversion, there will be no return value. The bus for the parasitic power supply shall be explained in detail in the GX20MH01 power supply section.

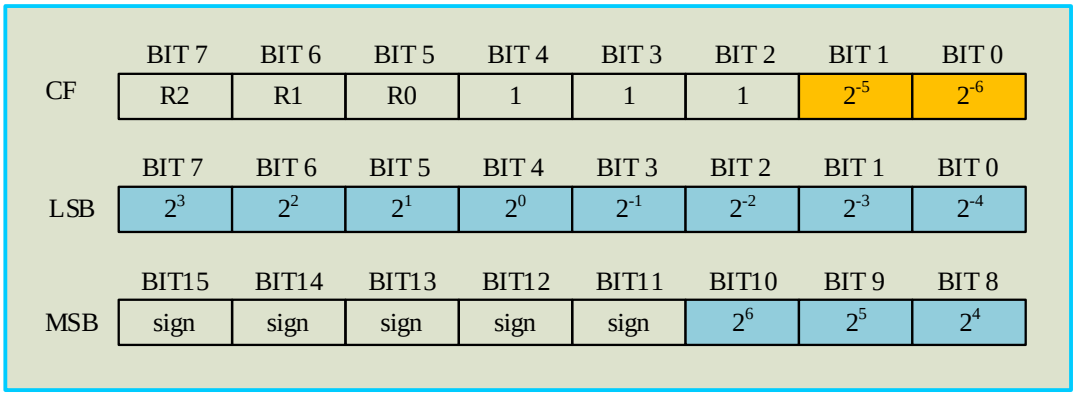


Figure 2. Temperature register format

Table 1. Temperature / data relationship

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0111 1101 0000 0000	7D00h
+85*	0101 0101 0000 0000	5500h
+25.0625	0001 1001 0001 0000	1910h
+10.125	0000 1010 0010 0000	0A20h
+0.015625	0000 0000 0000 0100	0004h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1000 0000	FF80h
-10.125	1111 0101 1110 0000	F5E0h
-25.0625	1110 0110 1111 0000	E6F0h
-55	1100 1001 0000 0000	C900h

The default value is + 85˚C

5.3 Alarm operation

GX20MH01 After a temperature conversion, the temperature value is compared with a user-defined alarm threshold stored in the TH and TL registers (as shown in Figure 3).Mark bit (S) indicates the positive and negative temperature value: positive number S=0, negative number S=1. The TH and TL registers are non-volatile (EEPROM), so the data remains after power loss.In the memory section it explains how the TH and TL are deposited in the 2nd and 3rd bytes of the register.

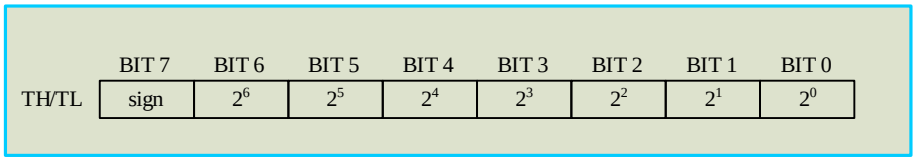


Figure 3. TH and TL register formats

When TH and TL are 8-bit registers, only the temperature register of 4 to 11 bits is applicable in comparison with TH and TL.If the measured temperature is higher than TH or lower than TL, and the alarm condition is valid, an alarm sign will be placed inside the GX20MH01.This sign is updated for every temperature measurement.Therefore, if the alarm status disappears, the sign will be turned off after the next temperature transition.The bus controller detects all GX20MH01 alarm signs on the bus by issuing an alarm search command [ECh].Any GX20MH01 with the alarm identification will respond to this command, so the bus controller can pinlocate each GX20MH01 that meets the alarm condition.If the alarm condition holds and the TH or TL settings have changed, another temperature transition will reconfirm the alarm condition.

5.4 GX20MH01 Power supply

GX20MH01 Can be powered by the pin VDD external power supply or work in parasitic power mode.The parasitic power supply mode allows the GX20MH01 to work in the external power supply demand state.Parasitic power modes are very useful for distance testing or space-restricted applications.The control circuit of the parasitic power supply is shown in Figure 1,When the bus is at a high level,The control loop "steals" the energy from the bus.Some of the "stolen" energy is stored in the parasitic power source storage capacitor (CPP), which releases the energy for the device when the bus is at a low level.When the GX20MH01 is in the parasitic power supply mode, the VDD pins must be grounded.

In parasitic power mode, single bus and CPP can provide sufficient current meeting the specified timing and voltage (see DC and AC characteristics) to GX20MH01.However, when the GX20MH01 is performing a temperature conversion or transmitting data from the register to the EEPROM, the operating current can be up to 1.5 mA.This current may cause an unacceptable pressure drop in the weak drag resistance connected to the single bus, which requires a larger current, which the CPP could not provide.In order to ensure that GX20MH01 has sufficient power

supply, when the temperature conversion or copy data to EEPORM operation, must provide a strong pull up to the single bus, using MOSFET directly pull the bus to the power supply,As shown in Figure 4. After issuing the temperature conversion instruction [44h] or the copy register instruction [48h],The single bus must be converted to a strong pull within up to 10us and must be kept strong at the temperature conversion sequence (tconv) or copy data sequence (twr = 10 ms).When the strong pull-up state is maintained, no other action is allowed.

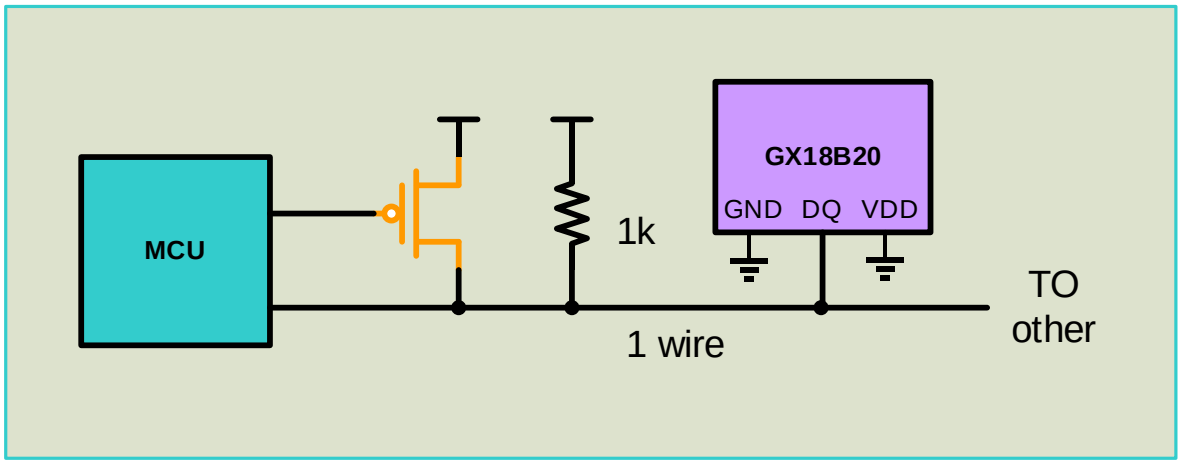


Figure 4. Power for parasitic GX20MH01 during temperature transition

Another way to power the GX20MH01 is the conventional access of an external power supply from the VDD pin,As shown in Figure 5. The advantage of this is that there is no need to pull up strongly on the single bus, and the bus does not have to remain high during the temperature transition.

The parasitic power supply is not recommended for temperatures above 100℃, because the GX20MH01 exhibits a relatively large leakage current at this temperature,Communication may not be possible. At a similar temperature, the GX20MH01 VDC pin supply is strongly recommended.For the bus controller does not know whether the GX20MH01 on the bus uses parasitic power supply or external power supply, GX20MH01 prepared a signal indication power supply use diagram.The bus controller issues a Skip ROM command [CCh] and then a read power supply command [B4h],After this command is issued, the controller issues a reading timing command, and the parasitic power supply will pull the bus down,The external power supply keeps the bus high. If the bus is pulled down, the bus controller will know to provide a strong pull-up on the single bus during the temperature transition.

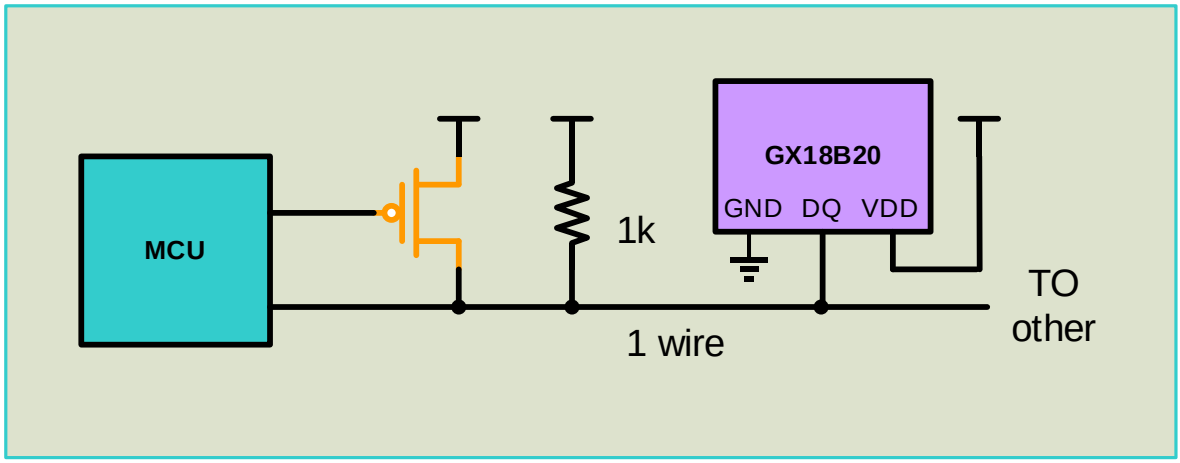


Figure 5. Use an external power supply to power the GX20MH01

6. Memory

6.1 A 64-bit read-only memory

Each GX20MH01 has a unique 64-bit code stored in the ROM (see Figure 6).The first 8 digits are a single line series code: 28h.The next position 48 is a unique serial number.The last 8 bits are the CRC codes for the above 56 bits.Detailed explanation of the CRC is provided in the CRC generator section.The 64-bit ROM and ROM operating control areas allow the GX20MH01 to act as a single bus device and work following the single bus protocol detailed in the single bus system section.

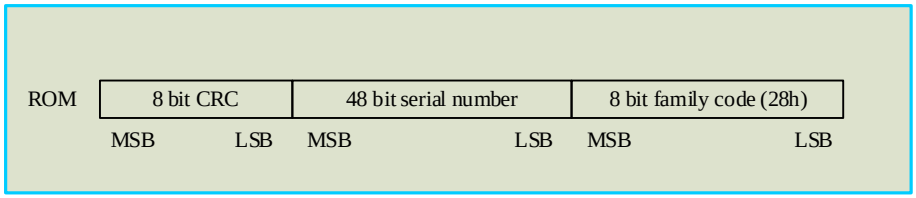


Figure 6. 64-bit ROM code

6.2 Memory

The memory structure of GX20MH01 is shown in Figure Figure 7.The memory has a staging SRAM and a storage manuscript alarm threshold TH and TL of non-volatile electrical erasable EEPROM composition.Note that when the TH and TL registers can be used as normal registers. All memory instructions are detailed in the GX20MH01 functional instruction section.

The byte 0 and byte 1 bytes of the memory are the LSB and the MSB of the temperature register, respectively,

and the memory of these two bytes is the read-only memory.Section 2 and 3 are TH and TL.The fourth byte is the configuration register data,However, the lowest 2bits of this register is used as a temperature register, as detailed in the configuration register section.Byte 5 is retained by the device prohibited; bytes 6 and 7 can be used by the user.

The 8th byte of the memory is read-only and contains the CRC code of the eight bytes above, and the CRC performs as described in the CRC Generator section.

Data is written to the 2,3,4,6 and 7 bits of the memory by the write register instruction [4 Eh]; data must be transmitted with the second byte as the lowest effective bit.For complete validation data, the memory can be read after the data is written (using the read register instruction [BEh]).When reading the register, the data is removed from the single bus with byte 0 as the lowest valid bit.The bus controller must issue a copy register instruction [48h] when transferring TH, TL and configuration data from register to EEPROM.

EEPROM The data in the memory remains maintained after the device is power;When powered on, the data is loaded into the register.Data can also be loaded from the register into the EEPROM via the recall EEPROM command.The bus controller issues the read sequence after issuing this command, GX20MH01 returns 0 indicates that the recall is ongoing,Return to 1 indicates the end of the operation.

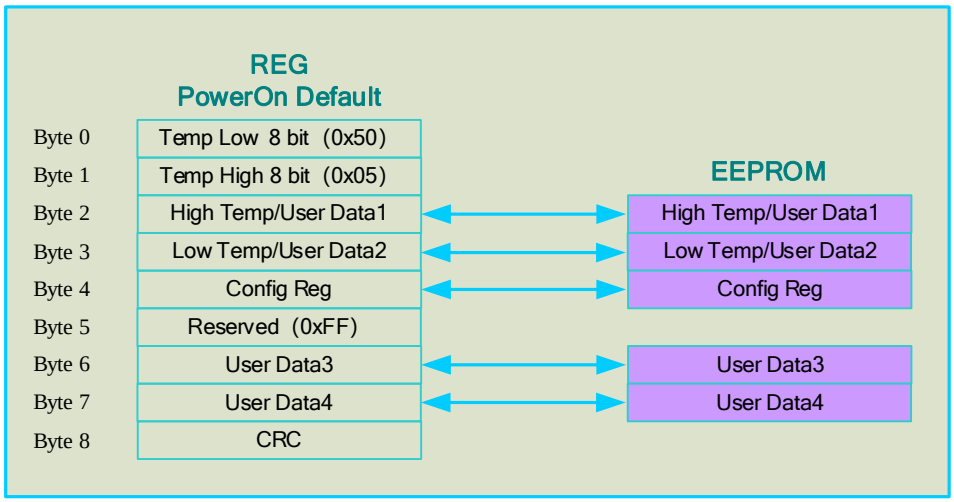


Figure 7. GX20MH01 memory diagram

6.3 Configure register

The fourth byte of the memory is the configuration register,Its structure is shown in Figure Figure 8.The user can set the accuracy of the GX20MH01 by setting the R2, R1 and R0 bits as shown in Table 2.Power on the default settings:R2=0, R1=1, R0=1 (12-bit precision).Note: There is a direct relationship between accuracy and conversion time.The configuration register bit 7 and bits 0 to 4 are retained by the device,write inhibit;When reading the

data,They all behave as logic 1.

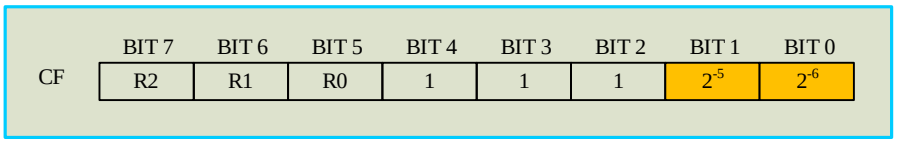


Figure 8. Configure the register

Table 2. Sensor accuracy configuration table

R2	R1	R0	RESOLUTION (BITS)	MAX CONVERSION TIME	
0	0	0	9	50ms	
0	0	1	10	100ms	
0	1	0	11	200ms	
0	1	1	12	400ms	
1	0	0	13	800ms	
1	0	1	14	1600ms	(t_{CONV})
1	1	*	14	1600ms	(t_{CONV})

7. CRC gen

The CRC is stored in memory as part of the GX20MH01 64-bit ROM.CRC codes were calculated from the first 56 bits of the ROM,Is included in the important byte of the ROM.The CRC is calculated from the data stored in the memory,So when the data in the memory changes,The value of the CRC also changes accordingly.

The CRC can verify the data when the bus controller reads the GX20MH01.To verify that the data is being read correctly,The bus controller must compare the received data to calculate a CRC value with the value stored in the 64-bit ROM of GX20MH01 (when reading ROM) or the 8-bit CRC value calculated inside GX20HM01 (when reading register).If the calculated CRC value matches the read CRC value, the data is transferred without error.The comparison of CRC values and whether to perform the next step is completely determined by the bus controller.When the CRC value stored in or calculated by the GX20MH01 does not match the value calculated by

the bus controller,GX20MH01 There is no circuit inside that prevents the command sequence from proceeding. The CRC is calculated as follows:

$$CRC = X^8 + X^5 + X^4 + 1$$

A single-bus CRC can be generated by a polynomial generator with a shift register and an XOR gate,As shown in Figure 9.This loop consists of a shift register and several XOR gates,Individual bits of the shift register are initialized to 0.Starting from the 0 byte of the lowest valid bit or register in the ROM,Move into a register one at a time.After transmitting the data in the 56-bit ROM or moving into the highest bit of the 7th byte of the register,The CRC values are stored in the shift register.Next, the value of the CRC must be recycled into.this moment,If the calculated CRC is correct, the shift register will be reset to 0.

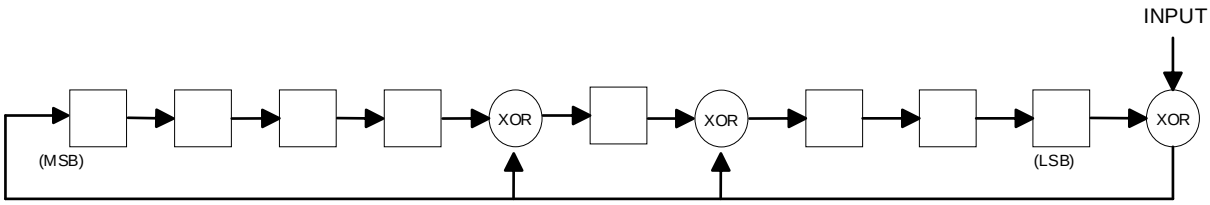


Figure 9. The CRC generator

8. Nnibus system

A single bus system uses a single bus controller to control one or more slave devices.GX20MH01 Always acts as a slave machine.When only one slave hangs on the bus,The system is called a "single-point" system;If multiple servers hang on the bus, the system is called a "multipoint" system.

All data and instructions are passed through the single bus starting from the lowest effective bit.The single bus system is discussed in three aspects: hardware structure, execution sequence, and single bus signal (signal type and timing).

9. Hardware structure

The single-bus system has only one defined signal line,The device on each bus must be a drain or three-state output.The device (master or slave) on each bus must be a drain open or three-state output.This mechanism causes each device on the bus that does not transmit data to release the bus for other devices to use.GX20MH01 The single bus port (DQ pin) is an open drain type, and the internal equivalent circuit is shown in Figure 10.

The single bus requires an external pull resistance of about 1 KΩ; the single bus idle state is high level.If there is a certain need to suspend a transmission, the bus must remain idle if you wanst to resume it.During the recovery

period,If the single bus is in an inactive (high-level) state,The recovery time between bits can be infinitely long.If the bus stays at a low level over 480us, all the devices on the bus will be reset.

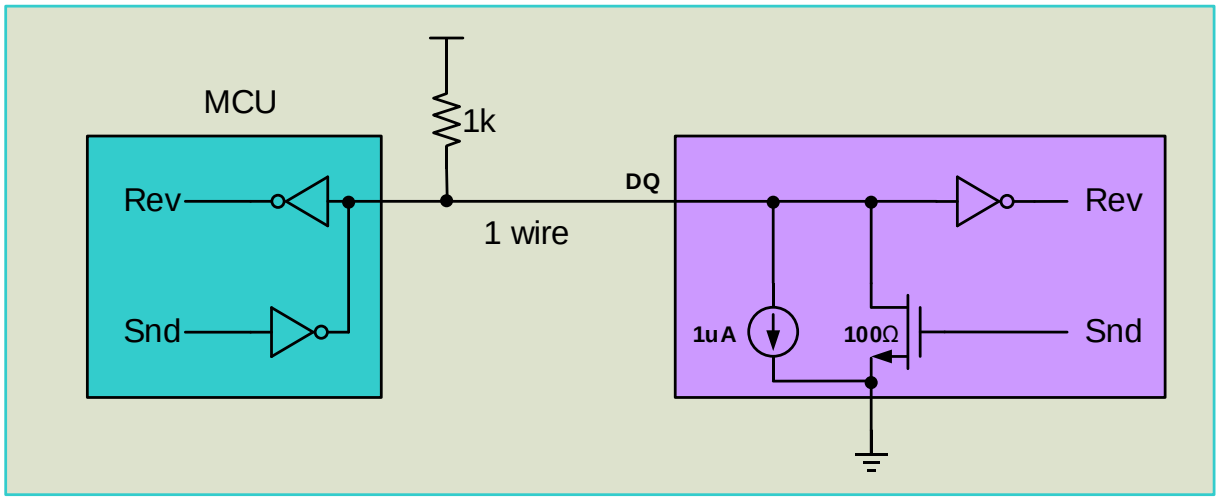


Figure 10. Hardware structure diagram

10. Execute the sequence

The execution sequence of GX20MH01 accessed via a single bus is as follows:

Step 1: Initialization

Step 2: The ROM operation instruction

Step 3: GX20MH01 Functional instruction

Each GX20MH01 operation must meet the above steps,If the steps are missing or the orders are confusing,The device will not have any return values.Search ROM command and alarm search command except.When both commands execute, the master controller must return to step 1.

10.1 Initialise

All execution through a single bus starts with a sequence of initialization programs.The initialization sequence contains a reset pulse emitted by the bus controller and a subsequent presence pulse emitted by the slave.There ses exists to let the bus controller know that the GX20MH01 is on the bus and is ready to operate, see the bus signal section.

10.2 ROM instruct

Once the bus controller detects a presence pulse,It just issues a ROM instruction.If there are multiple GX20MH01 to hang on the bus,These instructions will give the device a unique 64-bit ROM sequence code,causes the bus controller to select the specific device to be operated.These instructions can also enable the bus controller to identify how many,What type of device hangs on the bus,same,They can also identify which devices already meet

the alarm conditions.ROM instructions has 5,Both are 8-bit in length.The bus controller issues a ROM command before initiating a GX20MH01 function command.See Figure Figure 11 for the ROM instruction operation diagram.

SEARCH ROM [F0h]

When the system is electrographically initialized,The bus controller must identify all the ROM sequence codes on the bus to obtain the number and model of the slave machine.The bus controller checks the ROM code multiple times through the search ROM instruction to confirm all from the machine parts.If there is only one slave on the bus,Instead the search ROM instruction with a relatively simple read ROM instruction (see below).After each search for the ROM command, the bus controller must return to step 1 (initialization).

READ ROM [33h]

This command can only be used when a single GX20MH01 exists on the bus.This command allows the bus controller to read the 64-bit sequence code of the slave machine without using the Search ROM instruction.If the command is used for more than one slave on the bus, data conflicts occur when all slave attempt to transmit signals at the same time.

MATCH ROM [55h]

MATCH ROM Command is followed by the 64-bit ROM serial number,The bus controller locates a specific slave device on the multipoint bus.Only the GX20MH01 that exactly matches the 64-bit ROM serial number can respond to the subsequent memory operation instructions;All slave planes that do not match the 64-bit ROM sequence number will wait for the reset pulse.

SKIP ROM [CCh]

This command allows the bus controller to use functional instructions without providing a 64-bit ROM encoding.for instance,The bus controller can first issue a ignore ROM instruction,Then issue a temperature conversion command [44h],To complete the temperature conversion operation.pay attention to:When only one slave is on the bus,in any case,After ignoring the ROM instruction, only one read register instruction [BEh] can be followed.Use this command in the single-point bus case,Device does not need to send back a 64-bit ROM code,This saves you time.If more than one slave is on the bus,If the ignore ROM instruction is issued, since multiple servers transmit data at the same time,Data conflicts will occur on the bus.

ALARM SEARCH [ECh]

The operation process of this instruction is the same as the search ROM instruction, and only the slave that meets the alarm condition will respond to the command.This command allows the master device to determine whether any GX20MH01 has experienced an alarm state during the most recent temperature transition.After each

alarm search command cycle,The bus controller must return to step 1.See the alarm signal operation section for the alarm operation process.

10.3 GX20MH01 Functional instructions

After the bus controller uses the ROM command to determine the GX20MH01 with which it wishes to communicate,The host can issue a GX20MH01 function command.These instructions allow the bus controller to read and write the registers of the GX20MH01,Initiate the temperature conversion and identify the power supply mode. GX20MH01 Functional instructions are detailed below,It is also summarized in Table 3 and illustrated in Figure 12.

CONVERT T [44h]

This command is used to start a single temperature conversion.After the temperature conversion command is executed,The resulting temperature conversion result data is stored in the temperature register in 2 bytes,Then the GX20MH01 maintains a low-power waiting state.If the instruction is issued in the parasitic power supply mode,During the temperature transition period (tCONV),Pull the single bus within 10us (maximum),See the GX20MH01 power supply section.If the GX20MH01 is powered by an external power source,The bus controller follows the issuing reading sequence after issuing the command,GX20MH01 If it is in the conversion,Then the bus returns to 0,If the temperature conversion is complete,Then return 1.In the parasitic power supply mode,The bus is strongly pulled up before such communication mode will not be used.

WRITE SCRATCHPAD [4Eh]

This command writes the data to the GX20MH01's register,The Start position is in the TH register (the 2nd byte of the register),Next, write to the TL register (the third byte of the register),Last write to the configuration register (the fourth byte of the register),Data data transmission at the lowest valid bit.The writing of the above three bytes must occur before the bus controller issues the reset command, otherwise data conflicts will occur.

READ SCRATCHPAD [BEh]

The host reads the register command during this command.The read will start from the lowest valid bit of byte 0,Keep going,Until the 9th byte (byte 8, CRC) is finished,If you don't want to read through all the bytes,The controller can issue a reset command at any time to abort the reading.

COPY SCRATCHPAD [48h]

This command copies the contents of TH, TL and configuration registers and the user bytes 3,4 (2,3,4,6,7 bytes) to EEPROM.If the parasitic power bus controller must start a strong pull-up and hold at least 10ms within 10us of issuing this command, see as described in the GX20MH01 Supply section.

RECALL E^2 [B8h]

This command copies the TH, TL, and configured data from the EEPROM back to the register.The bus controller sends the reading sequence after issuing the command,GX20MH01 The copy identity is output:The 0 identity is copying back,1 identifies the end of the copy back.This operation is performed automatically, when the GX20MH01 is powered on,So there is valid data in the device as soon as it is in the register.

READ POWER SUPPLY [B4h]

The bus controller issues the reading sequence after this command is sent to the GX20MH01,n the parasitic power supply mode, the GX20MH01 will pull down the bus;In the external power supply mode,GX20MH01 Will pull the bus higher.Information on the usage of this directive is detailed in the GX20MH01 power supply section.

Table 3. GX20MH01 Functional instruction sheet

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITYAFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	GX20MH01 transmits conversion status to master (not applicable for parasite-	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	GX20MH01 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, 4, and 6, 7(T_H, T_L, configuration registers and User Bytes).	4Eh	Master transmits 3 or 4 or 5 data bytes to GX20MH01.	3
Copy Scratchpad	Copies T_H, T_L, config register and User Bytes data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, config register and User Bytes data from EEPROM to the scratchpad.	B8h	GX20MH01 transmits recall status to master.	
Read Power Supply	Signals GX20MH01 power supply mode to the master.	B4h	GX20MH01 transmits supply status to master.	

Note 1：For parasitic power mode GX20MH01 during temperature conversion and copy data to EEPROM,The single bus must be given a strong pull, and the bus can have no other activity during this time.

Note 2：The bus controller can abort the data transmission at any time by sending out a reset signal.

Note 3：The three bytes of TH, TL and configuration register must be written before the reset signal is initiated.

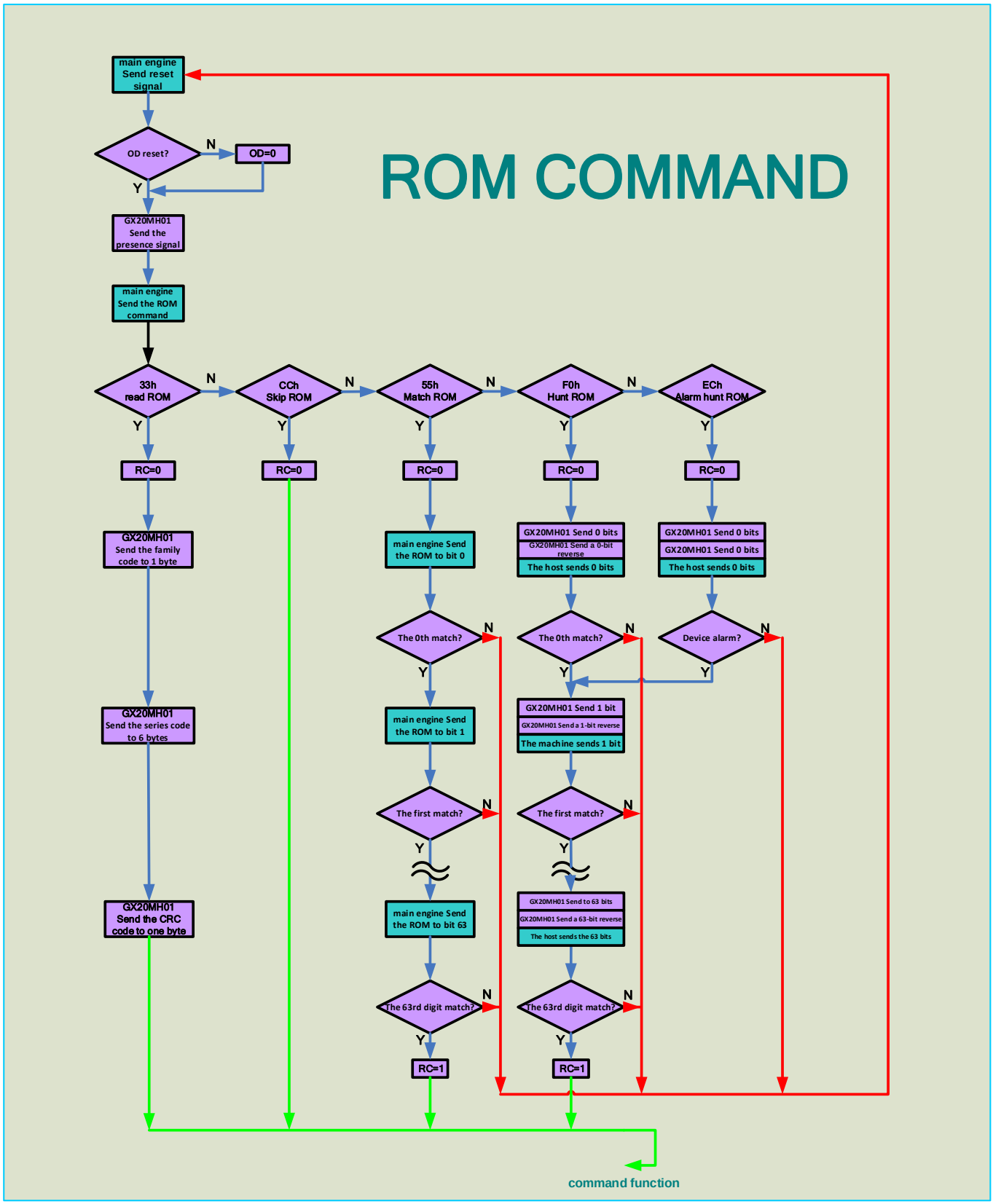


Figure 11. Flow chart of ROM instructions

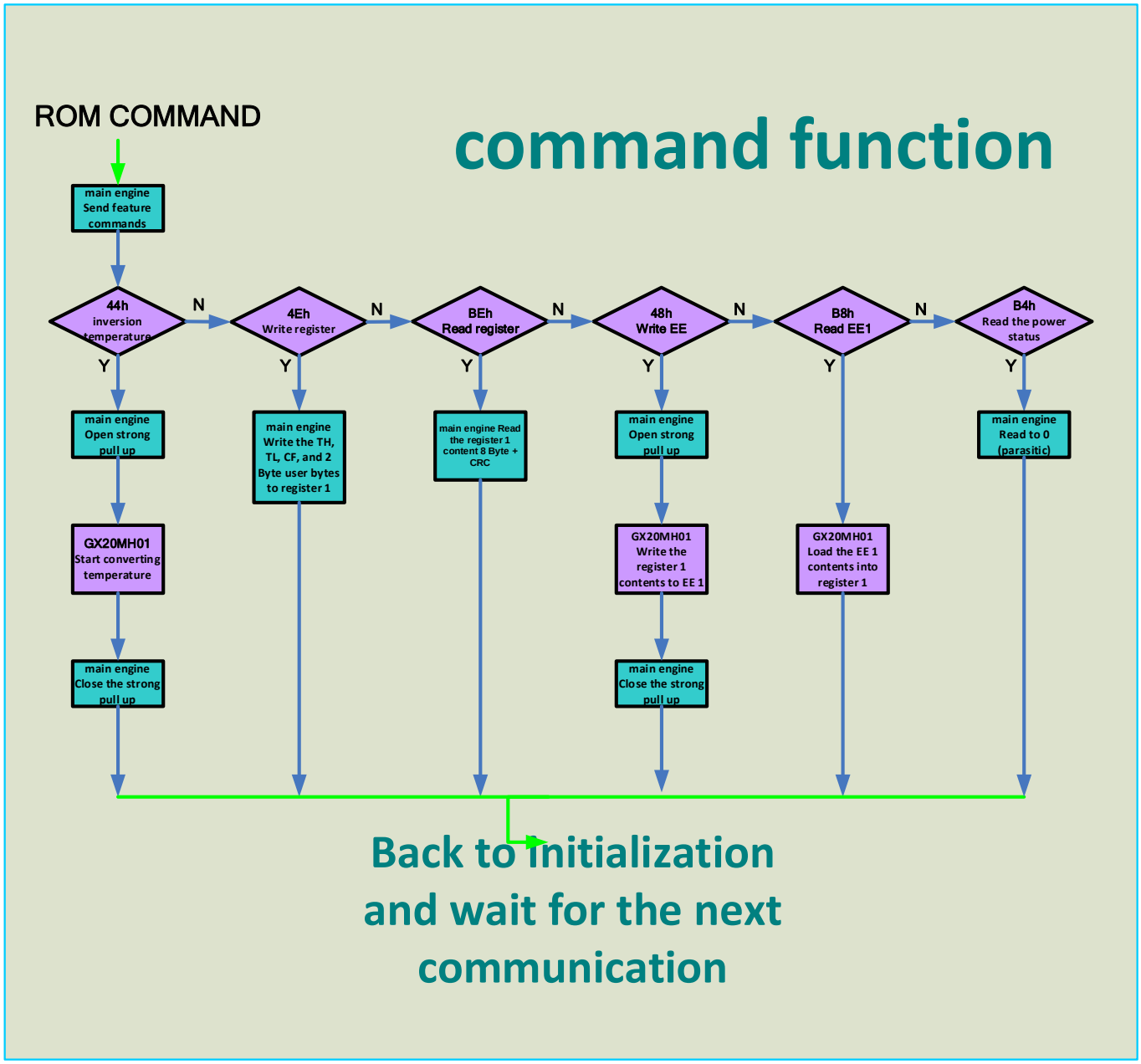


Figure 12. Flow chart of GX20MH01 functional instructions

11. Single bus signal

GX20MH01 A strict single-bus protocol is required to ensure data integrity.The protocol defines several types of single-bus signals:Respulse, presence pulse, write 0, write 1, read 0, and read 1. All these signals,Except for in the presence of the pulses,Are all emitted by the bus controller.

11.1 Reset sequence: reset and presence of a pulse

All and the between-GX20MH01 communication begin with an initialized sequence,The initialized sequence is shown in Figure Figure 13.A reset pulse followed by a presence pulse indicates that the GX20MH01 is ready to send and receive the data.

During the initialization of the sequence,The bus controller pulls down the bus and maintains 480us to emit (TX) a reset pulse signal,Then release the bus,Enter the receiving state (RX).When the bus is released,The 1 kΩ pull-up resistance pulls the bus to a high level.After the GX20MH01 has detected the rising edge on the IO pin,Wait for the period of 15-60us,A pulse of 60-240us low level signal is then emitted.

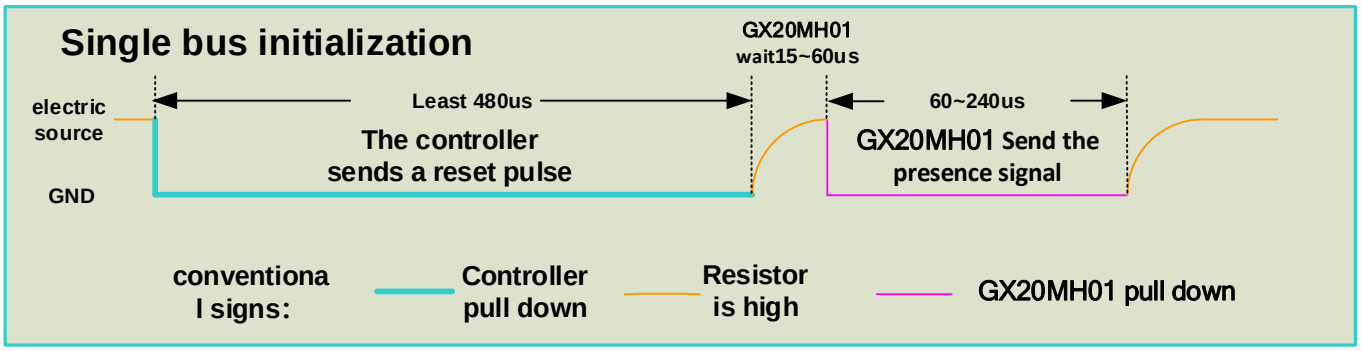


Figure 13. Initialize the sequence

11.2 Read / write the timing

GX20MH01 Data reading and writing is used for information exchange through temporal processing,Each time sequence transmits 1 bit of data.

Write the timing

GX20MH01 There are two kinds of writing sequence: writing 1 sequence and writing 0 sequence.The bus controller writes logic 1 by writing 1 sequence;Write logic 0 by writing 0 sequence.Writing timing must last at least 60us,ncluding a recovery time of at least 1us between the two writing cycles.When the bus controller pulls the data line down from the logical high level to the low level,Start the timing (see Figure 14).

The bus controller to write to produce a write sequence,The data cable must be pulled to a low level and then released,The bus shall be released within 15us.When the bus is released, the pull-up resistance will drag the bus

up.To generate the write 0 time sequence, the bus controller must pull the data line to a low level and maintain at least 60us.After the bus controller initializes the write time sequence,GX20MH01 Adopt the signal lines in a window from 15us to 60us.If the level is high on the line, write 1.Instead, if the line is low, write 0.

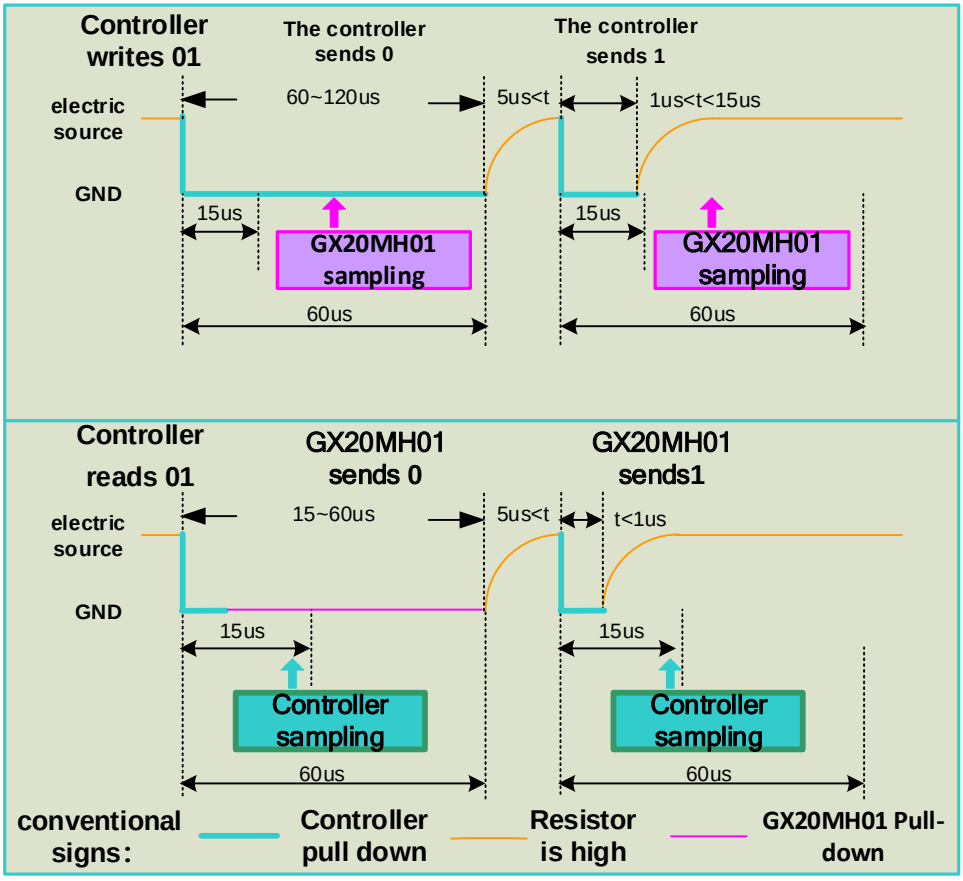


Figure 14. Read / write time slot timing diagram

Read the timing

When the bus controller initiates the reading sequence,GX20MH01 Is used to transfer data to the controller.therefore,The bus controller must start the sequence immediately after issuing the read register instruction [BEh] or the power mode command [B4h],So that the GX20MH01 can provide the requested data.besides,The bus controller reads the time sequence after issuing the sending temperature conversion command level [44h] or recalling the EEPROM command [B8h],See the GX20MH01 functional instruction section for details.

All reading sequence must be at least 60us,Recovery time of at least 1us during two read weeks was included.When the bus control pulls the data down from high to low,Read time sequence starts, the data line must remain at least 1us,The bus is then released (see Figure 14).After the bus controller issues the read time sequence,GX20MH01 Transfer 1 or 0 by raising up or pulling down the bus.When the transmission of the 0

ends,The bus will be released,Return to the high-level idle state by pulling up the resistance.The data output from GX20MH01 is valid within 15us after the onset of the read sequence.Therefore, the bus controller releases the bus within 15us at the start of the reading sequence and then samples the bus state to read the state of the data line.Figure 15 identifies that the sum of TINIT, TRC, and TSAMPLE must be less than 15us. Figure 16 indicates that the system time can be maximized by keeping TINIT and TRC holding time as short as possible and placing the controller sampling time to the end of the 15us cycle.

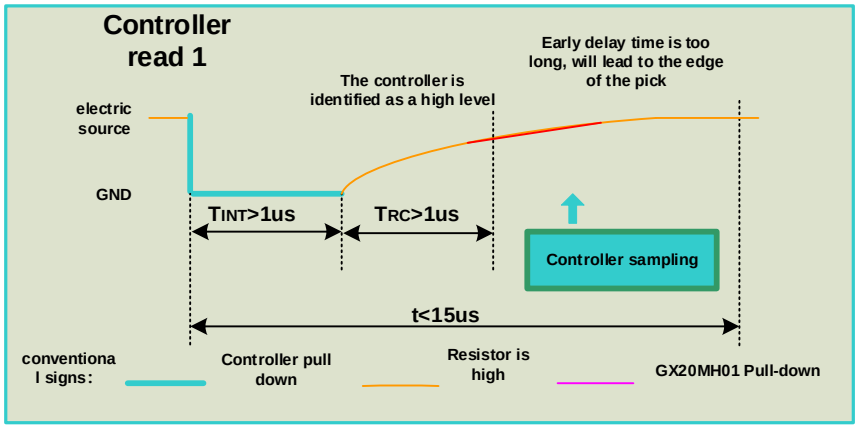


Figure 15. Detailed timing of the controller read 1

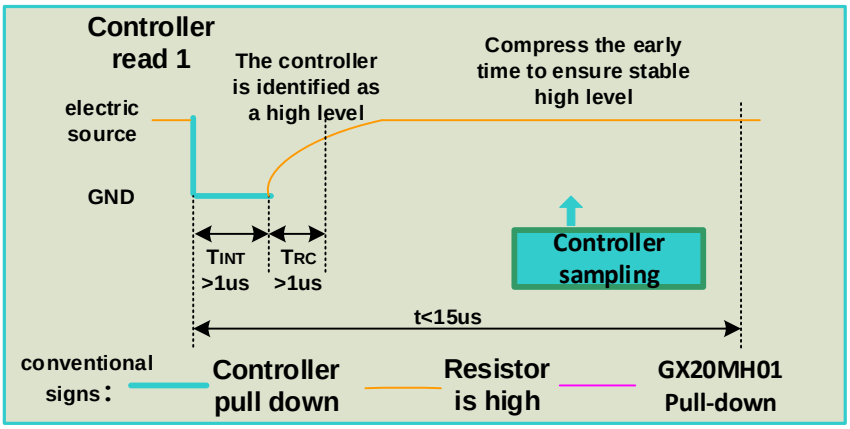


Figure 16. Recommended control read 1 timing

12. GX20MH01 Operation for example

12.1 Instance 1

In this example,There are several GX20MH01 powered by parasitic power supply hanging on the bus.The bus controller initiates a temperature conversion of a specific GX20MH01,Its register is then read and the CRC is recalculated to confirm the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	The controller emits a reset pulse
Rx	Presence	GX20MH01 Return presence pulse
Tx	55h	The master controller sends a matching ROM command
Tx	64-bit ROM code	The main controller sends the GX20MH01 address
Tx	44h	The main controller sends a temperature conversion command
Tx	DQ line held high by strong pullup	The DQ signal is saved during the conversion period, and the temperature conversion has been completed
Tx	Reset	reset pulse
Rx	Presence	GX20MH01 Return presence pulse
Tx	55h	The master controller sends a matching ROM command
Tx	64-bit ROM code	The main controller sends the GX20MH01 address
Tx	BEh	Master control reading register instruction
Rx	9 data bytes	Read the entire register plus CRC: the controller recalates the CRC of 8 data bytes read from the register, compares the calculated CRC with the read CRC, if the same, the controller goes down; if different, operates again

12.2 Instance 2

In this example, there is only one parasitic power supply of GX20MH01 on the bus.Controller writes TH, TL and configuration registers,Then the read register then calculates the CRC to verify the data.The master controller copies the data in the register into the EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	reset pulse

Rx	Presence	GX20MH01 Return presence pulse
Tx	CCh	Skips the ROM instruction
Tx	4Eh	Write register instructions
Tx	3 data bytes	Write 3 data to TH, TL, and configuration registers.
Tx	Reset	reset pulse
Rx	Presence	GX20MH01 Return presence pulse
Tx	CCh	Skips the ROM instruction
Tx	BEh	Read the register instructions.
Rx	9 data bytes	The main controller reads all registers including the CRC: the controller recalates 8 bytes of CRC read from the register, compares the calculated CRC with the read CRC, if the same,
Tx	Reset	reset impulse.
Rx	Presence	GX20MH01 Return presence pulse
Tx	CCh	Skips the ROM instruction.
Tx	48h	Copy the register instruction
Tx	DQ line held high by strong pullup	The controller gives a DQ a strong pull-up and holds at least 10ms during the copy operation

13. Limit usage conditions

Voltage range of each pin to the ground ..... -0.5V to +6.0V

operating temperature range ……..-55°C to +125°C

Storage range ……..... -55°C to +125°C

Welding temperature range ..... reference J-STD-020A rule

The above points out the environmental conditions required by the device in the normal operation, and the long-term working under the limit conditions may affect the reliability of the device.

14. Direct-current characteristic

(-55°C to +125°C; V_{DD} = 2.5V to 5.5V)

parameter	symbol	condition	minimum	representative	maximum	unit	notes
supply voltage	V_{DD}	Local power	+2.5		+5.5	V	1
Pull-up power supply voltage	V_{PU}	Parasitic	+2.5		+5.5	V	1,2
		Local power	+2.5		V_{DD}		
temperature error	t_{ERR}	-10℃~+85℃			±0.4	℃	3

		-55℃~+125℃			±1.2		
Enter the logic to	V_{IL}		-0.3		+0.8	V	1,4,5
Enter the logic high level	V_{IH}	Local power	+2.2		5.5 and lower in VDD + 0.3	V	1,6
		Parasitic	+2.5				
Irrigation current	I_L	$V_{I/O}$ = 0.4V	4.0			mA	1
Standby current	I_{DDS}			750	1000	nA	7,8
working current	I_{DD}	V_{DD} = 5V		1	1.5	mA	9
DQ input currenton	I_{DQ}			5		μA	10
shift				±0.2		℃	11

remarks:

1) All voltages are based on the ground potential as the reference potential.

2) The pull-up voltage is obtained as follows:Assuming that the pull-up device is perfect,Therefore, the high ceiling should be equal to the VPU. To meet the VIH specifications of the GX20MH01,The actual transistor pull-up supply must include the voltage drop limit; so the VPU _ ACTUAL = VPU _ IDEAL + VTRANSISTOR.

3) Typical curves are shown in Figure Figure 17.

4) The logical 0 level is obtained at an absorption current of 4 mA.

5) Low-voltage state in the parasitic power supply mode,To ensure the presence of the pulse VILMAX may have to be reduced to 0.5V.

6) The logic 1 voltage is obtained at the source current of 1 mA.

7) The standby current is defined at 70℃; the typical standby current value at 125℃ is 3 uA.

8) To reduce the IDDS, the range of the DQ is as follows: GNDDQGND + 0.3V or VDD 0.3 VDQVDD.

9) Dynamic current involves temperature conversion and write in EEPROM memory.

10) The DQ data line is high (the "high resistance" state).

11) The drift of the data was obtained at the + 125 C supply voltage VDD = 5.5 V tested for 1000 hours.

15. AC characteristic

nonvolatile memory (-55°C to +125°C; V_{DD} = 2.5V to 5.5V)

parameter	symbo	condition	minimu	representative value	maximum	unit
NV Write Cycle Time	t_{WR}			8	12	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	1000			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

(-55°C to +125°C; V_{DD} = 2.5V to 5.5V)

parameter	symbol	condition	minimu	representative value	maximum	unit	notes
Temperature Conversion Time	t_{CONV}	9-bit resolution			93.75	ms	1

		10-bit resolution			187.5		
		11-bit resolution			375		
		12-bit resolution			750		
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	μs	
Time Slot	t_{SLOT}		60		120	μs	1
Recovery Time	t_{REC}		1			μs	1
Write 0 Low Time	t_{LOW0}		60		120	μs	1
Write 1 Low Time	t_{LOW1}		1		15	μs	1
Read Data Valid	t_{RDV}				15	μs	1
Reset Time High	t_{RSTH}		480			μs	1
Reset Time Low	t_{RSTL}		1			ms	1
Presence-Detect High	t_{PDHIGH}		15		60	μs	1
Presence-Detect Low	t_{PDLOW}		60		240	μs	1
Capacitance	$C_{IN/OUT}$				25	pF	

remarks:：

1) Typical characteristic curves are shown in Figure Figure 17.

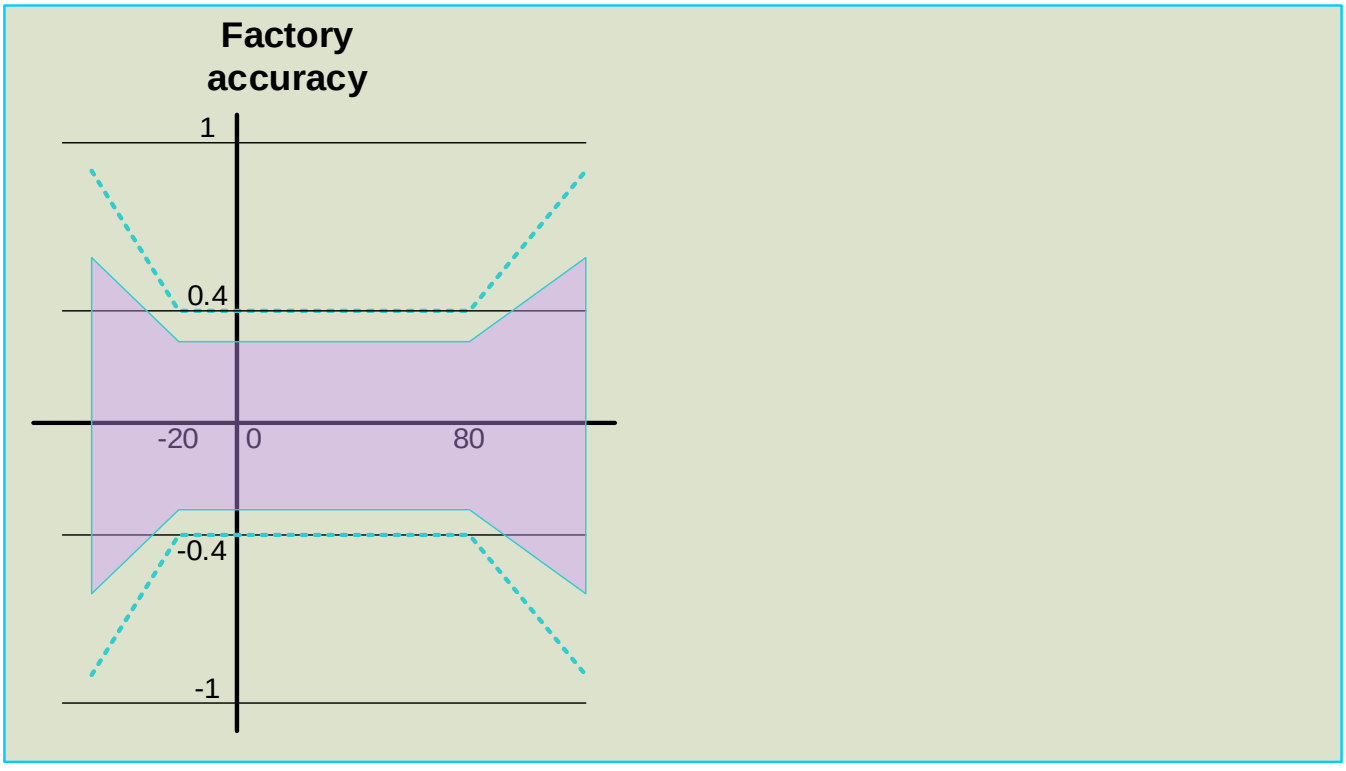


Figure 17. Typical characteristic curves

2) See Figure Figure 18 for the timing.

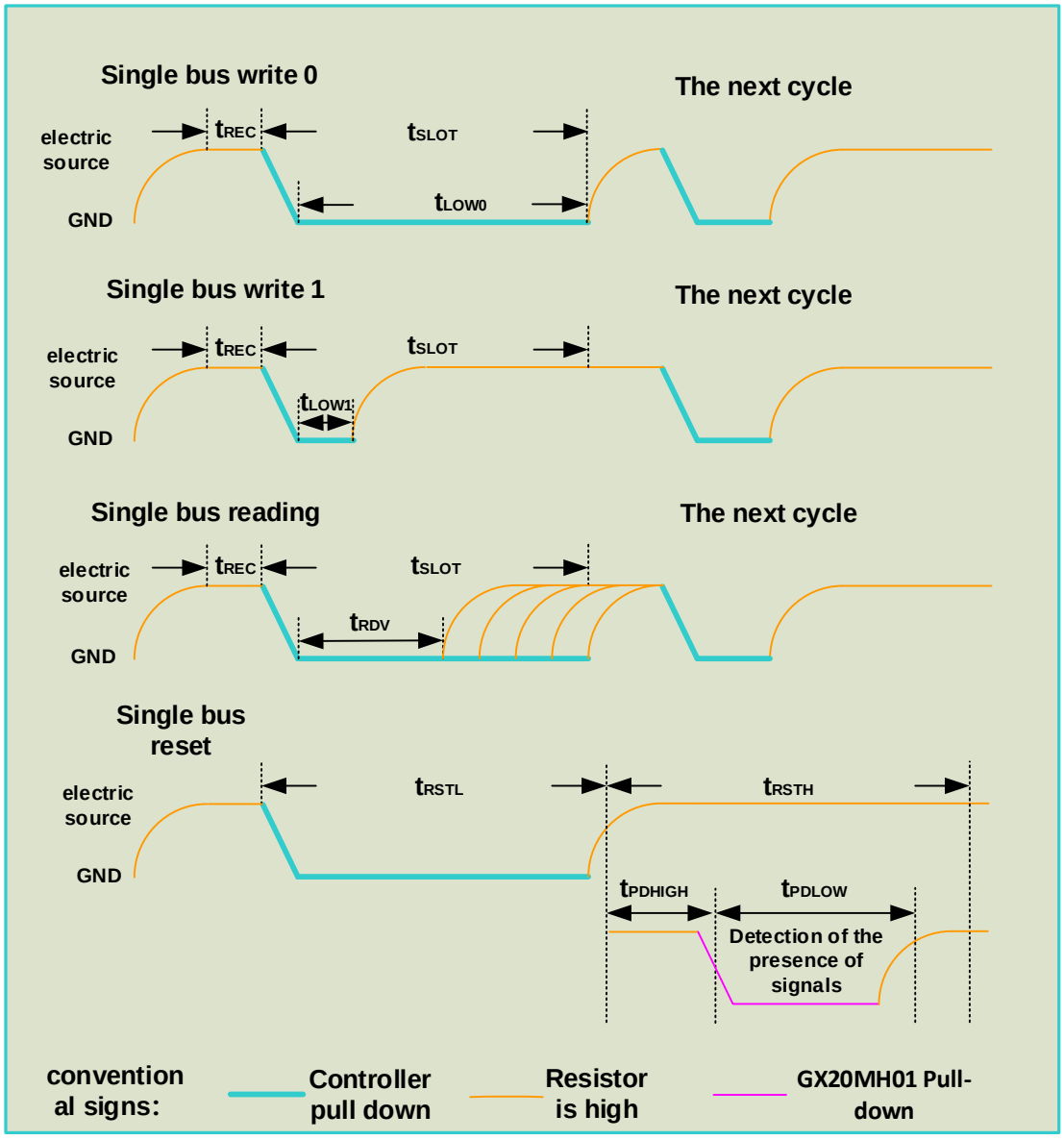


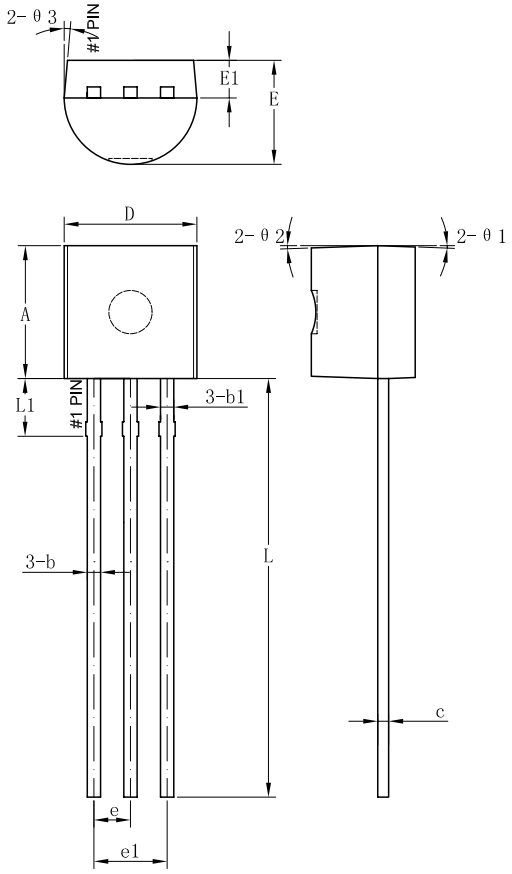
Figure 18. Timing sequence

16. List of product package models

model	Packaging form	accuracy
GX20MH01	TO-92（3 Pin）	±0.4℃

16.1 Package size

1) TO92 Package



符号	机械尺寸/mm		
	最小值	典型值	最大值
A	4.5	4.6	4.7
b	0.38	0.45	0.56
b1		0.45	
c	0.36	0.38	0.51
D	4.5	4.6	4.7
E	3.45	3.6	3.75
E1	1.2	1.3	1.4
e		1.27	
e1		2.54	
L	13.5	14.5	15.3
L1		1.96	
θ1		2°	
θ2		2°	
θ3		5°	

Order information

Purchase code	component	package	Standard packaging quantity	remark
GX20MH01-Bu	GX20MH01	TO92(3)	2000	in bags