2022

Motorcomm YT8010A Datasheet

100BASE-T1 PHY FOR AUTOMOTIVE ETHERNET

REV V1.10

裕太微电子
Motorcomm

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Revision History

Revision	Release Date	Summary
0.1		Draft
1.0		Update register table
1.01	2020/03/17	Modify Error
1.02	2021/01/04	Add power consumption, sleep/wake-up description. Correct product name from YT8010 to YT8010A Correct 3.2 TRP/TRN pin names Update 7 AC/DC characteristics Update 6 register table，remove and add some registers Update 9.2 mechanical information Correct some function descriptions Update 5.3 XMII diagram
1.03	2021/01/11	Update 3.2 pin name and description Correct 5.1 software reset description Update 6.2.1 internal loopback register description Update 7.2 absolute max ratings Update 10 ordering information
1.04	2021/05/17	Modify 7.10 RMII T_iphd_tx_rmii min. value from 2ns to 3ns
1.05	2021/09/02	Delete IEC61000-4-2 ESD test level since it depends on board design
1.06	2022/03/09	Add revision summary section information. Modify 5.1 RESET_N time from 5us to 200us Modify 5.6 description Modify 5.8 Sleep Current to 20uA

		Modify 6.3.7 register 0x4000 bit6-0 definition
1.07	2022/03/17	Modify 7.10 RMII timing to RMII1 and RMII2 timing respectively. Add 8 max power consumption
1.08	2022/05/09	Add 8 RESET/SLEEP max power consumption
1.09	2022/11/03	Modify pin17 description,
1.10	2022/11/23	add RGMII/RMII/MII voltage description and strapping description

TABLE OF CONTENTS

1 GENERAL DESCRIPTION

The Motorcomm YT8010A is a single pair Ethernet physical layer transceiver (PHY) which implements the Ethernet physical layer portion of the 100BASE-T1 standard as defined by the IEEE 802.3bw task force. Ideally suited for a wide range of automotive applications, it is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a single balanced twisted pair.

Based on cutting-edge DSP technology, combing adaptive equalizers, echo canceller, ADCs, phase-locked loops, line drivers, encoders/decoders and all other required support circuitry at a 100Mbps data rate to achieve robust performance and exceed automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

The YT8010A is designed to be fully compliant with RGMII, RMII and MII interface specifications, allowing compatibility with industry-standard Ethernet media access controllers (MACs) and switch controllers.

The YT8010A delivers the most comprehensive automotive technology solution required by OEM and Tier 1 suppliers, meeting AEC-Q100 Grade 1 temperature range.

1.1 TARGET APPLICATIONS

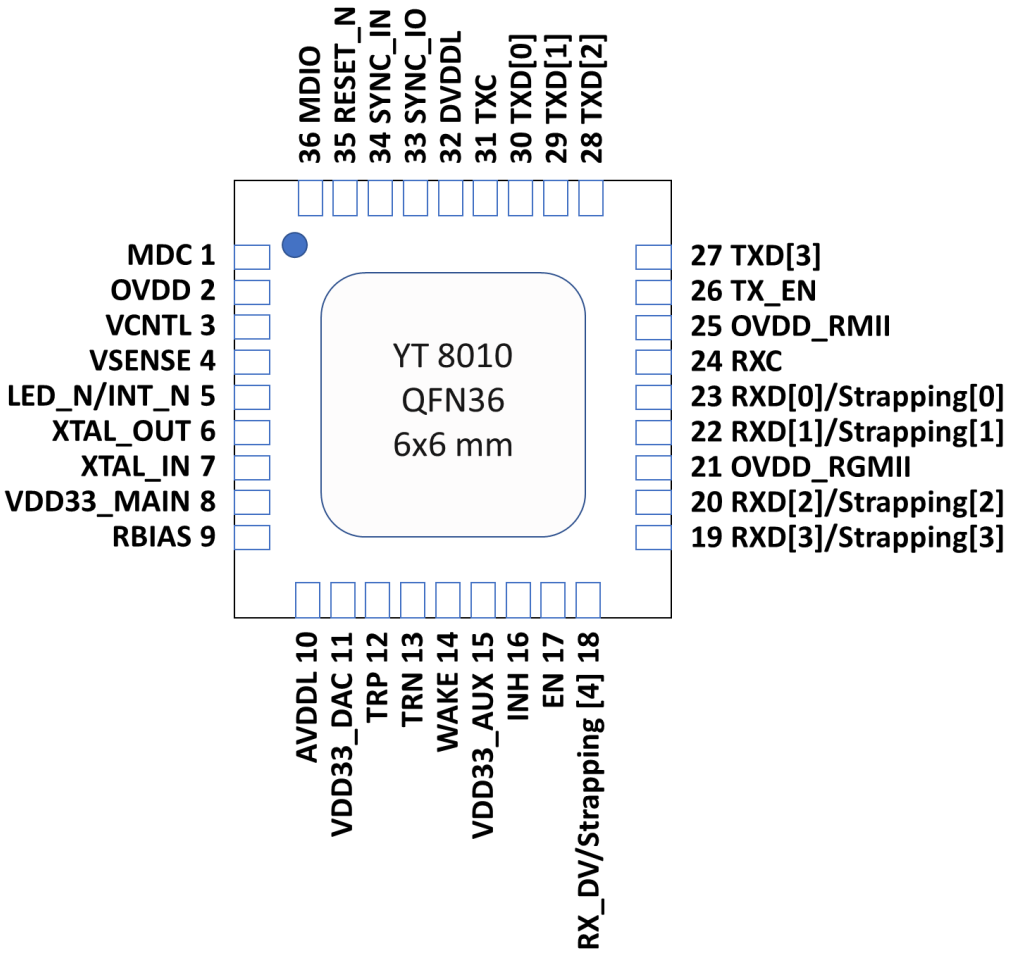
- Automotive infotainment systems
- Automotive diagnostics
- Advanced driver assistance systems
- Vehicle body control electronics

2 FEATURE

- 100BASE-T1 Transceiver
- 100BASE-T1 IEEE 802.3bw standards
- Full duplex
- Rapid linkup time
- Support auto cable detection and working mode selection.
- MII/RMII/RGMII support
- Selectable 3.3V/2.5V signaling for RGMII/RMII/MII
- RMII/RGMII interface EMI enhancement
- Support latency accommodation of RGMII clock
- Support IEEE 802.1AS
- Support Remote Wake up 3.3V analog supply.
- Advanced low-power management with local wake-up support
- Automotive Cable Diagnostics support
- Integrated LDO regulator allowing a single supply
- Internal/external/remote loopback mode for diagnosis
- MDI pins protected against ESD to 6kV HBM
- Jumbo frame supports up to 16 kB
- Polarity detection and auto/manual correction
- Integrated twisted-pair termination resistors
- AEC-Q100 Grade 1 (-40~125°C)
- Trace matched output impedance
- Integrated low-pass filter
- Robust cable ESD tolerance
- Package QFN 36, 6x6mm

3 PIN ASSIGMENT

3.1 YT8010A QFN36 6X6MM



3.2 PIN DESCRIPTIONS

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open-drain output
- OT = Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- CS = Continuously sampled
- ST = Schmitt trigger

- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = RGMII pin type
- A = Analog pin type

Pin No.	Symbol	Type	Description
1	MDC	I, ST	Management Data Clock. Only need to be effect during mdio operation.
2	OVDD	PWR, IO	2.5V or 3.3V for non-RGMII digital pads. When 2.5V is selected, RESET, MDIO, and LED pins are not 3.3V tolerant.
3	VCNTL	A	Vcontrol. Output point of an internal error amplifier. This pin shall be connected to the base of an external PNP power transistor.
4	VSENSE	A	Vsense. Sensing point of the external power transistor. This pin shall be connected to the external 1.2V power.
5	LED_N/INT_N	O, od	LED_N/INT_N Dual function pin. This pin is a dual function pin. It is active low.
6	XTAL_OUT	O/A	25 MHz Crystal Oscillator Output Pin. A continuous 25 MHz reference clock must be supplied to the chip by connecting a 25 MHz crystal between these two pins or by driving XTAL_IN with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTAL_OUT unconnected.
7	XTAL_IN	I/A	25 MHz Crystal Oscillator Input Pin.
8	VDD33_MAIN	PWR, I	3.3V power for the main core.
9	RBIAS	A	Bias Resistor. A 2.4 kΩ±1% resistor is connected between the RBIAS pin and GND
10	AVDDL	PWR, I	1.2V power for the analog.
11	VDD33_DAC	PWR, I	3.3V power for the DAC.
12	TRP	A	Transmit/Receive Pairs . Differential data from copper media is transmitted and received on the single TRD± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap supply.
13	TRN	A	
14	WAKE	I, pd	WAKE. Active-high. When in sleep mode, transitioning the WAKE pin from low to high will cause the PHY to exit the sleep mode.
15	VDD33_AUX	PWR, I	3.3V power for the auxiliary domain. This pin supplies power to the passive signal detect circuitry and must remain powered with 3.3V.

16	INH	O	Inhibit. Output to be connected to the LDO supplying power to the PHY. When entering sleep mode, INH will be pulled low and will disable the LDO. When exit sleep mode, INH will be pulled high and will enable the LDO
17	EN	I, pd	EN. This pin is used in conjunction with INH to enable sleep mode or to provide a local wakeup from sleep mode. Note: This pin must be pulled high via an external 4.7k resistor when you do not use EN function.
18	RX_DV/ Strapping[4]	IO, pd	Receive Data Valid. Active-high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid. Strapping[4]. Used as power on strapping[4] bit when reset is active.
19	RXD[3]/ Strapping[3]	IO, pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[3] is the most significant bit. Strapping[3]. Used as power on strapping[3] bit when reset is active.
20	RXD[2]/ Strapping[2]	IO, pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. Strapping[2]. Used as power on strapping[2] bit when reset is active.
21	OVDD_RGMII	PWR, I	2.5V or 3.3V for RGMII/RMII/MII IO. This pin is internally shorted with OVDD_RMII.
22	RXD[1]/ Strapping[1]	IO, pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. Strapping[1]. Used as power on strapping[1] bit when reset is active.
23	RXD[0]/ Strapping[0]	IO, pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[0] is the less significant bit. Strapping[0]. Used as power on strapping[0] bit when reset is active.
24	RXC	IO, pu	Receive Clock. 2.5M/25M output or input. This clock is used to synchronize the receive data outputs RXD[3:0]. The direction and frequency depend on MII mode and link mode.
25	OVDD_RMII	PWR, I	2.5V or 3.3V for RGMII/RMII/MII IO. This pin is internally shorted with OVDD_RGMII.
26	TX_EN	I, ST	Transmit Enable. Active-high. When TX_EN is asserted, the data on the

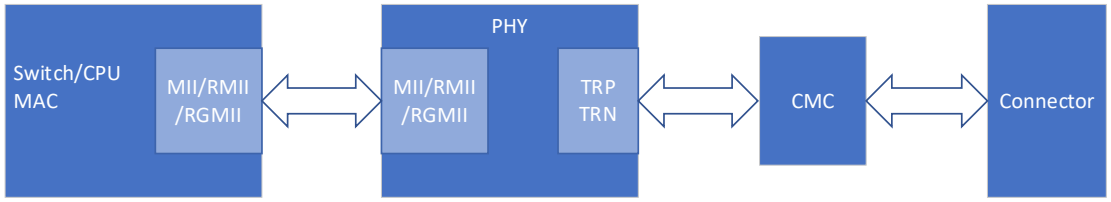
			TXD pins is encoded and transmitted.
27	TXD[3]	I, pd	Transmit Data Input. Data is input synchronously with TXC clock.
28	TXD[2]	I, pd	Transmit Data Input. Data is input synchronously with TXC clock.
29	TXD[1]	I, pd	Transmit Data Input. Data is input synchronously with TXC clock.
30	TXD[0]	I, pd	Transmit Data Input. Data is input synchronously with TXC clock.
31	TXC	IO, pd	Transmit Clock. 2.5M/25M/50M output or input. This clock is used to synchronize the transmit data inputs TXD[3:0]. The direction and frequency depend on MII mode and link mode.
32	DVDDL	PWR, I	1.2V input for digital core
33	SYNC_IO	IO, pd	802.1AS Frame Sync event/sync pulse input or output
34	SYNC_IN	I, ST	802.1AS Frame Sync event/sync pulse input.
35	RESET_N	I, pu	RESET. Active-low, reset pin for chip.
36	MDIO	IO, pu	Management Data I/O. This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.

3.3 STRAPPING PINS SETTING

Pin No	Pin Name	Type	Description
18	RX_DV/Strapping[4]	IO,PD	PHY Address configuration: PHYAD = Strapping[4] + 1'b1
19	RXD[3]/Strapping[3]	IO,PD	Master/Slave configuration: Pull high: Master Pull low: Slave
20	RXD[2]/Strapping[2]	IO,PD	xMII mode configuration: Strapping[2:0]: 3'b000: MII (Default) 3'b001: RMII2 (REF_CLK output) 3'b010: RMII1 (REF_CLK input) 3'b100: REMII (Reverse MII) 3'b110: RGMII 3'b111: Scan mode (for internal test) Other: Reserved
22	RXD[1]/Strapping[1]	IO,PD	
23	RXD[0]/Strapping[0]	IO,PD	

4 FUNCTION DESCRIPTION

4.1 APPLICATION DIAGRAM



4.2 MII INTERFACE

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 100BASE-T1 mode. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8010A supports a subset of MII signals. This subset includes all MII signals except TX_ER, RX_ER, CRS and COL.

4.3 RMII INTERFACE

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by clocking data on both the rising and falling edge of the transmit clock.

4.4 RGMII INTERFACE

Reduced gigabit media-independent interface (RGMII) is a standard interface between Gigabit MAC and Gigabit PHY. which is used to connect a PHY to a MAC. It is a parallel bus by clocking data on both the rising and falling edges of the clock. The clock frequency is adaptive to the speed of MAC and PHY link speed so that it can work in 1000/100/10Mbps modes. For YT8010A, RGMII only works at 100Mbps mode since it only supports 100BASE-T1.

4.5 MANAGEMENT INTERFACE

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 25 MHz.

4.6 DAC

The digital-to-analog converter (DAC) transmits PAM3, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

4.7 ADC

Receive channel has its own analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

4.8 ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog-to-digital converter (ADC) on each

channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

4.9 ECHO-CANCELLER

The echo impairment is caused on each channel because of the bidirectional transceiver in 100BASE-T1 mode. An echo canceller is added to remove this impairment from the ADC output. The echo canceler coefficients are adaptive to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

4.10 CLOCK RECOVERY

The clock recovery block creates the transmit and receive clocks for 100BASE-T1 the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is

configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo.

4.11 LINK MONITOR

Description about link status in different working mode.

In 100BASE-T1 mode, after receiver synchronizes to link partner's transmit signal and finishes local training process, local receive status will be good. Phy will monitor local receive status continuously. Local receive status should be good for at least 1.8us in 100BASE-T1 mode, then link monitor enters link pass status. Accordingly, if Local receive status is bad then link monitor enters link fail status immediately. Link status can be read in mii reg address 0x1h, bit2.

4.12 POLARITY DETECTION AND AUTO CORRECTION

YT8010A can detect and correct swapping of wires within a pair.

5 OPERATIONAL DESCRIPTION

5.1 RESET

YT8010A have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 200us to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up including wakeup from sleep mode.

RESET_N is also used as enable for power on strapping. During RESET_N is active, YT8010A latches input value on RX_DV and RXD[3:0] as strapping[4:0]. Strapping[4:0] is used as configuration information which provides flexibility in application without mdio access.

YT8010A also provides one software reset control register which are used to reset all internal logic except some mdio configuration registers. Configure mii register (address 0x0.bit15) to 1 to enable software reset. These bit is self-clear after reset process is done. For detailed information, please refer to the register table.

5.2 PHY ADDRESS

For YT8010A, Strapping[4] is used to generate phy address. Phy address is Strapping[4]+1. For example, if strapping[4] is 1'b1, then phy address is 2.

YT8010A always responses to phy address 0. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0x0) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0x0) is enable control for broadcast phy address and its default value is 1'b1.

5.3 XMII INTERFACE

YT8010A support 4 kinds of MII related interfaces: MII, RMII, RGMII and REMII.

5.3.1 MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 100BASE-T1 mode. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8010A supports a subset of MII signals. This subset includes all MII signals except TX_ER, RX_ER, CRS and COL. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

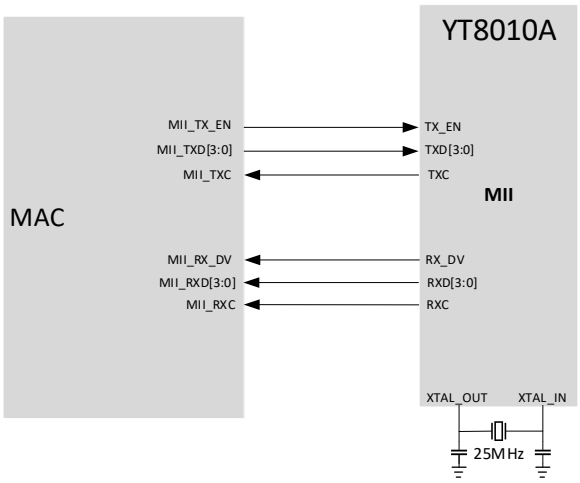


Figure 1 . connection diagram of MII

5.3.2 RMII

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF_CLK, TX_EN, TXD[1:0], RX_DV and RXD[1:0]. In YT8010/YT8050, we use TXC as REF_CLK. For 100M application, REF_CLK is 50MHz; for 10M application,

REF_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles. YT8010A supports two types of connection method:

1. RMII1 mode: TXC 50MHz is sent by MAC (MAC should be set to TXC output).

2. RMII2 mode: TXC 50MHz is sent by PHY (MAC should be set to TXC input).

The above RMII1/2 modes are set by hardware strapping pins.

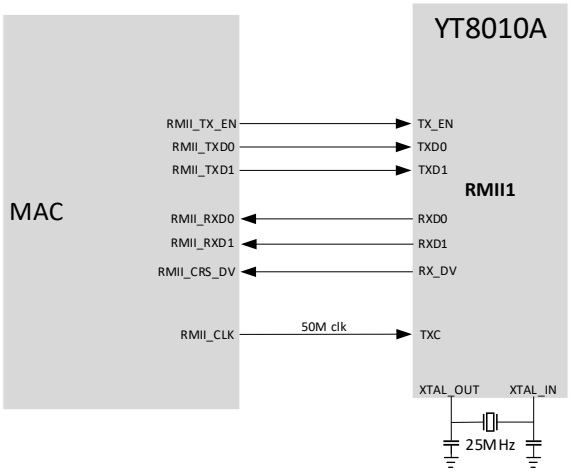


Figure 2 .connection diagram of RMII1

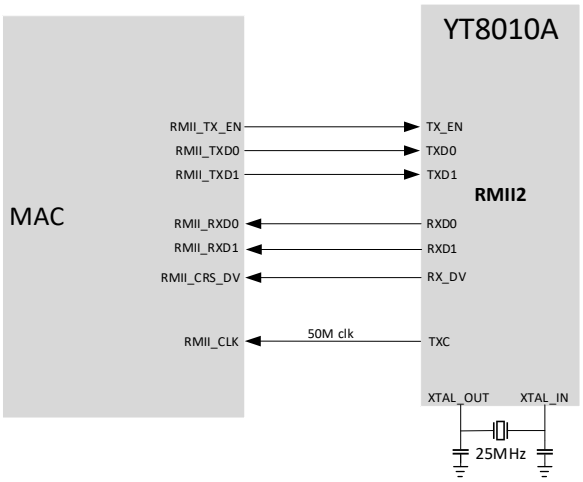


Figure 3 .connection diagram of RMII2

5.3.3 RGMII

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by tx_en/rx_dv on the falling edge of clock. TXD[3:0] and RXD[3:0] will

be duplicated on both rising and falling edge of clock. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz.

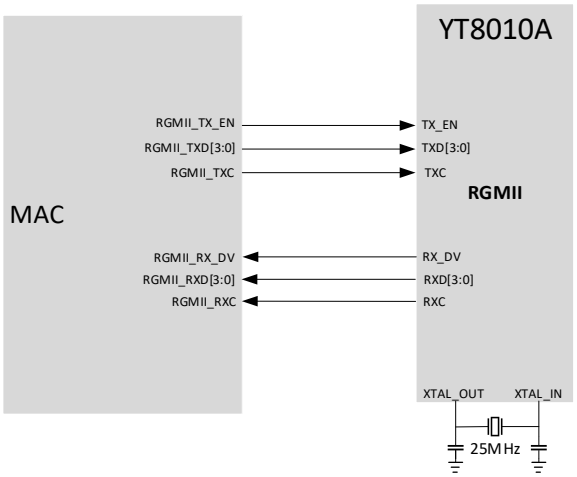


Figure 4 .connection diagram of RGMII

5.3.4 REMII INTERFACE

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two phys.

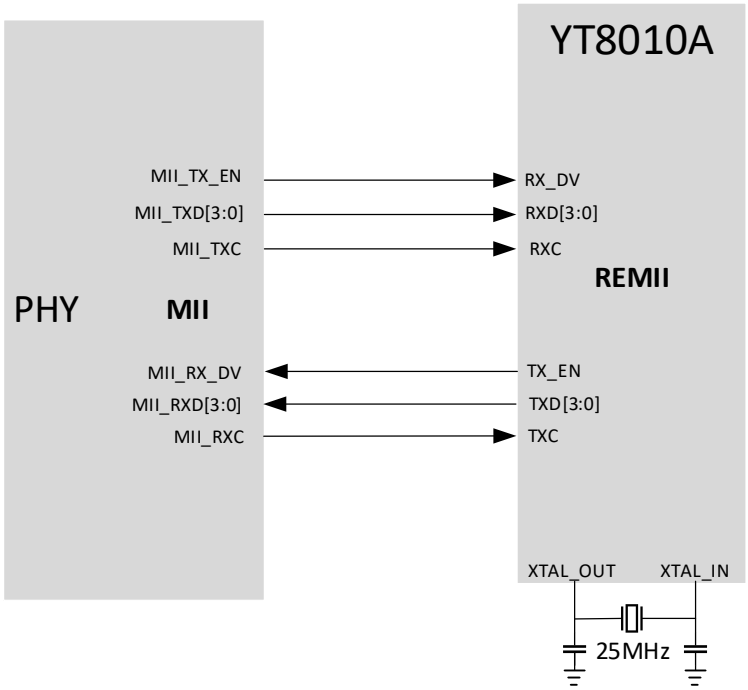


Figure 5 .connection diagram of REMII

5.4 SQI

YT8010A provides a method to monitor quality of link.

By reading extended register mse(address 0h1005), we can obtain SNR during following steps.

a) Read register mse[14:0]

b) Calculate SNR = 10*log10(32768/(3*mse))

c) Average over 200 readings A= avg(SNR)

d) Rank the link quality

i. SQI = 5 when A > 25

ii. SQI = 4 when 23 < A < 25

iii. SQI = 3 when 21 < A < 23

iv. SQI = 2 when 19 < A < 21

v. SQI = 1 when 17 < A < 19

vi. SQI = 0 when A < 17

5.5 LOOPBACK MODE

There are three loopback modes in YT8010A.

5.5.1 INTERNAL LOOPBACK

In Internal loopback mode, YT8010A feed transmit data to receive path in chip.

Configure bit 14 of mii register (address 0h0) to enable internal loopback mode. For 100BaseT1

YT8010A feeds digital pcs transmit data to pcs receiver directly.

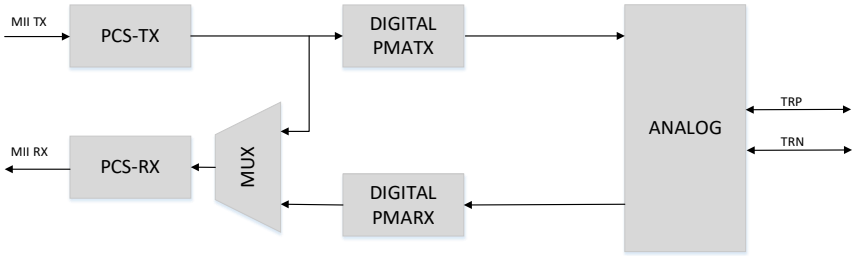


Figure 6 . Internal loopback

5.5.2 EXTERNAL LOOPBACK

In external loopback mode, YT8010A feed transmit data to receive path out of chip. For 100 BASE-T1 configure bit 12 of extended register(address 0h4000) and just leave TRP/N unconnected.

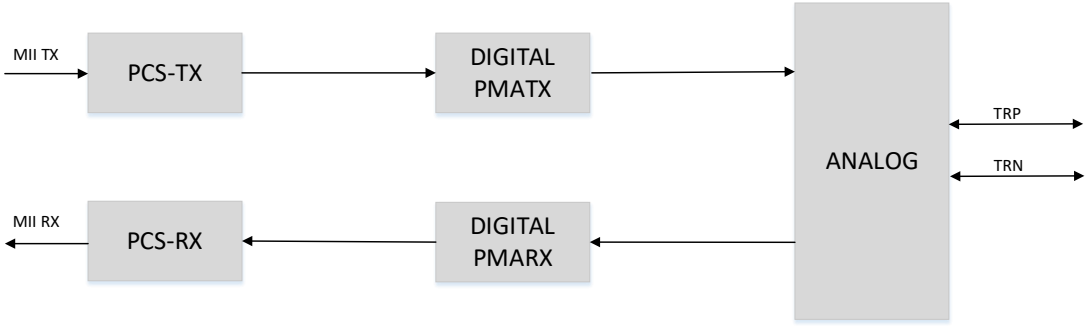


Figure 7 . external loopback

5.5.3 REMOTE LOOPBACK

In remote loopback mode, YT8010A feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

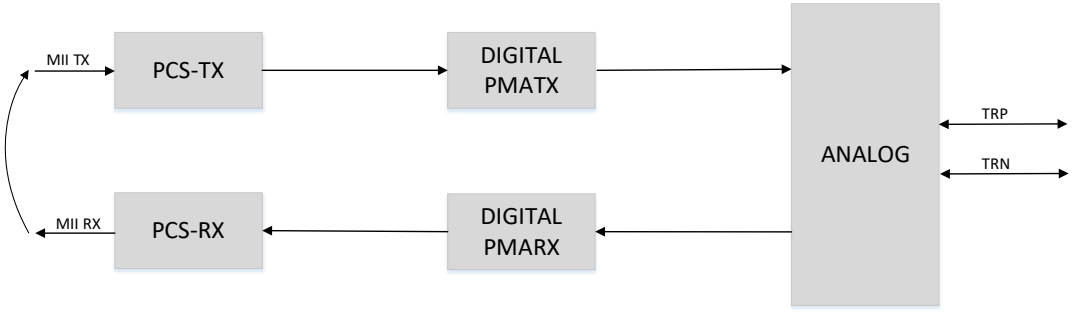


Figure 8 . remote loopback

5.6 MASTER-SLAVE CONFIGURATION

Master and slave configuration is from hardware strapping or configured by bit 9 of extended register(address 0xh1000).

5.7 INTERRUPT

Interrupt shares the same pin with LED.

Interrupt function can be selected by configuring bit 14 of extended register (address 0xh4001). Interrupt and led pin is open drain output and should be pulled up on board. It is low active

Every interrupt event has a corresponding mask bit and interrupt enable bit. Please refer to mii register map (address 0h12, 0h13, 0h16 and 0h17) for detailed information.

5.8 POWER SAVING

YT8010A supports standby mode and sleep mode to save power.

In standby mode, PHY turn off analog ADC, DAC, and PLL. All digital logic is gated except MDIO register access. INH pin is high and power supply is still on. The link is down in standby mode, YT8010A can recover from standby mode rapidly. Write bit 11 of mii address 0x0h to 1'b1 to enter standby mode. To exit standby mode, write the same bit to 1'b0.

In sleep mode, PHY turn off all power supply except always on 3.3v supply. The only working block is analog INH generation circle and signal detect circle. In this mode, INH pin is low. There are three ways to enter sleep mode:

1. Pull down local EN pin from high.

2. Write bit12 of extended 0x1007 register.

3. Use TC10 standard to control remote phy to enter sleep mode.

There are also three ways to exit sleep mode:

1. Pull up local En pin from low.

2. Pull up local Wake pin from low.

3. Inject wake up signal at TRP/TRN for more than 100us to wake up phy remotely.

Please refer to following chapter for detailed information about remote control. In sleep mode, the current consumption of YT8010A is less than 20uA.

5.9 APPLICATION NOTES ABOUT SLEEP MODE

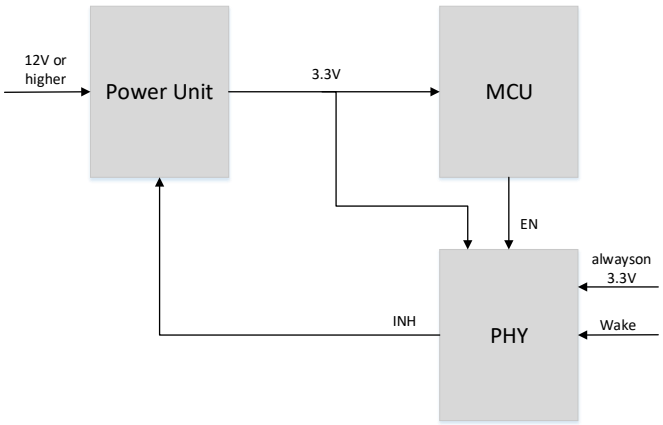


Figure 9. Hardware connection description (MCU don't support Sleep and Wakeup function)

When MCU don’t support sleep and wakeup function, YT8010A can take the responsibility of power control. If MCU decides to enter sleep mode,it can pull down EN pin or configure sleep_mode_en register through mdio, then INH goes down and power supply for MCU and phy will turn off except always on 3.3V power supply. The whole system can be wakeup remotely by injecting wakeup pulse on TRP/TRN or pulling up wake pin.

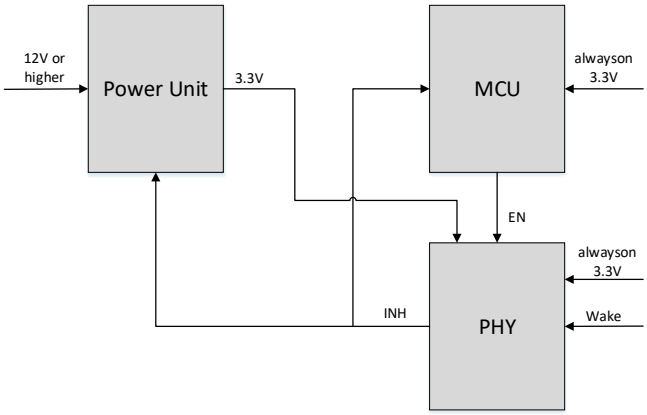


Figure 10. Hardware connection description (MCU support Sleep and Wakeup function)

When MCU support sleep and wakeup function, INH pin only control the power supply of phy. If MCU decides to enter sleep mode, it can pull down En pin or configure

sleep_mode_en register through mdio, then INH goes down and power supply for phy will turn off except always on 3.3V power supply. MCU can pull up En/Wake pin to wakeup phy or phy will be wakeup remotely and send out a wake interrupt to MCU.

Following is an example of INH control application. Only AVDD_PPD is connected to always on 3.3V power and other power pins are controlled by INH pin.

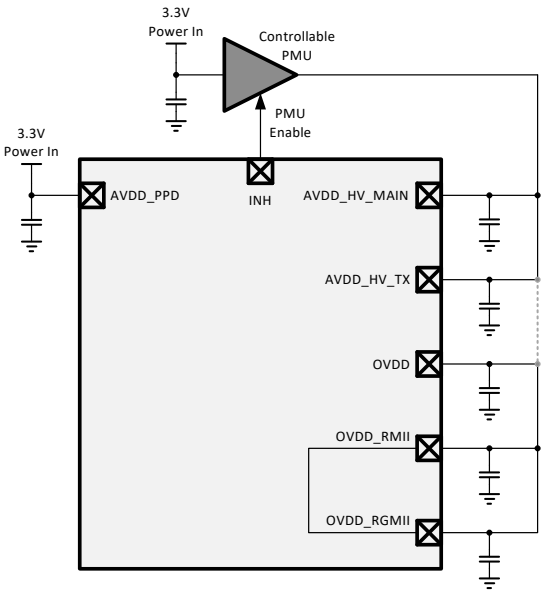


Figure 11. Power solution for INH control

5.10 SLEEP NEGOTIATION PROCESS

YT8010A Support OPEN TC10 standard. Following figure gives the state transition in sleep negotiation process。

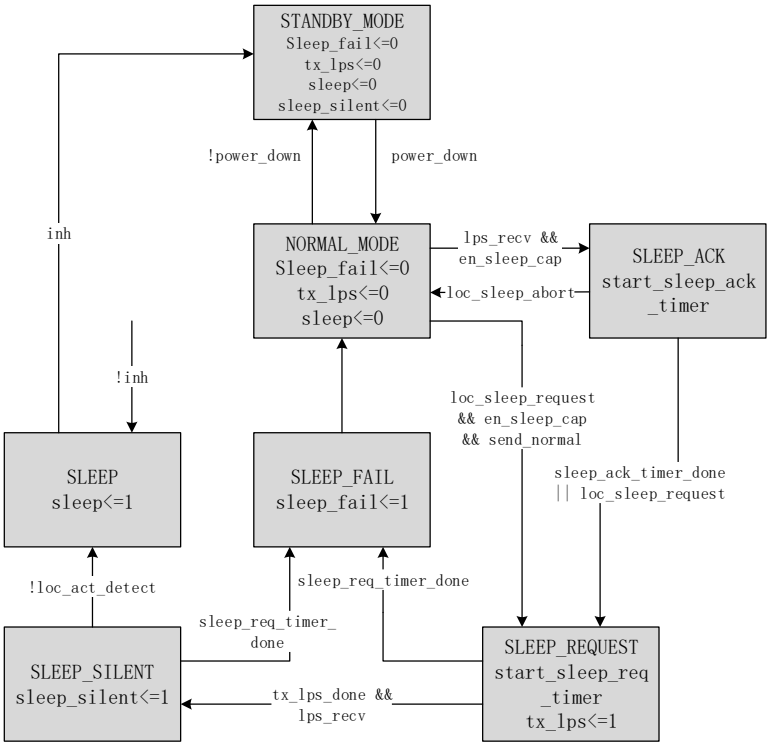


Figure 12. State diagram in sleep negotiation process

After YT8010A is power up, it enters standby mode. Power down register control the Translation between Standby mode and Normal mode. Default value of Power down register is zero, phy will enter normal mode directly without MCU.

Phy can start sleep negotiation process after link is set up between two phys.

Initiator configures loc_sleep_request register to start sleep negotiation process. Then Initiator enter SLEEP_REQUEST state and send LPS pattern and enable sleep_req_timer(16ms). Responder receive LPS pattern and enter SLEEP_ACK state, enable sleep_ack_timer(8ms) and send out interrupt to MCU to inform that sleep request is received. In SLEEP_ACK state, phy wait response form MCU。MCU can accept the sleep request by configuring loc_sleep_request or reject by configuring loc_sleep_abort. If there is no response from MCU before sleep_ack_timer done, Responder will think sleep request is accepted and enter SLEEP_REQUEST state. If Responder rejects sleep request, Initiator will enter SLEEP_FAIL state after sleep_req_timer done and sleep negotiation process is done. If Responder accepts sleep request, Responder will send LPS pattern to inform initiator. After received LPS pattern from Responder, Initiator enters SLEEP_SILENT state and stops sending any signal on txp/txn and keeps checking signal energy on TRP/TRN. After the signal is gone, Initiator enters SLEEP_MODE state. In the meanwhile, responser enters SLEEP_SILENT state after LPS

pattern is sent and keeps checking signal energy on txp/txn. After the signal is gone, Responder enters SLEEP_MODE state and sleep negotiation process is done.

Following figures give out the process of sleep negotiation.

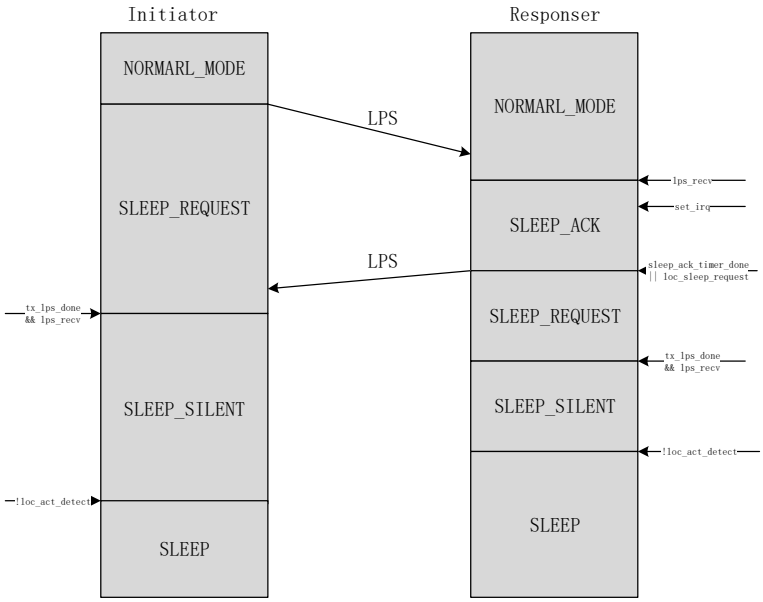


Figure 13. Process of successful sleep negotiation

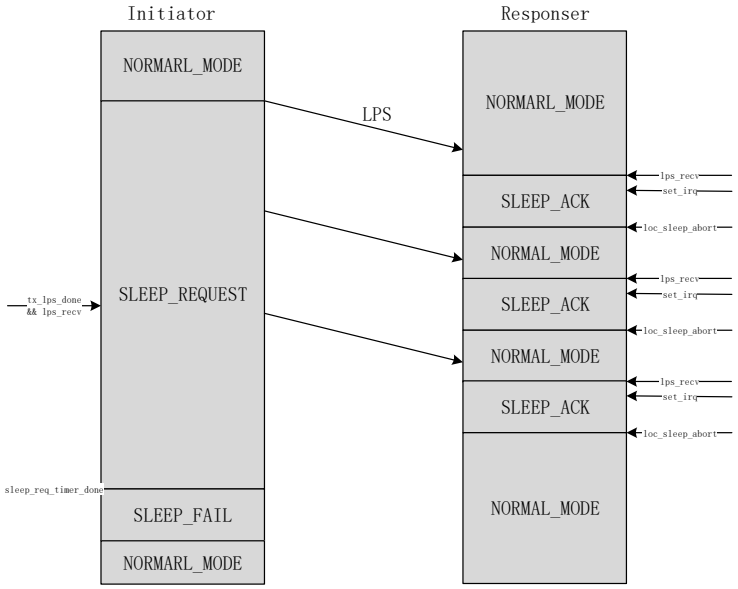


Figure 14. Process of failed sleep negotiation

5.11 REMOTE WAKEUP

YT8010A can send wakeup pulse to wakeup link partner remotely if link partner support remote wakeup. YT8010A can also wakeup by wake up pulse sent by link partner.

To send out wakeup pulse to link partner, configure link_control to 0 and loc_wake_req to 1 in NORMARL_MODE. YT8010A will send 1ms wakeup pulse (IDLE symbol) to wake up link_partner。

If link is already setup, configure loc_wake_req to 1. YT8010A will send 128bits wake up request to link partner. YT8010A will send an interrupt to inform MCU after received wake up request from link partner.

6 REGISTER OVERVIEW

6.1 MII MANAGEMENT INTERFACE CLAUSE 22 REGISTER PROGRAMMING

The YT8010A transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

Clock is driven from MDIO controller to the MDC pin of the YT8010. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

6.2 MII REGISTERS

6.2.1 MII REGISTER 00H: BASIC CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	1'b0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	1'b0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback

13	Reserved	RO	1'b1	Reserved
12	Reserved	RO	1'b1	Reserved
11	Power_down	RW SWC	1'b0	1 = Power down 0 = Normal operation
10	Isolate	RW SWC	1'b0	Isolate phy from MII/GMII/RGMII: PHY will not respond to RGMII TXD/TX_CTL, and present high impedance on RXD/RX_CTL. 1'b0: Normal mode 1'b1: Isolate mode
9	Reserved	RO	1'b0	Reserved
8	Reserved	RO	1'b1	Reserved
7	Reserved	RO	1'b0	Reserved
6	Reserved	RO	1'b1	Reserved
5:0	Reserved	RO	5'b0	Reserved

6.2.2 MII REGISTER 01H: BASIC STATUS REGISTER

Bit	Symbol	Access	Default	Description
2	Link_Status	RO LL SWC	1'b0	Link status 1'b0: Link is down 1'b1: Link is up
1	Jabber_Detect	RO RC LH SWC	1'b0	10Baset1 jabber detected 1'b0: no jabber condition detected 1'b1: Jabber condition detected

6.2.3 MII REGISTER 02H: PHY IDENTIFICATION REGISTER1

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	16'b0	Bits 3 to 18 of the Organizationally Unique Identifier

6.2.4 MII REGISTER 03H: PHY IDENTIFICATION REGISTER2

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	6'b0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	6'h30	For motor phy, 30
3:0	Revision_No	RO	4'h9	4 bits manufacturer's revision number

6.2.5 MII REGISTER 0FH: EXTENDED STATUS REGISTER

Bit	Symbol	Access	Default	Description

15	1000Base-X_Fd	RO	1'b0	PHY not able to support 1000Base-X_Fd
14	1000Base-X_Hd	RO	1'b0	PHY not able to support 1000Base-X_Hd
13	1000Base-T_Fd	RO	1'b0	PHY not able to support 1000Base-T_Fd
12	1000Base-T_Hd	RO	1'b0	PHY not able to support 1000Base-T_Hd
11:8	Reserved	RO	1'b0	Reserved
7	100Base-T1	RO	1'b1	PHY able to support 100Base-T1
6	1000Base-T1	RO	1'b0	PHY not able to support 1000Base-T1
5:0	Reserved	RO	6'b0	Reserved

6.2.6 MII REGISTER 12H: INTERRUPT MASK REGISTER

Bit	Symbol	Access	Default	Description
11	Link_Failed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
10	Link_Succeed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
9	IEEE1588_Misc_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
8	IEEE1588_Rx PTP_message_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
7	IEEE1588_Tx PTP_message_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
0	Jabber_Happened_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable

6.2.7 MII REGISTER 13H: INTERRUPT STATUS REGISTER

Bit	Symbol	Access	Default	Description
11	Link_Failed_INT	RO RC	1'b0	1 = Link down takes place 0 = No link down takes place
10	Link_Succeed_INT	RO RC	1'b0	1 = Link up takes place 0 = No link up takes place
9	IEEE1588_Misc_INT	RO RC	1'b0	1 = IEEE1588 module's MISC interrupt happened 0 = IEEE1588 module's MISC interrupt didn't happen
8	IEEE1588_Rx_PTP_message_INT	RO RC	1'b0	1 = PHY received 1588 message 0 = PHY didn't receive 1588 message
7	IEEE1588 Tx PTP message INT	RO RC	1'b0	1 = PHY transmitted 1588 message 0 = PHY didn't transmit 1588 message
0	Jabber_Happened_INT	RO RC	1'b0	1 = 10BaseT T1 jabber happened

				0 = 10BaseT T1 jabber didn't happen

6.2.8 MII REGISTER 16H: INTERRUPT MASK REGISTER

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	7'b0	Always 0.
7	Link_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
6	Loc_rcvr_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
5	Rem_rcvr_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
4	Training_failed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
3	LPS_recv_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
2	Wake_recv_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
1	Sleep_fail_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable

6.2.9 MII REGISTER 17H: INTERRUPT STATUS REGISTER

Bit	Symbol	Access	Default	Description
7	Link_status_change_int	RO RC	1'b0	
6	Loc_rcvr_status_change_int	RO RC	1'b0	
5	Rem_rcvr_status_change_int	RO RC	1'b0	
4	Training_failed_int	RO RC	1'b0	
3	LPS_recv_int	RO RC	1'b0	
2	Wake_recv_int	RO RC	1'b0	
1	Sleep_fail_int	RO RC	1'b0	

6.2.10 MII REGISTER 1EH: DEBUG REGISTER'S ADDRESS OFFSET REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Address_Offset	RW	16'h0	It's the address offset of the extended register that will be Write or Read

6.2.11 MII REGISTER 1FH: DEBUG REGISTER'S DATA REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Datas	RW	16'b0	It's the data to be written to the

				extended register indicated by the address offset in register 0x1E, or the data read out from that debug register.

6.3 EXTENDED REGISTERS

6.3.1 EXTENDED REGISTER 1000H: BASIC AUTO100 CONTROL1

Bit	Symbol	Access	default	Description
15	Link_control	RW	1'b1	Link control. 0: disable; 1: enable
14	Transmit_Disable	RW	1'b0	Transmit disable control. 1'b0: Normal operation; 1'b1: Disable transmit
13	Test_Mode_En	RW	1'b0	Switch to turn on test mode. 1'b0: disable test mode; 1'b1: enable test mode
12:10	Test_Mode	RW	3'b000	Test mode selection 3'b000: no test mode 3'b001: test mode 1 3'b010: test mode 2 3'b100: test mode 4 3'b101: test mode 5 Others: reserved
9	Pma_Config	RW	1'b0	PHY Master/Slave configuration 1'b0: Configured as Slave 1'b1: Configured as Master
7	Scrambler_Sync_Err_En	RW	1'b1	Enable scrambler sync err calculation 1'b0: disable data upload 1'b1: enable data upload
6	Uldata_rloopback	RW	1'b0	Still upload data in remote loopback mode 1'b0: disable 1'b1: enable
4	Super_Isolate	RW	1'b0	Isolate phy from MII/RMII/RGMII/REMII 1'b0: Normal mode 1'b1: Super_Isolate mode
3	Polar_Det_En	RW	1'b1	Cable polarity detect control in slave 1'b0: disable cable polarity detect 1'b1: enable cable polarity detect

6.3.2 EXTENDED REGISTER 1003H: BASIC AUTO100 STATUS1

Bit	Symbol	Access	Default	Description
15:0	Sym_Err_Cnt	RO/RC/SWC	16'b0	The symbol error counter is incremented when an invalid code symbol is received (including idle symbols). Only increase by one if more than one error in one frame

6.3.3 EXTENDED REGISTER 1004H: AUTO100 STATUS2

Bit	Symbol	Access	Default	Description
15	Loc_Rcvr_Status	RO SWC	1'b0	Local receiving status 1'b0: local receiving is down 1'b1: local receiving is ok
14	Rem_Rcvr_Status	RO SWC	1'b0	Local receiving status 1'b0: remote receiving is down 1'b1: remote receiving is ok
13	Scr_Locked	RO SWC	1'b0	Local scramble lock status 1'b0: local scramble lock is down 1'b1: local scramble lock is ok
12	Polarity_inv	RO SWC	1'b0	Polarity inversion status 1'b0: no polarity inversion detected 1'b1: polarity inversion detected
11	Interleave_Detect	RO SWC	1'b0	Interleave order of rx ternary symbols 1'b0: TAn, TBn 1'b1:TBn, TAn
10:6	Linkfail_Cnt	RO RC SWC	5'b0	Number of link fails
5	Ssd_Err	RO LH RC SWC	1'b0	Ssd status 1'b0: no ssd error detected 1'b1: ssd error detected
4	Esd_Err	RO LH RC SWC	1'b0	Esd error status 1'b0: no esd error detected 1'b1: esd error detected
3	Receive_Err	RO LH RC SWC	1'b0	receive error status 1'b0: no rx error detected 1'b1: rx error detected
2	Transmit_Err	RO LH RC SWC	1'b0	transmit error status 1'b0: no tx error detected 1'b1: tx error detected
1	Scr_Locked_Err	RO LH RC SWC	1'b0	Scr lost lock status 1'b0: no scr lost lock detected 1'b1: scr lost lock detected
0	Sym_Err	RO LH RC SWC	1'b0	Symbol err status

				1'b0: no symbol err detected 1'b1: symbol err detected

6.3.4 EXTENDED REGISTER 1005H: AUTO100STATUS3

Bit	Symbol	Access	default	Description
15	Reserved	RO	1'b0	Reserved
14:0	Mse	RO SWC	1'b0	mse value used to indicate the link quality

6.3.5 EXTENDED REGISTER 1006H: AUTO100 STATUS4

Bit	Symbol	Access	default	Description
15:8	Loc_Rcvr_cnt	RO RC SWC	8'b0	Number of times local receiver was not OK
7:0	Rem_Rcvr_cnt	RO RC SWC	8'b0	Number of times remote receiver was not OK

6.3.6 EXTENDED REGISTER 1007H: AUTO100 LOW POWER CONTROL

Bit	Symbol	Access	default	Description
15	Loc_Wake_Req	RW SC	1'b0	Transmit WUP or wake up command to link partner
14	Loc_Sleep_Req	RW SC	1'b0	Start LP handshake process
13	Loc_Sleep_Abort	RW SC	1'b0	Abort LP handshake process
12	Sleep_Mode_En	RW	1'b0	Enter sleep mode directly
11	En_Sleep_cap	RW	1'b0	Bypass LP handshake process
10	Bypass_Power_Control	RW	1'b0	Bypass whole power control management
9:4	Lps_recv_th	RW	6'd5	Lps command receive threshold
3:0	Wake_recv_th	RW	4'd10	Wake command receiver threshold

6.3.7 EXTENDED REGISTER 4000H: EXTENDED COMBO CONTROL1

Bit	Symbol	Access	default	Description
15:13	MII_mode	RW	3'b000	MII mode selection 3'b000: MII mode 3'b010: RMII1mode(refclk input) 3'b001: RMII2mode(refclk output) 3'b110: RGMII mode 3'b100: REMII mode(Reversed MII)

				Others: reserved
12	External_Loopback	RW	1'b0	External loopback control 1'b0: disable 1'b1: enable
11	Remote_Loopback	RW	1'b0	Remote loopback control 1'b0: disable 1'b1: enable
10:6	Reserved	RW	5'b0	Reserved
5	Jumbo_Enable	RW	1'b0	Enable Jumbo frame reception up to 18KB frame, when disabled only up to 4.5KB frame supported 0: disable jumbo frame reception 1: enable jumbo frame reception
4:0	Reserved	RW	5'b0	Reserved

6.3.8 EXTENDED REGISTER 4001H: EXTENDED PAD CONTROL

Bit	Symbol	Access	default	Description
15	Reserved	RO	1'b0	Reserved
14	Int_led_sel	RW	1'b0	1'b1: interrupt selected 1'b0: led selected
13:12	Xmii_dr_rgmii	RW	2'b11	Rgmii pad diver strength
11:8	Reserved	RO	4'b0	Reserved
7:6	Int_N_Led_Dr	RW	2'b11	Int_n_led pin driver strength control
5:4	Xmii_Dr	RW	2'b10	Xmii interface driver strength control
3:2	Mdio_Dr	RW	2'b11	Mdio pin driver strength control
1:0	Sync_Io_Dr	RW	2'b11	Sync_io pin driver strength control

6.3.9 EXTENDED REGISTER 4002H: EXTENDED CLOCK DELAY CONTROL

Bit	Symbol	Access	default	Description
15:12	Mii_Rxc_Delay_Sel	RW	4'd0	Rxc out delay sel
11:8	Mii_Txc_Delay_Sel	RW	4'd0	Txc in delay sel
7:4	Rgmii_Rxc_Delay_Sel	RW	4'd10	Rxc out delay sel
3:0	Rgmii_Txc_Delay_Sel	RW	4'd10	Txc in delay sel

7 TIMING AND AC/DC CHARACTERISTICS

7.1 DC CHARACTERISTICS

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
3.3V (optional) MDIO, MDC, RGMII I/O	3.3V RGMII/RMII/MII Supply Voltage	-	2.97	3.3	3.63	V
2.5V (optional) MDIO, MDC, RGMII I/O	2.5V RGMII/RMII/MII Supply Voltage	-	2.25	2.5	2.75	V
Voh (3.3V)	High Level Output Voltage	-	2.4	-	3.6	V
Voh (2.5V)	High Level Output Voltage	-	2	-	2.8	V
Vol (3.3V)	Low Level Output Voltage	-	-0.3	-	0.4	V
Vol (2.5V)	Low Level Output Voltage	-	-0.3	-	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	-	2	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	-	0.8	V
Vih (2.5V)	Minimum High Level Input Voltage	-	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	-	0.7	V

7.2 ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Unit
VDD33	3.3 V power supply	-0.3	3.80	V
AVDDL	1.2 V power supply	-0.3	1.40	V
DVDDL	1.2 V power supply	-0.3	1.40	V
Maximum Junction Temperature			150	°C

7.3 RECOMMENDED OPERATING CONDITION

Description	Pins	Min	Typical	Max	Unit
Power supply	VDD33	2.97	3.30	3.63	V
	AVDDL	1.08	1.20	1.32	V
	DVDDL	1.08	1.20	1.32	V
Ambient Operation Temperature Ta		-40	-	125	°C

7.4 CRYSTAL REQUIREMENT

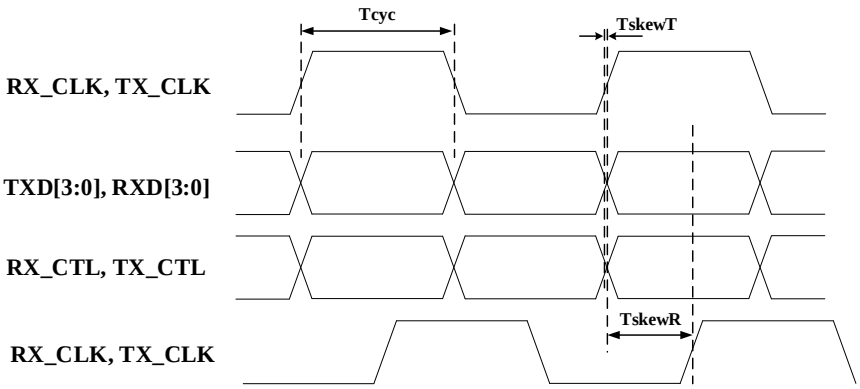
Symbol	Description	Min	Typ	Max	Unit
F ref	Crystal Reference Frequency	-	25	-	MHz
F ref Tolerance	Crystal Reference Frequency tolerance	-50	-	50	ppm
Duty Cycle	Reference clock input duty cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.4	V

7.5 OSCILLATOR/EXTERNAL CLOCK REQUIREMENT

Parameter	Condition	Min	Typ	Max	Unit
Frequency		-	25	-	MHz

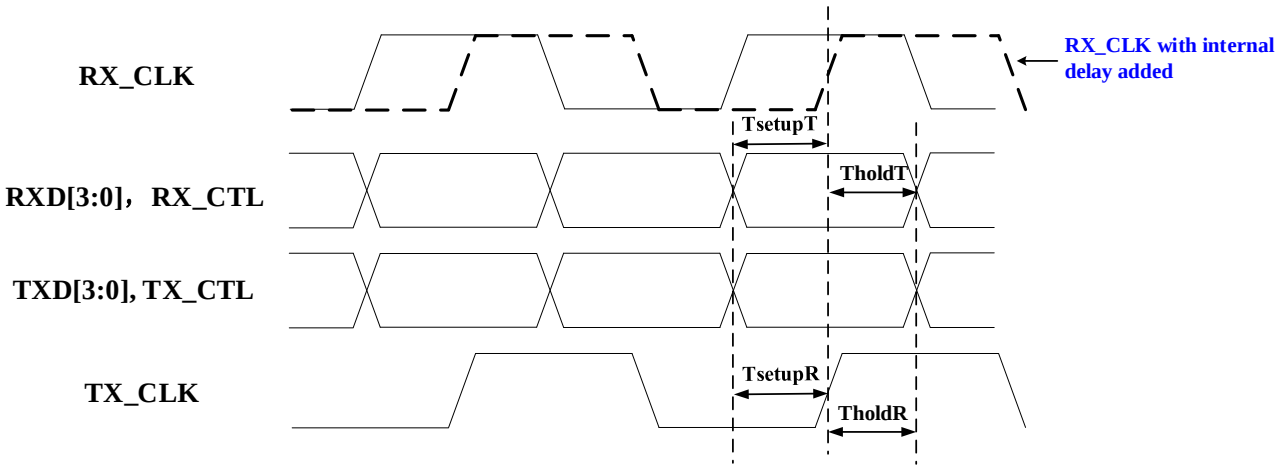
Frequency tolerance	Ta= -40~125 C	-50	-	50	PPM
Duty Cycle		40	-	60	%
Peak to Peak Jitter		-	-	200	ps
Vih		1.4		AVDD33+0.3	V
Vil		-	-	0.4	V
Rise Time	10%~90%	-	-	10	ns
Fall Time	10%~90%	-	-	10	ns
Temperature Range	YT8010A	-40	-	125	°C

7.6 RGMII TIMING W/O DELAY



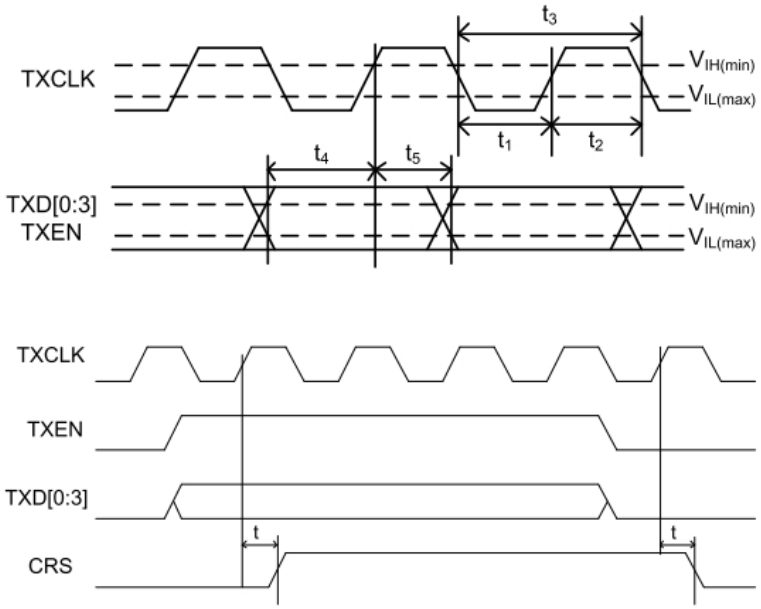
Symbol	Parameter	Min	Typical	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	-500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	-	-	ns
Tcyc	Clock cycle duration	36.0	40.0	44.0	ns
Duty_T	Duty cycle for 100MF	40	50	60	%

7.7 RGMII TIMING WITH INTERNAL DELAY



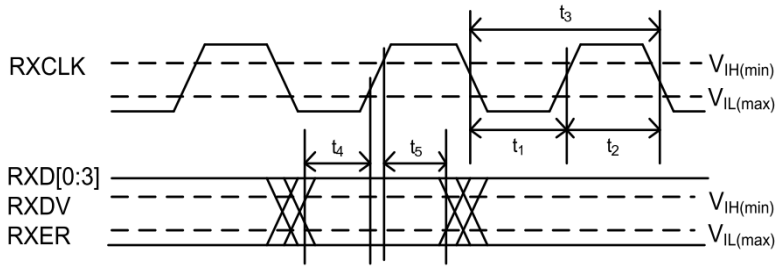
Symbol	Parameter	Min	Typical	Max	Unit
TsetupT	Data to Clock output Setup time(at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TholdT	Clock to Data output Hold time(at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TsetupR	Data to Clock input setup time (at Receiver — integrated delay)	1.0	2.0	-	ns
TholdR	Clock to Data input hold time (at Receiver — integrated delay)	1.0	2.0	-	ns

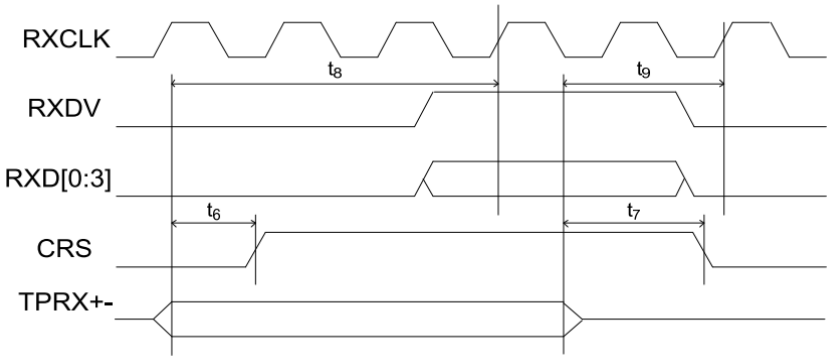
7.8 MII TRANSMISSION CYCLE TIMING



Symbol	Description		Min	Typical	Max	Unit
t1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	TXEN, TXD[0:3]	100Mbps	10	-	-	ns
	Setup to TXCLK Rising Edge	10Mbps	5	-	-	ns
t5	TXEN, TXD[0:3]	100Mbps	0	-	-	ns
	Hold After TXCLK Rising Edge	10Mbps	0	-	-	ns
t6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

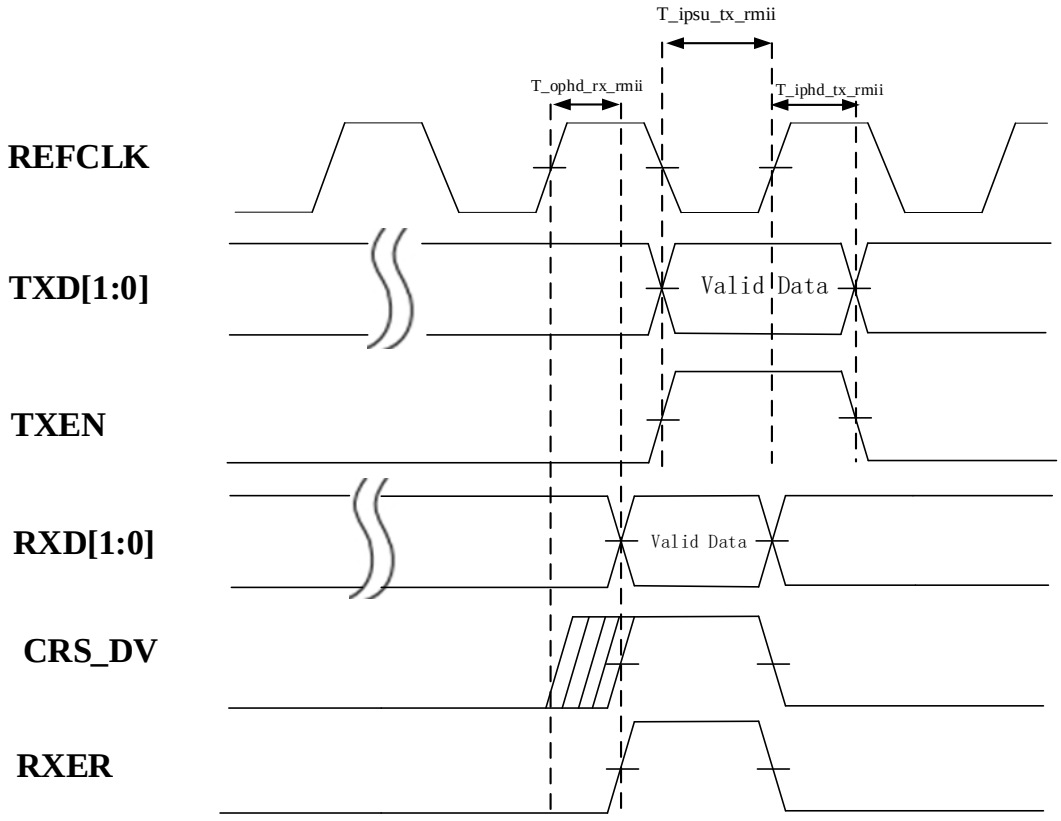
7.9 MII RECEPTION CYCLE TIMING





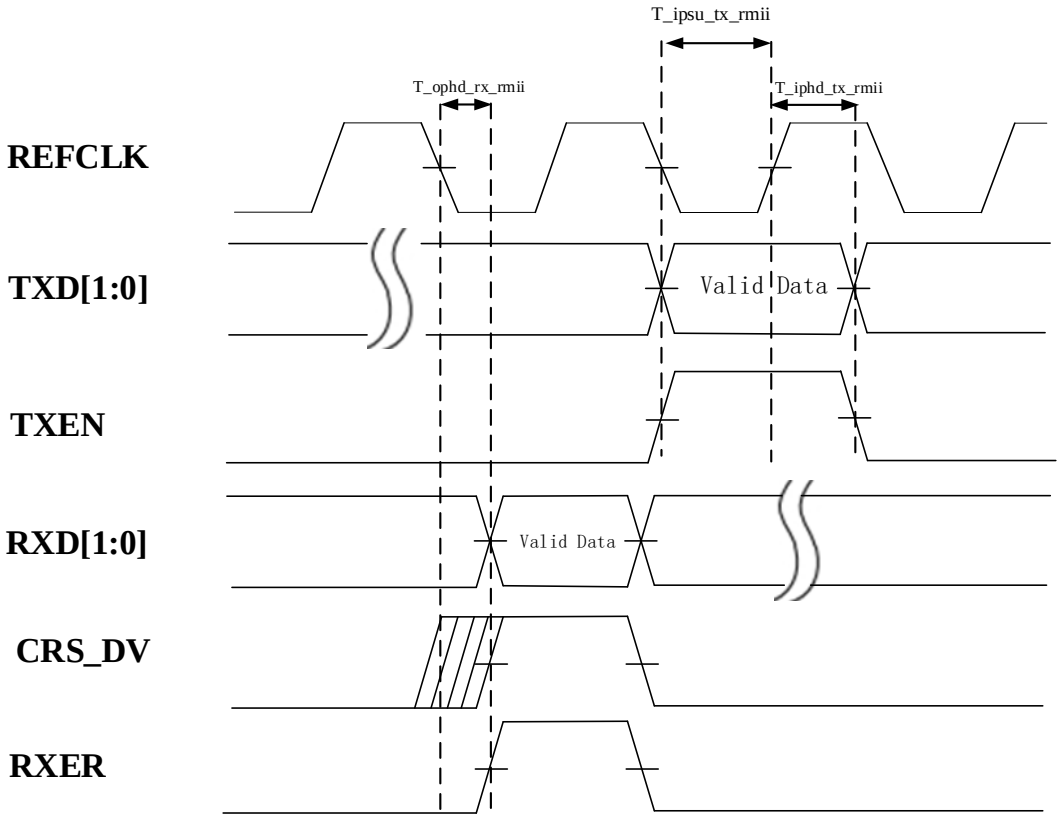
Symbol	Description		Min	Typical	Max	Unit
t1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	RXCLK Low Pulse Width RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	RXCLK Period RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	RXER, RX_DV,RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t5	RXER, RX_DV, RXD[0:3] Hold of RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t8	Receive Frame to Sampled Edge of RX_DV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t9	End of Receive Frame to Sampled Edge of RX_DV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

7.10 RMII1 TRANSMISSION AND RECEPTION CYCLE TIMING



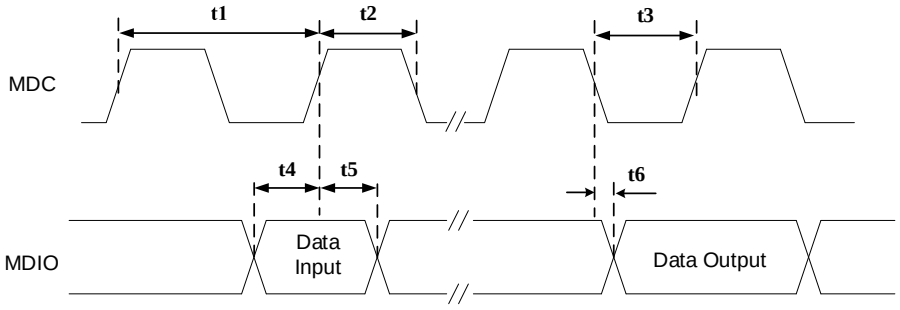
Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	6	-	12	ns

7.11 RMII2 TRANSMISSION AND RECEPTION CYCLE TIMING



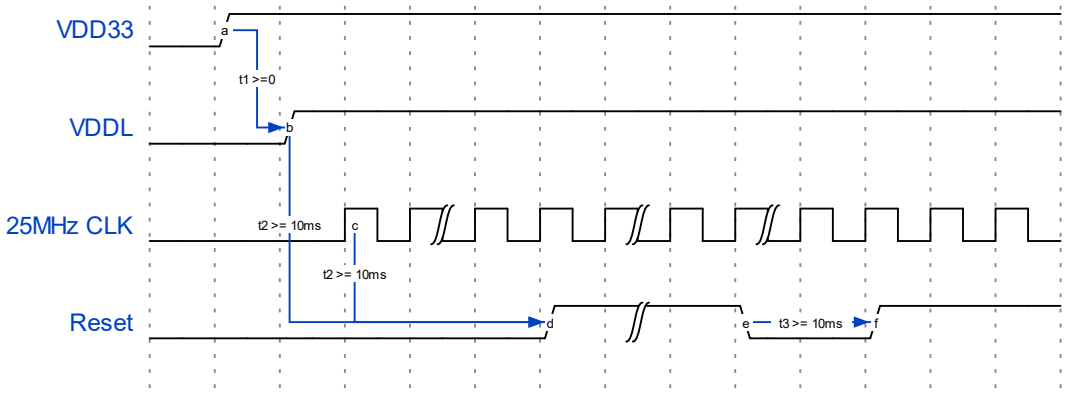
Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	0	-	3	ns

7.12 MDC/MDIO INTERFACE CHARACTERISTICS



Symbol	Description	Min	Typical	Max	Units
t1	MDC Clock Period	80	-	-	**ns**
t2	MDC High Time	32	-	-	**ns**
t3	MDC Low Time	32	-	-	**ns**
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	**ns**
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	**ns**
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

7.13 POWER ON SEQUENCE/CLOCK/RESET



When using crystal, the clock is generated internally after power is stable. For a reliable power on reset, suggest to keep asserting the reset low long enough (10ms) to ensure the clock is stable and clock-to-reset 10ms requirement is satisfied.

8 POWER REQUIREMENTS

Power consumption		
Mode	**Supply**	**Current (typical)**
Reset	3.3V	4.1mA
	1.2V	2.0mA
Traffic	3.3V	25.7mA
	1.2V	49.7mA
Sleep	3.3V	12uA

Note: Test by TT IC in RGMII mode with OVDD = 3.3V at 25℃ ambient temperature.

Max Power consumption		
Mode	**Supply**	**Current (typical)**
Reset	3.3V	4.9mA
	1.2V	2.4mA
Traffic	3.3V	30.2mA
	1.2V	58.3mA
Sleep	3.3V	15.3uA

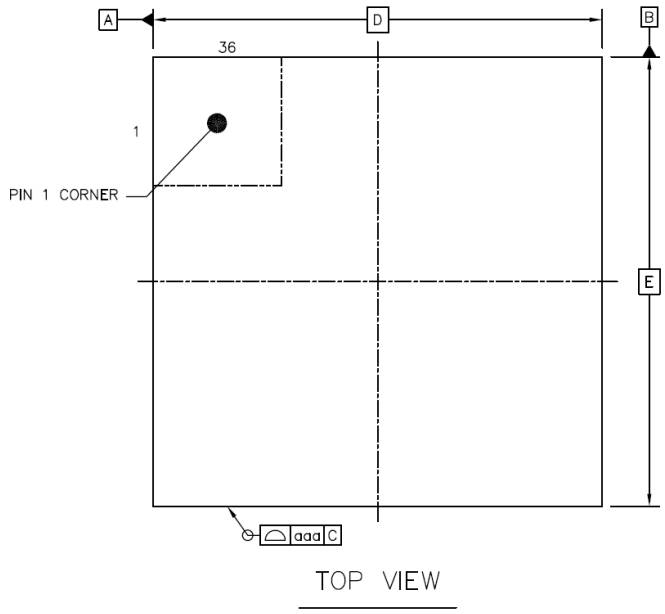
Note: Test by FF corner IC in RGMII mode with OVDD = 3.3V at 125℃ ambient temperature.

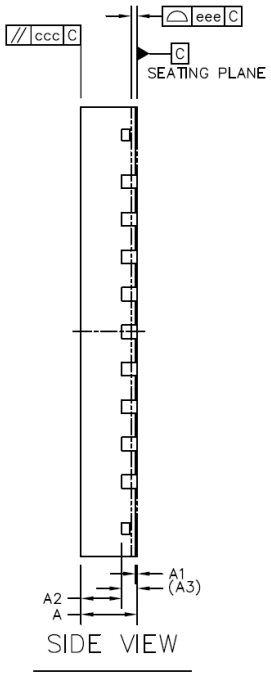
9 MECHANICAL AND THERMAL

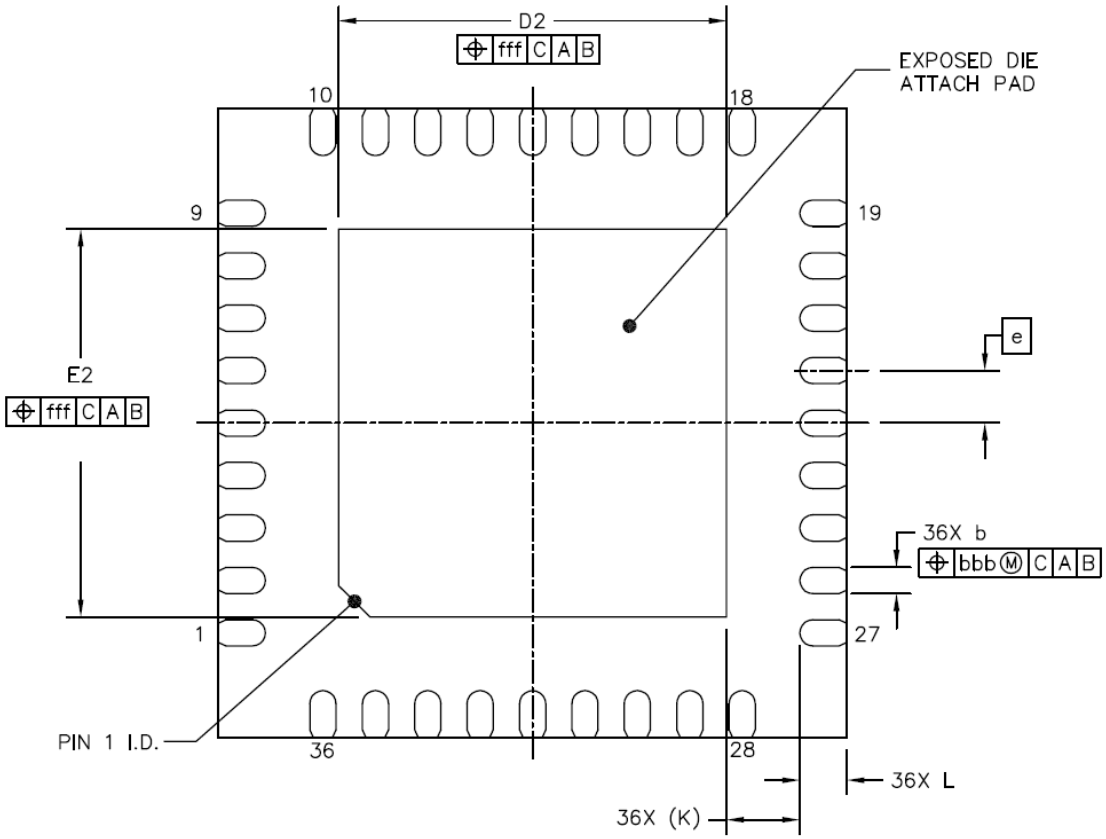
9.1 ROHS-COMPLIANT PACKAGING

Motorcomm offers an RoHS package that is compliant with RoHS.

9.2 MECHANICAL INFORMATION







BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.35	0.45	0.55
LEAD TIP TO EXPOSED PAD EDGE		K		0.7 REF.	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

9.3 THERMAL RESISTANCE

Symbol	Parameter	Conditon	Typ	Units
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=25°C	30	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow TA=125°C	26.1	°C/W
θ_{JC}	Thermal resistance - junction to case $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow	16.8	°C/W
θ_{JB}	Thermal resistance - junction to board $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	10.4	°C/W

10 ORDERING INFORMATION

Part Number	Package	Pack	Status
YT8010A	QFN36 6x6mm	3000ea Tape&Reel	Mass production