30V 125KHz 4A Fast-PWM Synchronous Step-Down Converter TD1372

General Description

The TD1372 is a fully integrated high efficiency synchronous step-down converter which requires minimum number of external components. It offers very compact solution with up to 4A continuous output current over a wide input range.

The TD1372 employs proprietary Constant On-Time (COT) control scheme providing superior transient response and maintaining constant switching frequency under the continuous conduction mode operation. The internal ramp compensation network allows stable operation with ultra-low equivalent series resistance (ESR) output ceramic capacitors without using external compensation network. An error amplifier in the control loop provides excellent line and load regulation.

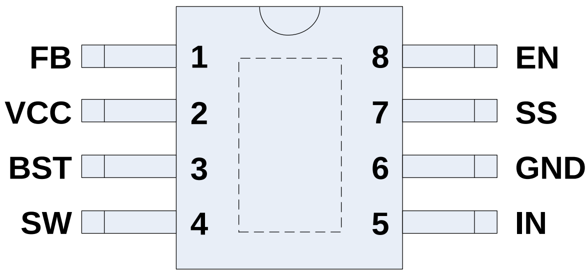
The TD1372 integrates extensive protection functions include: UVLO, OCP, OVP and thermal shutdown. Input under- voltage lockout is internally set as 3.8V.

The TD1372 is available in an ESOP-8 package.

Features

- 4V to 30V Input Voltage Range with Surge Up to 32V
- 2% 0.8V Feedback Voltage Accuracy
- 4A continuous output current
- Support 98% duty cycle Low Dropout Operation
- Stable operation with output low ESR ceramic capacitors
- Fast PWM Constant on Time (COT) control scheme with superior transient performance
- 125KHz Switching frequency with Light Load Pulse Skip Mode
- Frequency Jittering for better EMI performance
- Integrated 40mΩ and 40mΩ High Side and Low Side Switches
- Accurate EN Threshold for the External Programmable VIN UVLO
- Low quiescent current
- Thermal Shutdown with Auto recovery.
- Hiccup mode Over Current protection
- Available in an ESOP-8 Package

Pin Configurations



(Top view)

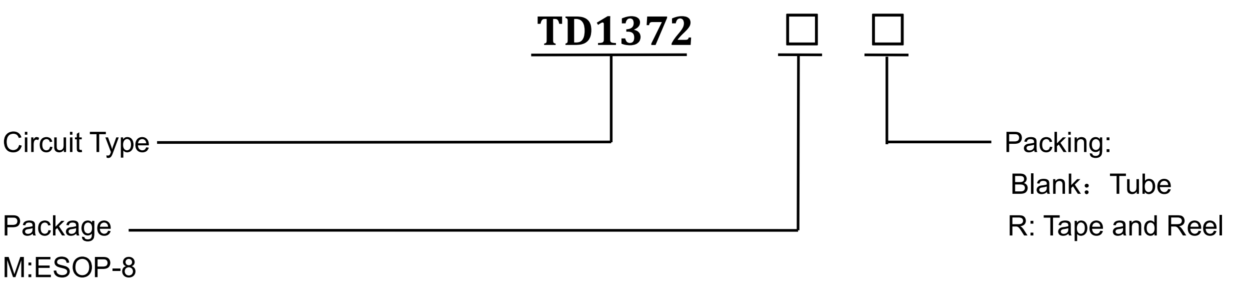
Applications

- PD Fast Charge
- USB HUB
- Laptop Computer
- Tablet PC
- Networking Systems
- Personal Video Recorders
- Distributed Power Systems

Pin Description

Pin Number	Pin Name	Description
1	FB	Feedback Input. Connect FB to the center of the external resistor divider from the output to the AGND to set the output voltage.
2	VCC	Internal 5V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 1µF ceramic capacitor to PGND as close to the pin as possible.
3	BST	High-Side Driver Bootstrap Supply. Connect a 0.1µF capacitor between SW and BST for proper operation.
4	SW	Output pin of internal power switches. Connect this pin to the inductor and bootstrap capacitor.
5	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The TD1372 operates from a +4V to +30V input rail. Bypass IN to PGND with a 22µF or greater low ESR ceramic capacitor.
6	GND	System Analog Ground.
7	SS	Output Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. An internal 10µA pull-up current from VCC on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions.
8	EN	The device is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.3V going up and 1.2V going down. An external resistor divider from VIN can be used to program a VIN threshold below which the device will shut down. Connect EN to VIN through a 100k resistor for automatic startup.
EP	PGND	Exposed Pad is connected to the low side MOSFET Power Ground. Connect EP to a large-area contiguous copper ground plane for effective power dissipation.

Ordering Information



Function Block

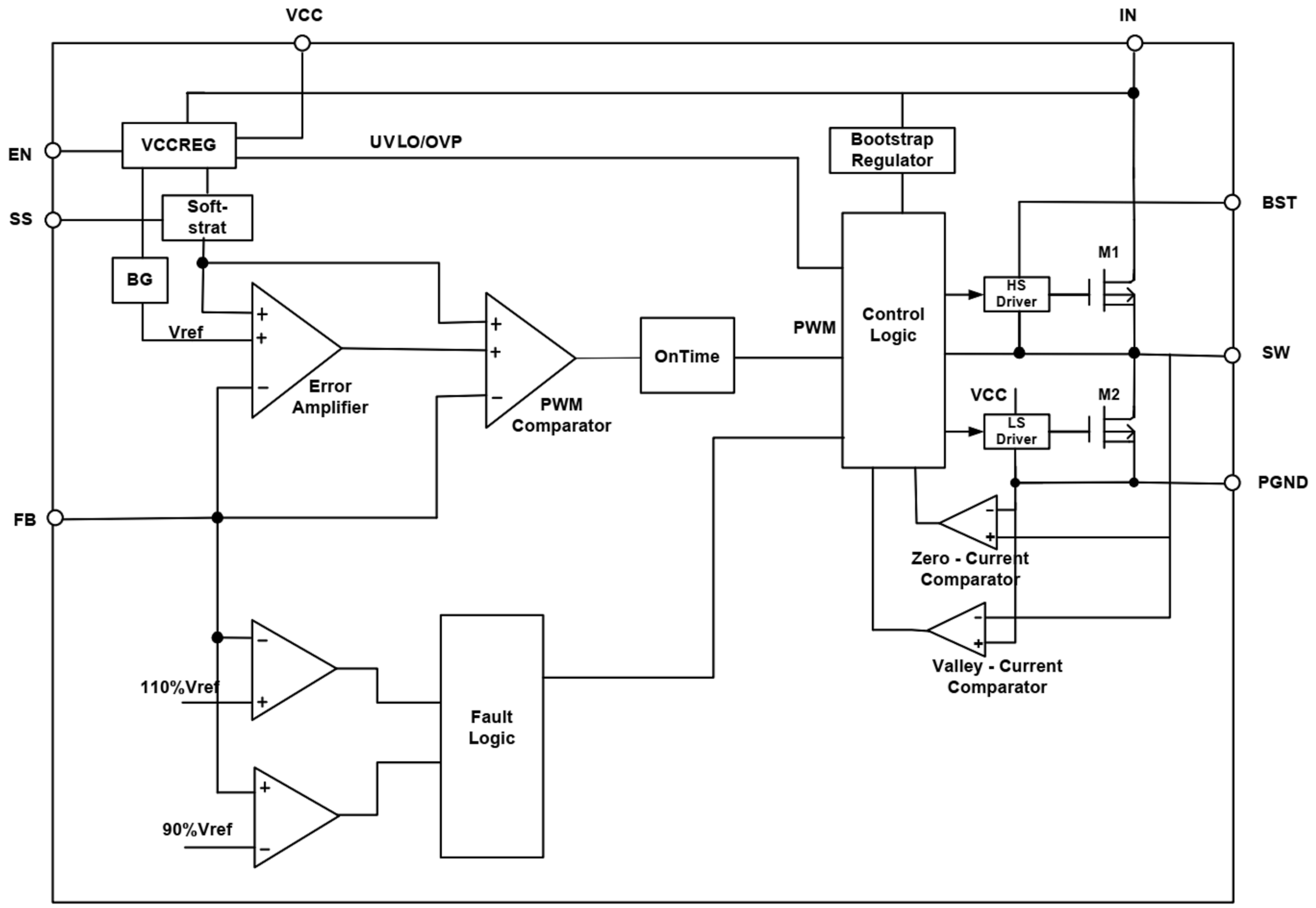


Figure1 Function Block Diagram of TD1372

Absolute Maximum Ratings (Note1)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage IN to GND	+32	V
V_{EN}	EN to GND	+32	V
V_{SW}	SW to GND Voltage	-0.3 to V_{IN}+0.3	V
V_{BST}	BST to SW	- 0.3 to +6	V
	All Other Pins	-0.3 to +6	V
P_D	Power Dissipation	Internally Limited	W
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	50	°C/W

T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	+4 to +30	V
V_{OUT}	Converter Output Voltage	+0.8 to V_{IN}	V
	Operating Junction Temp	-40 ~ +125	°C

Note 3: Refer to the typical application circuit

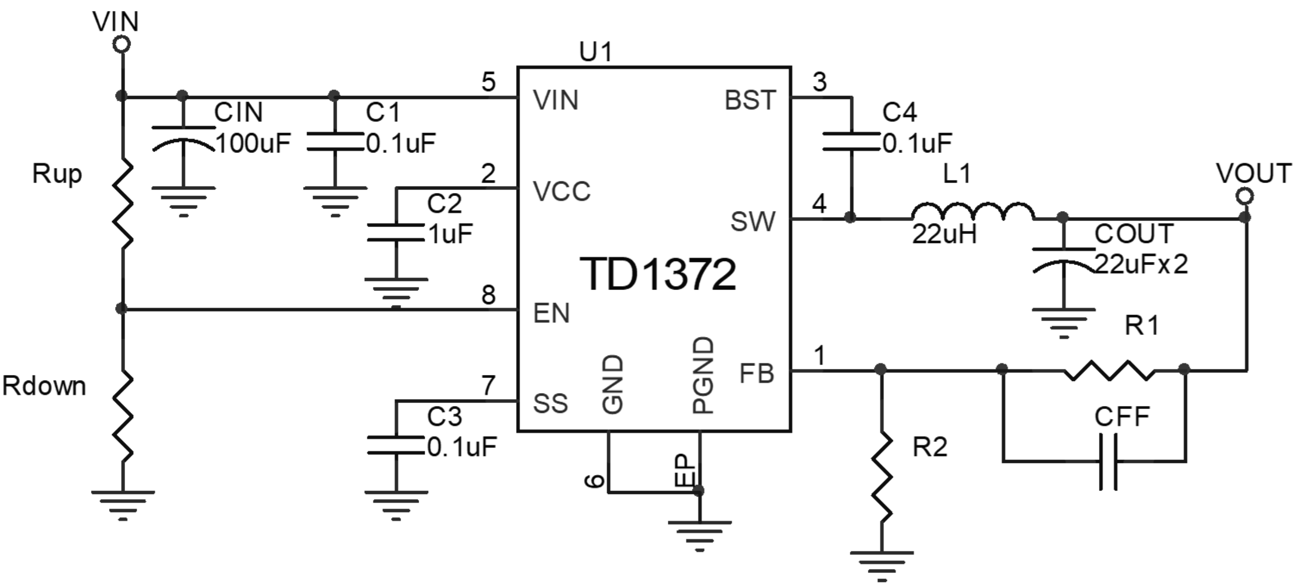
Electrical Characteristics

T_A = +25°C, V_{IN}=12V and V_{EN}=2V, unless otherwise noted. Typical values are at V_{IN}=12V, V_{EN}=2V and V_{OUT} = 5V.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		4	-	30	V
V_{UVLO_R}	Input Under Voltage Lockout Threshold	V_{IN} Increasing	-	3.80	4.05	V
V_{UVLO_HYS}	Input Under Voltage Lockout Hysteresis		-	430	-	mV
I_{SD}	Shutdown Current	V_{EN} = 0V, V_{IN} = 12V	-	1	8	μA
	Supply Current	V_{FB} = 0.85V	-	500	-	μA
V_{FB}	Feedback Voltage		0.784	0.800	0.816	V
I_{FB}	Feedback Current	VFB = 0.8V	-100	-	100	nA
f_{SW}	Oscillator Frequency	I_{OUT}=1A	-	125	-	KHz
T_{OFF}	Minimum OFF-Time		-	120	-	ns
D_{MAX}	Maximum Duty Cycle	V_{FB}=0.57V	-	98	-	%
$R_{DS(ON)HS}$	HS Main Switch On Resistance		-	40	-	mΩ
I_{HSW_LKG}	HS Switch Leakage Current	V_{IN}=12V, V_{EN}=V_{SW}=0V	-	-	1	μA
I_{SL}	Low Side(LS) Switch Valley Current Limit		4	-	-	A

I_{ZX}	LS Switch Zero-Cross Current Limit		-	80	-	mA
R_{ONLS}	LS Switch On Resistance		-	40	-	mΩ
I_{LSW_LKG}	LS Switch Leakage Current	$V_{IN} = V_{SW} = 12V$, $V_{EN} = 0V$	-	-	1	µA
V_{EN_R}	EN Threshold, Rising		-	1.3	-	V
V_{EN_F}	EN Threshold, Falling		-	1.2	-	V
	EN Internal Pull Down Resistor		700	1000	1300	KΩ
	VCC Linear Regulator	$V_{FB} = 0.63V$, $0<I_{VCC}<10mA$	4.7	5.0	5.3	V
T_{SD}	Thermal Shutdown		-	160	-	ºC
T_{SD_HYS}	Thermal Shutdown Hysteresis		-	30	-	ºC

Typical Application Circuit



OPERATION

The TD1372 is a fully integrated synchronous step-down converter employing constant on-time (COT) control scheme to achieve superior transient performance. Its proprietary internal ramp compensation offers stable operation with lower ESR ceramic output capacitors without using external complex compensation networks.

CONSTANT ON-TIME CONTROL

The constant on-time control (COT) operates by comparing the feedback voltage V_{FB} with the reference voltage (V_{FBREG}). When FB droops below the reference, the control circuit turns on HS switch immediately for a pre-determined period of time (on-time) to ramp up the inductor current. When this on-time times out, the LS switch is then turned on to ramp down the inductor current. The LS switch is turned off when inductor current reaches zero I_{ZX} (or triggers negative current limit INEG TD1372) or HS switch is turned on again for the next cycle. This operation repeats itself if FB droops below reference again.
The TD1372 uses a proprietary algorithm to calculate the on-time based on input voltage, output voltage and load current to achieve nearly constant switching frequency over entire continuous conduction load current range. The on-time can be estimated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} * 2\mu S$$

Due to its immediate response on FB voltage droop and simplified loop compensation, The TD1372 offers superior transient response compare to traditional fixed frequency PWM control converters.

LIGHT LOAD OPERATION

In medium and heavy load condition, the TD1372 operates in PWM mode with typical switching frequency of 125KHz. When load current reduces, the TD1372 naturally transitions from PWM mode to PFM mode where the pulse width remains the calculated on-time but the switching frequency reduces to accommodate the low output current. The lower the output current, the lower the switching frequency. Once the switching frequency drops to low enough, the devices enter sleep mode to cut down its quiescent current to maintain high efficiency in light load.
The critical load current at the boundary of PWM mode and PFM mode is related to the inductor ripple current, which depends on the inductor value, input voltage and output voltage. Typically, this critical load current level is estimated as:

$$I_{CRIT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2L \times V_{IN} \times f_{SW}}$$

In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

98% DUTY CYCLE LOW DROPOUT OPERATION

When input voltage approaches the output voltage, the TD1372 will extend the on-time toward the maximum on-time to satisfy the duty cycle requirement to regulate the output voltage. If the input further drops to equal or lower than the output level, the TD1372 forces the main high side (HS) switch to remain on for more than one cycle, eventually reaching 98% duty cycle. The 98% duty cycle operation allows the converter to effectively pass through the input voltage directly to output with minimum voltage drops on the HS switch and the inductor. In the low dropout operation mode, the TD1372 turns on HS switch for multiple switching cycles until it turns off HS switch momentarily and turns on low side (LS) switch (typical 120ns) to refresh the BST supply voltage. The LS switch is turned off after the BST refresh pulse, then the HS switch resumes on for multiple switching cycles which gives the effective 98% duty cycle. The refresh BST pulse is needed to charge the BST capacitor and ensure the HS switch driver circuit proper operation.

ENABLE

TD1372 offers an accurate enable threshold of EN pin, which is typically 1.3V rise and 1.2V fall. The TD1372 is enabled by pulling up the EN pin above 1.3V and TD1372 is disabled by pulling down the EN pin above below 1.2V.
When using the EN pin threshold voltage to program the input startup voltage level, the following equation shall be used:

$$V_{IN-START} = 1.3V \times \frac{R_{UP} + R_{DOWN}//1M}{R_{DOWN}//1M}$$

Where the 1MΩ is the internal pull down resistor on EN pin.
When EN is pulled high, TD1372 will start up if V_{IN} is higher than UVLO threshold. When EN is pulled low, TD1372 will go into shutdown. Tie EN pin to VIN if the shutdown feature is not used.

SOFT START

During the soft start period, output voltage is ramped up linearly to the regulation level, independent of the load current and output capacitor value. SS pin allows user control of output voltage ramp rate during start-up. An internal 10μA pull-up current from VCC on this pin allows a capacitor to program output voltage slew rate. The soft start time with different capacitor is below:

$$T_{SS} = \frac{0.8V \times C_{SS}}{10\mu A}$$

CURRENT LIMIT and HICCUP MODE

The TD1372 has built-in cycle-by-cycle current limit protection to prevent inductor current from running away in any fault conditions. The TD1372 continuously monitors the inductor valley current during its operation. Once the valley current exceeds the limit level, TD1372 will turn on LS and wait for the inductor current to drop down to a pre-determined level before the HS can be turned on again. If this current limit condition is repeated for a sustained long period of time, TD1372 will enter hiccup mode, where it stop switching for a pre-determined period of time before automatically re-try to start up again. It always starts up with soft-start to limit inrush current and avoid output overshoot.
When TD1372 enters valley current limit mode, the peak current is also limit due to the fixed on-time of the HS, and this peak current can be estimated as:

$$I_{PEAK} = I_{VALLEY} + T_{ON} \times \frac{(V_{IN} - V_{OUT})}{L}$$

Application Information

Setting the Output Voltage

External feedback resistors are used to set the output voltage. 1% resistors are recommended to maintain output voltage accuracy. Refer to typical application circuit on page5, the top feedback resistor R1 has some impact on the loop stability, R1 recommended range is between 10kΩ-150kΩ. For any chosen R1, the bottom feedback resistor R2 can be calculated as:

$$\mathrm{R}_2 = \frac{R_1}{\frac{V_{OUT}}{0.8} - 1}$$

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{\mathrm{V_{OUT}}}{\mathrm{f_{SW}} \times \Delta \mathrm{I_L}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Where ΔIL is the peak-to-peak inductor ripple current.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled ISAT) rating of the inductor must be higher than the maximum load current plus 1/2 of in inductor ripple current. The peak inductor current can be calculated by:

$$\mathrm{I_{LP}} = \mathrm{I_{OUT}} + \frac{\mathrm{V_{OUT}}}{2\mathrm{f_{SW}} \times \mathrm{L}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$\mathrm{I_{CIN}} = \mathrm{I_{OUT}} \times \sqrt{\frac{\mathrm{V_{OUT}}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at $V_{IN} = 2*V_{OUT}$, where:

$$\mathrm{I_{CIN}} = \frac{\mathrm{I_{OUT}}}{2}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{\mathrm{I_{OUT}}}{\mathrm{f_{SW}} \times C_{\mathrm{IN}}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Under worst-case conditions where V_{IN} = 2*V_{OUT}:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}}$$

Output Capacitor

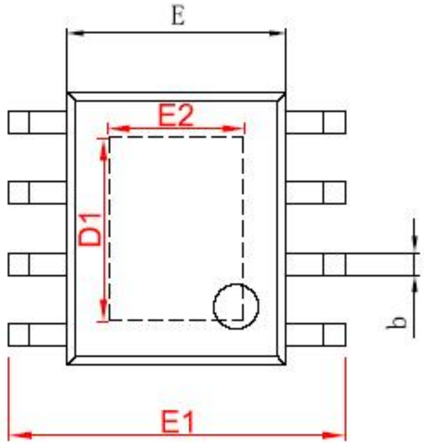
The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the TD1372 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the TD1372's control loop. X5R or X7R type ceramic capacitors have very low equivalent series resistance (ESR) and provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feed forward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

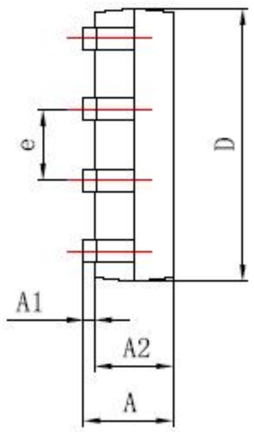
PCB Layout Instruction

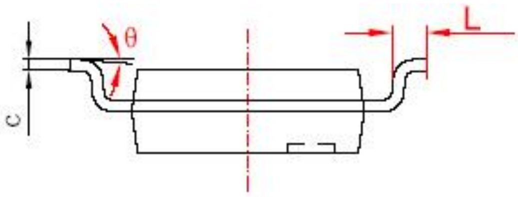
(1) The high current paths (PGND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
(2) Put the input capacitors as close to the IN and PGND pins as possible.
(3) Put the decoupling capacitor as close to the VCC and GND pins as possible. Place the Cap close to GND if the distance is long. And place >3 Vias if via is required to reduce the leakage inductance.
(4) Keep the switching node SW short and away from the feedback network.
(5) The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
(6) Keep the BST voltage path (BST, R_{BST} , C_{BST} and SW) as short as possible.
(7) Keep the IN and PGND pads connected with large copper and use at least two layers for IN and PGND trace to achieve better thermal performance. Also, add several Vias with 10mil_drill/18mil_copper_width close to the IN and P GND pads to help on thermal dissipation.
(8) Four-layer layout is strongly recommended to achieve better thermal performance.

Package Information

ESOP-8 Package Outline Dimensions







	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Design Notes