



CD4020

14-stage Binary Counter

Product Specification

Specification Revision History:

Version	Date	Description
2023-06-A1	2023-06	New
2024-07-A2	2024-07	Modify the content



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1、General Description

The CD4020 is a 14-stage binary counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0, and Q3 to Q13).

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Features:

- Supply voltage range: 3V to 15V
- Temperature range: -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4020DA16.TB	DIP16	CD4020	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4020SA16.TB	SOP16	CD4020	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4020TA16.TB	TSSOP16	CD4020	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4020SA16.TR	SOP16	CD4020	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4020TA16.TR	TSSOP16	CD4020	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

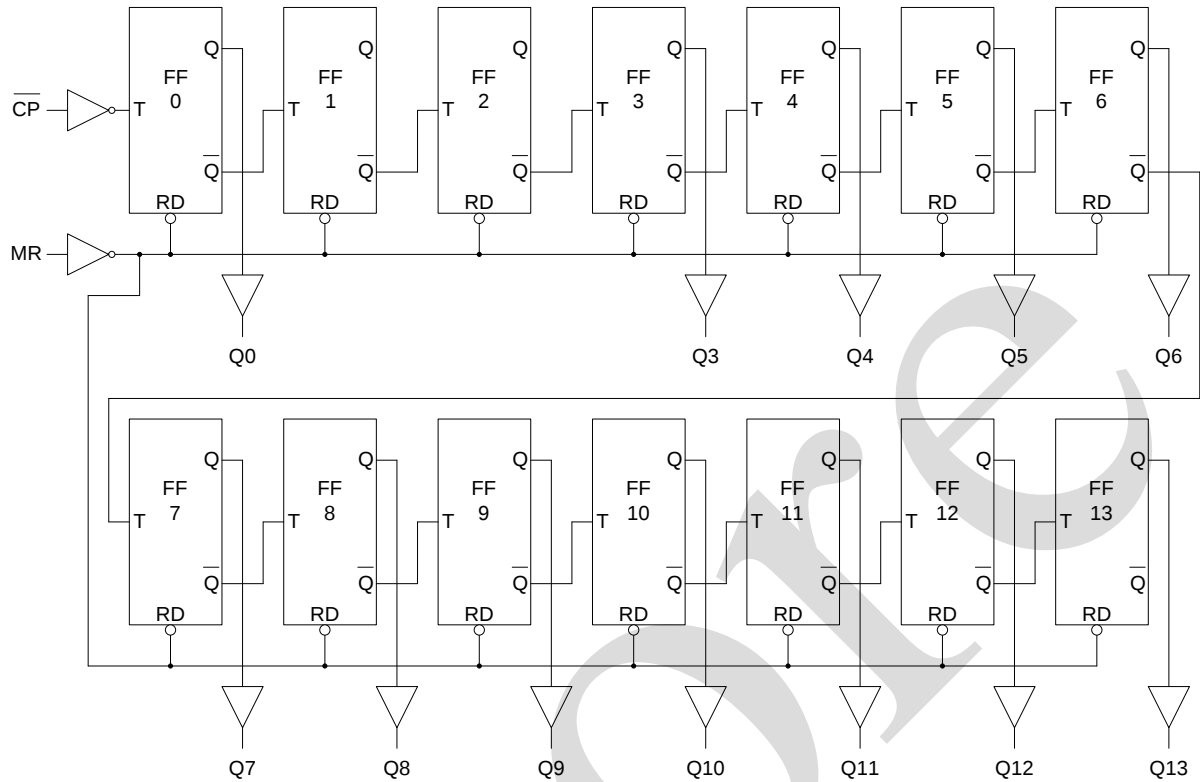
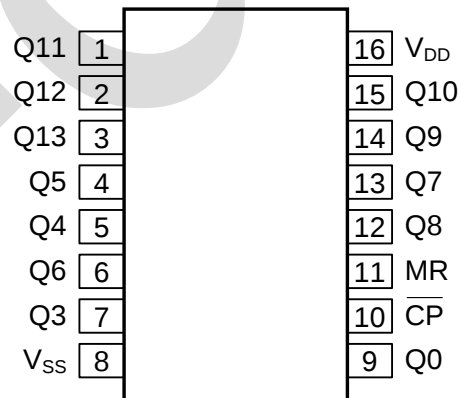


Figure 1. Logic diagram

2.2、Pin Configurations





2.3、Pin Description

Pin No.	Pin Name	Description
1	Q11	parallel output
2	Q12	parallel output
3	Q13	parallel output
4	Q5	parallel output
5	Q4	parallel output
6	Q6	parallel output
7	Q3	parallel output
8	V _{SS}	ground supply voltage
9	Q0	parallel output
10	$\overline{CP}$	clock input (HIGH-to-LOW edge triggered)
11	MR	master reset input (active HIGH)
12	Q8	parallel output
13	Q7	parallel output
14	Q9	parallel output
15	Q10	parallel output
16	V _{DD}	supply voltage

2.4、Function Table

Input		Output
$\overline{CP}$	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	Count
X	H	L

Note:

H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=positive-going transition; ↓=negative-going transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{DD}	-		-0.5	+18	V
input voltage	V _I	all inputs		-0.5	V _{DD} +0.5	V
DC input current	I _{IK}	any one input		-	±10	mA
storage temperature	T _{stg}	-		-65	+150	°C
soldering temperature	T _L	10s	DIP	245		°C
			SOP/SSOP	260		



3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		15V	-	11	-	-	V
LOW-level input voltage	V_{IL}	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		15V	-	-	-	4	V
HIGH-level output voltage	V_{OH}	5V	$ I_O <1\mu\text{A}$	4.95	-	-	V
		10V	$ I_O <1\mu\text{A}$	9.95	-	-	V
		15V	$ I_O <1\mu\text{A}$	14.95	-	-	V
LOW-level output voltage	V_{OL}	5V	$ I_O <1\mu\text{A}$	-	-	0.05	V
		10V	$ I_O <1\mu\text{A}$	-	-	0.05	V
		15V	$ I_O <1\mu\text{A}$	-	-	0.05	V
HIGH-level output current	I_{OH}	5V	$V_O=4.6\text{V}$	-	-	-0.34	mA
		5V	$V_O=2.5\text{V}$	-	-	-1.3	mA
		10V	$V_O=9.5\text{V}$	-	-	-0.55	mA
		15V	$V_O=13.5\text{V}$	-	-	-1.65	mA
LOW-level output current	I_{OL}	5V	$V_O=0.4\text{V}$	0.34	-	-	mA
		10V	$V_O=0.5\text{V}$	0.46	-	-	mA
		15V	$V_O=1.5\text{V}$	1.4	-	-	mA
input leakage current	I_I	15V	$V_I=15\text{V}$ or GND	-	-	± 1	μA
supply current	I_{DD}	5V	$V_I=5\text{V}$ or GND; $I_O=0\text{A}$	-	-	150	μA
		10V	$V_I=10\text{V}$ or GND; $I_O=0\text{A}$	-	-	300	μA
		15V	$V_I=15\text{V}$ or GND; $I_O=0\text{A}$	-	-	600	μA



3.3.2、DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{V}$, unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		15V	-	11	-	-	V
LOW-level input voltage	V_{IL}	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		15V	-	-	-	4	V
HIGH-level output voltage	V_{OH}	5V	$ I_O < 1\mu\text{A}$	4.95	-	-	V
		10V	$ I_O < 1\mu\text{A}$	9.95	-	-	V
		15V	$ I_O < 1\mu\text{A}$	14.95	-	-	V
LOW-level output voltage	V_{OL}	5V	$ I_O < 1\mu\text{A}$	-	-	0.05	V
		10V	$ I_O < 1\mu\text{A}$	-	-	0.05	V
		15V	$ I_O < 1\mu\text{A}$	-	-	0.05	V
HIGH-level output current	I_{OH}	5V	$V_O = 4.6\text{V}$	-	-	-0.3	mA
		5V	$V_O = 2.5\text{V}$	-	-	-1.15	mA
		10V	$V_O = 9.5\text{V}$	-	-	-0.45	mA
		15V	$V_O = 13.5\text{V}$	-	-	-1.4	mA
LOW-level output current	I_{OL}	5V	$V_O = 0.4\text{V}$	0.29	-	-	mA
		10V	$V_O = 0.5\text{V}$	0.38	-	-	mA
		15V	$V_O = 1.5\text{V}$	1.2	-	-	mA
input leakage current	I_I	15V	$V_I = 15\text{V}$ or GND	-	-	± 1	μA
supply current	I_{DD}	5V	$V_I = 5\text{V}$ or GND; $I_O = 0\text{A}$	-	-	150	μA
		10V	$V_I = 10\text{V}$ or GND; $I_O = 0\text{A}$	-	-	300	μA
		15V	$V_I = 15\text{V}$ or GND; $I_O = 0\text{A}$	-	-	600	μA



3.3.3、AC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{V}$, unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	5	$\overline{CP}$ to Q0; see Figure 4	-	105	210	ns
		10		-	45	90	ns
		15		-	30	65	ns
		5	Qn to Qn+1	-	80	160	ns
		10		-	30	60	ns
		15		-	20	40	ns
		5	MR to Qn; see Figure 4	-	180	360	ns
		10		-	90	180	ns
		15		-	70	140	ns
LOW to HIGH propagation delay	t_{PLH}	5	$\overline{CP}$ to Q0; see Figure 4	-	105	210	ns
		10		-	50	95	ns
		15		-	35	70	ns
		5	Qn to Qn+1	-	70	140	ns
		10		-	25	50	ns
		15		-	20	40	ns
transition time	t_t	5	see Figure 4	-	60	120	ns
		10		-	30	60	ns
		15		-	20	40	ns
pulse width	t_w	5	$\overline{CP} = \text{HIGH}$; minimum width; see Figure 4	50	25	-	ns
		10		25	15	-	ns
		15		20	10	-	ns
		5	MR=HIGH; minimum width; see Figure 4	130	65	-	ns
		10		95	50	-	ns
		15		90	45	-	ns
recovery time	t_{rec}	5	MR input; see Figure 4	115	60	-	ns
		10		65	35	-	ns
		15		55	25	-	ns
maximum frequency	f_{max}	5	see Figure 4	5	10	-	MHz
		10		13	25	-	MHz
		15		18	35	-	MHz



3.3.4、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{SS} = 0\text{V}$, unless otherwise specified.)

Parameter	Symbol	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	5	$\overline{CP}$ to Q0; see Figure 4	-	-	252	ns
		10		-	-	108	ns
		15		-	-	78	ns
		5	Qn to Qn+1	-	-	192	ns
		10		-	-	72	ns
		15		-	-	48	ns
		5	MR to Qn; see Figure 4	-	-	432	ns
		10		-	-	216	ns
		15		-	-	168	ns
LOW to HIGH propagation delay	t_{PLH}	5	$\overline{CP}$ to Q0; see Figure 4	-	-	252	ns
		10		-	-	114	ns
		15		-	-	84	ns
		5	Qn to Qn+1	-	-	168	ns
		10		-	-	60	ns
		15		-	-	48	ns
transition time	t_t	5	see Figure 4	-	-	144	ns
		10		-	-	72	ns
		15		-	-	48	ns
pulse width	t_w	5	$\overline{CP} = \text{HIGH};$ minimum width; see Figure 4	60	-	-	ns
		10		30	-	-	ns
		15		24	-	-	ns
		5	MR=HIGH; minimum width; see Figure 4	156	-	-	ns
		10		114	-	-	ns
		15		108	-	-	ns
recovery time	t_{rec}	5	MR input; see Figure 4	138	-	-	ns
		10		78	-	-	ns
		15		66	-	-	ns
maximum frequency	f_{max}	5	see Figure 4	4.2	-	-	MHz
		10		10.8	-	-	MHz
		15		15	-	-	MHz



4、Testing Circuit

4.1、AC Testing Circuit

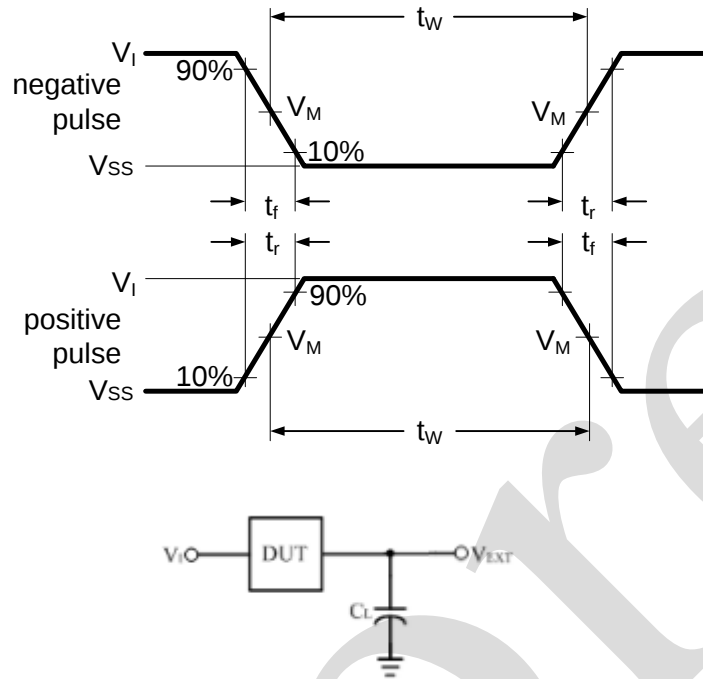


Figure 3. Load circuit

C_L includes probe and jig capacitance.

4.2、Test Data

Supply voltage	Input		Load	V_{EXT}		
V_{DD}	V_I	$t_r = t_f$	C_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
5V to 15V	V_{CC}	$\leq 20ns$	50pF	Open	V_{DD}	V_{SS}



4.3、AC Testing Waveforms

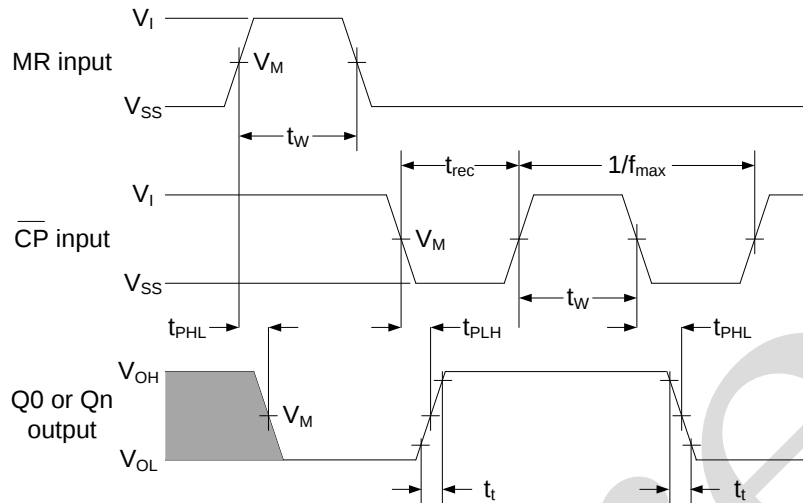


Figure 4. Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency

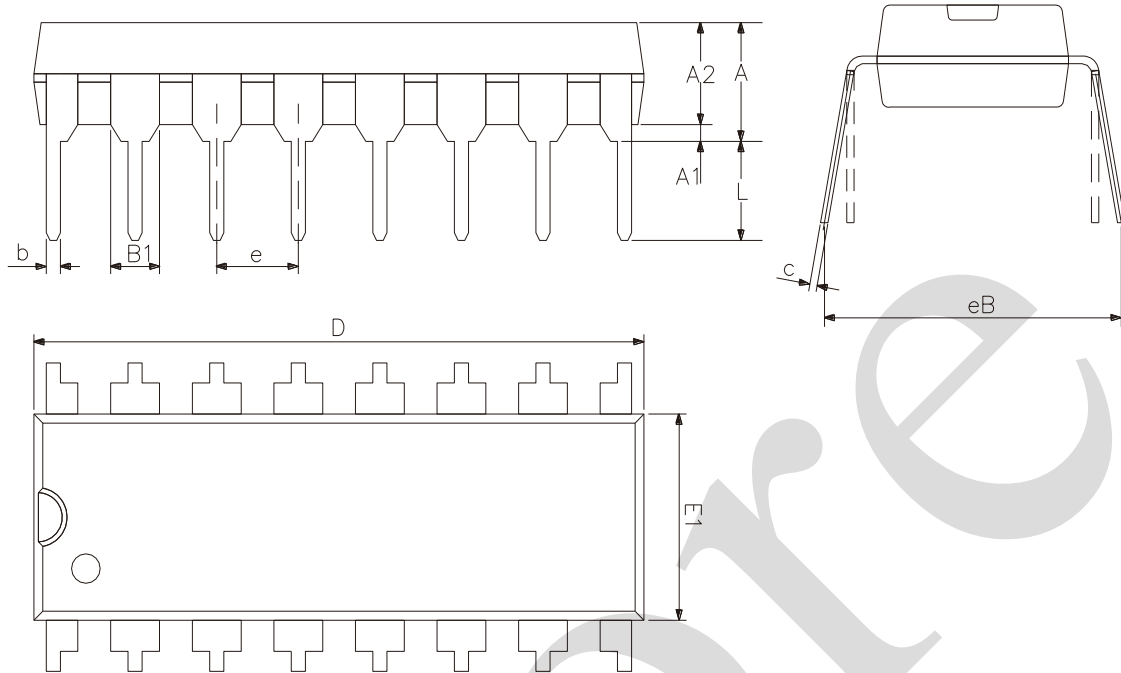
4.4、Measurement Points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$



5、Package Information

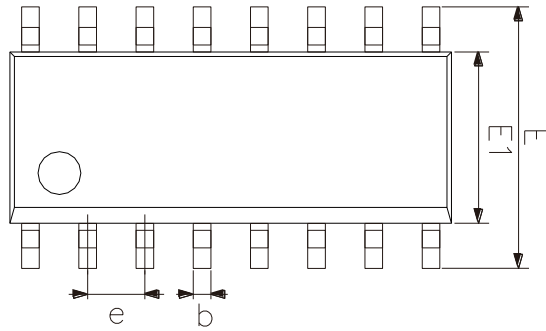
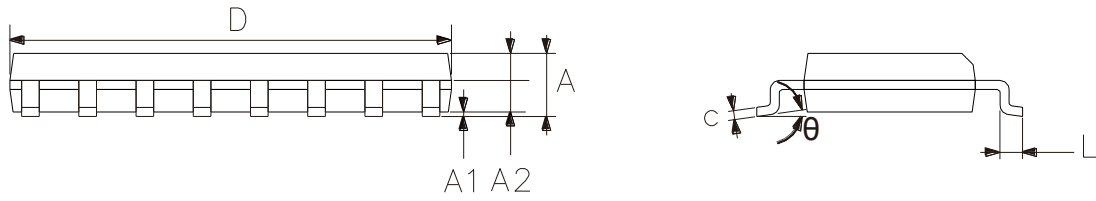
5.1、DIP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A2	3.00	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



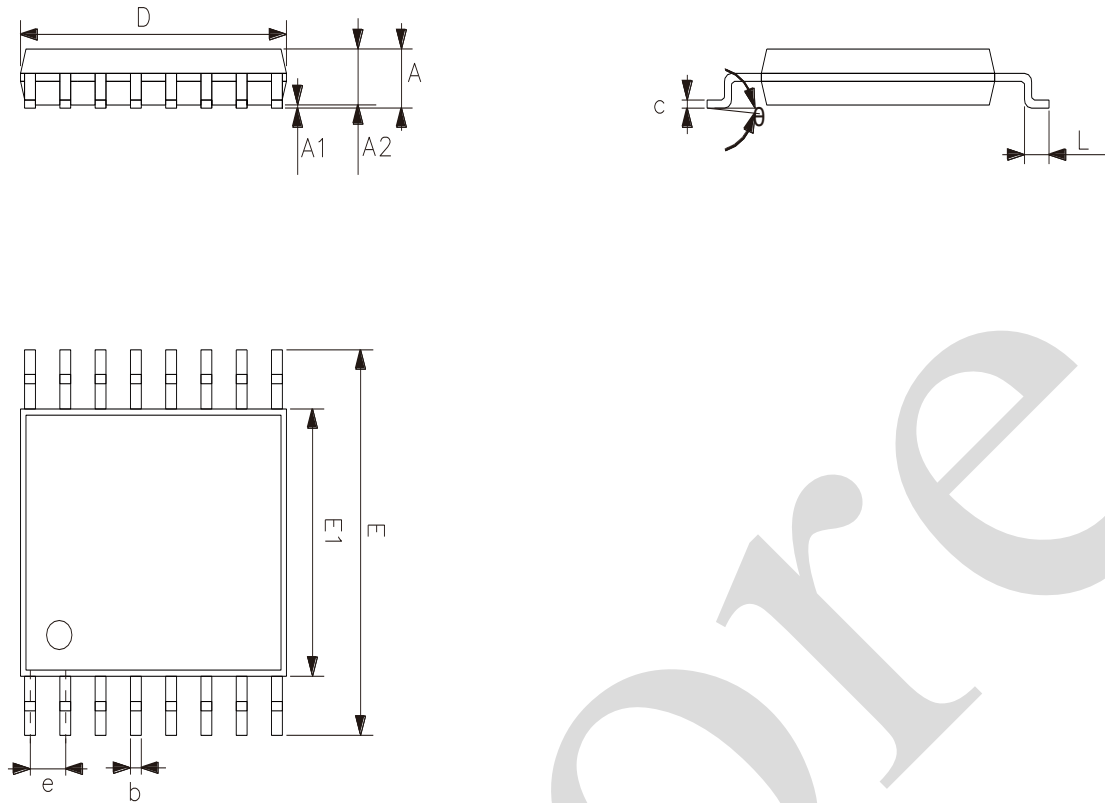
5.2、SOP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

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