



Description

The HTN2404K uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 240V$ $I_D = 0.1A$

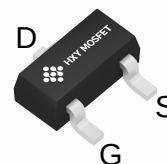
$R_{DS(ON)} < 14\Omega @ V_{GS}=10V$

Application

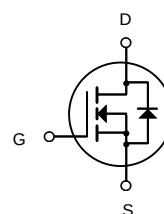
Battery protection

Load switch

Uninterruptible power supply



SOT-23



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HTN2404K	SOT-23	SR	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Limit	Unit
V_{DS}	Drain-Source Voltage		240	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_A = 25^\circ\text{C}$	0.1	A
		$T_A = 100^\circ\text{C}$	0.09	
I_{DM}	Drain Current-Pulsed (Note 1)		0.4	A
P_D	Maximum Power Dissipation		0.36	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 To 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)		200	$^\circ\text{C/W}$



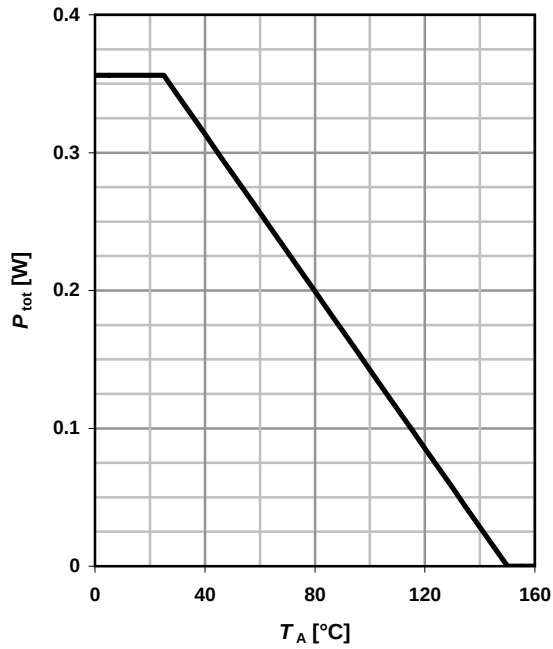
Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - minimal footprint	R_{thJA}		-	-	350	K/W
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	240	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0\text{ V}$, $I_D=56\text{ }\mu\text{A}$	0.8	1.4	1.8	
Drain-source leakage current	$I_{D(off)}$	$V_{DS}=240\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25^{\circ}\text{C}$	-	-	0.01	μA
		$V_{DS}=240\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150^{\circ}\text{C}$	-	-	5	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	10	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$, $I_D=0.09\text{ A}$	-	9.07	20	Ω
		$V_{GS}=10\text{ V}$, $I_D=0.1\text{ A}$	-	7.7	14	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=0.08\text{ A}$	0.06	0.13	-	S
Input capacitance	C_{iss}	$V_{GS}=0\text{ V}$, $V_{DS}=25\text{ V}$, $f=1\text{ MHz}$	-	58	77	pF
Output capacitance	C_{oss}		-	7.3	10	
Reverse transfer capacitance	C_{rss}		-	2.8	4.2	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=120\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=0.1\text{ A}$, $R_G=6\text{ }\Omega$	-	3.3	5.0	ns
Rise time	t_r		-	3.1	4.6	
Turn-off delay time	$t_{d(off)}$		-	13.7	20	
Fall time	t_f		-	64.5	97	
Gate to source charge	Q_{gs}	$V_{DD}=192\text{ V}$, $I_D=0.1\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$	-	0.16	0.22	nC
Gate to drain charge	Q_{gd}		-	0.8	1.2	
Gate charge total	Q_g		-	2.1	3.1	
Gate plateau voltage	$V_{plateau}$		-	2.90	-	V
Diode continuous forward current	I_S	$T_A=25^{\circ}\text{C}$	-	-	0.11	A
Diode pulse current	$I_{S,pulse}$		-	-	0.43	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}$, $I_F=0.1\text{ A}$, $T_j=25^{\circ}\text{C}$	-	0.81	1.2	V
Reverse recovery time	t_{rr}	$V_R=120\text{ V}$, $I_F=0.1\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$	-	42.9	64.3	ns
Reverse recovery charge	Q_{rr}		-	22.6	34	



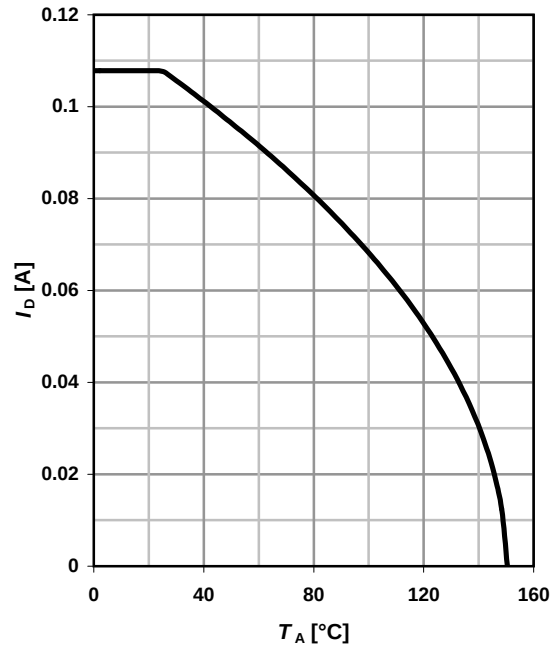
1 Power dissipation

$$P_{\text{tot}} = f(T_A)$$



2 Drain current

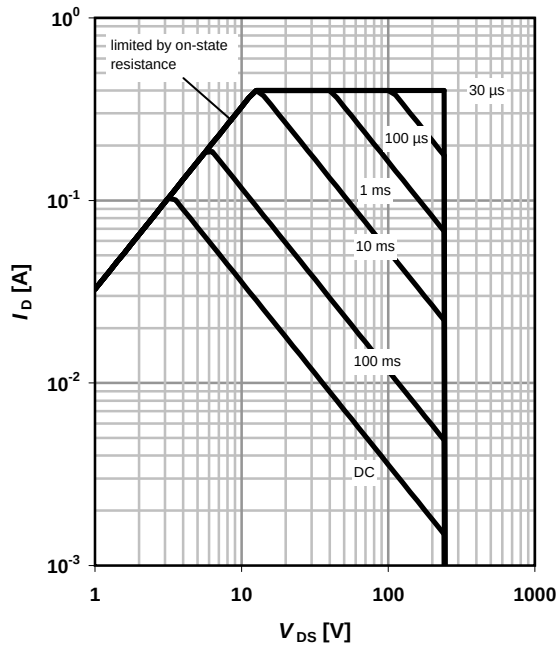
$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_A = 25^\circ\text{C}; D = 0$$

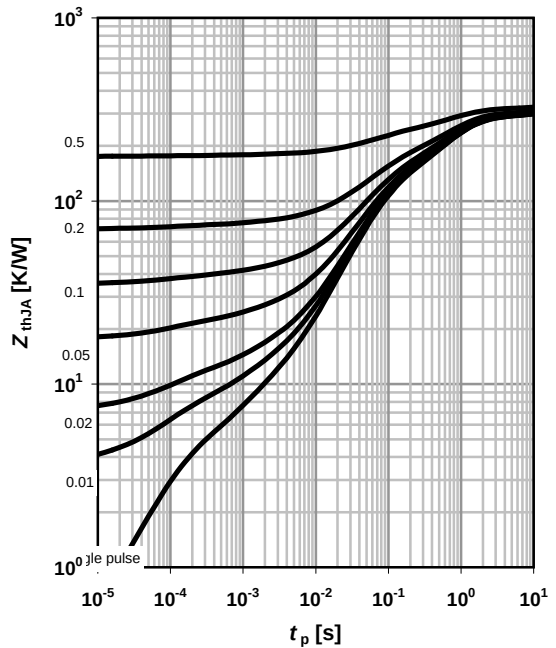
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJA}} = f(t_p)$$

parameter: $D = t_p / T$

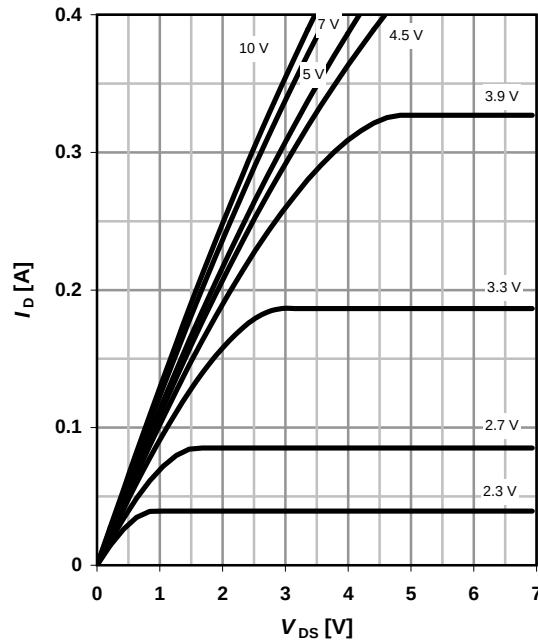




5 Typ. output characteristics

$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$

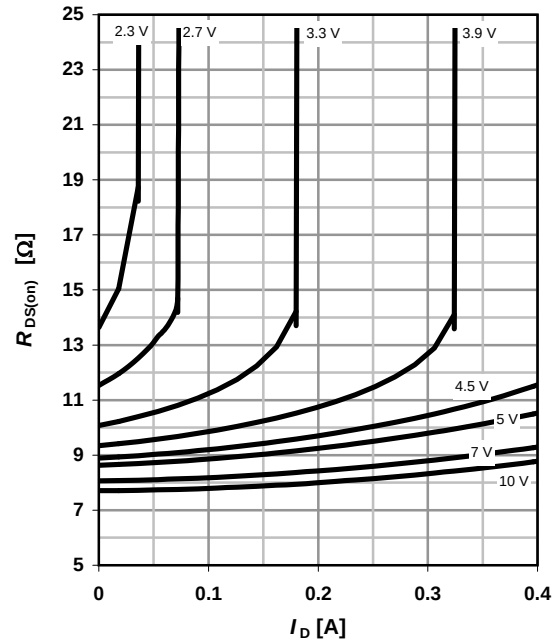
parameter: V_{GS}



6 Typ. drain-source on resistance

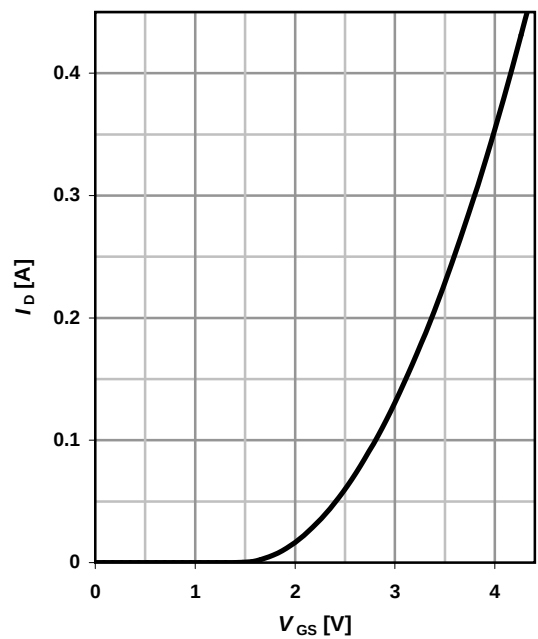
$R_{DS(on)} = f(I_D); T_J = 25^\circ\text{C}$

parameter: V_{GS}



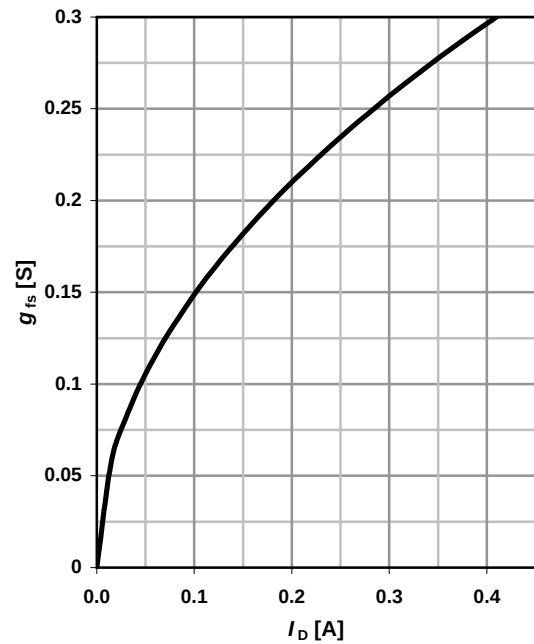
7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$



8 Typ. forward transconductance

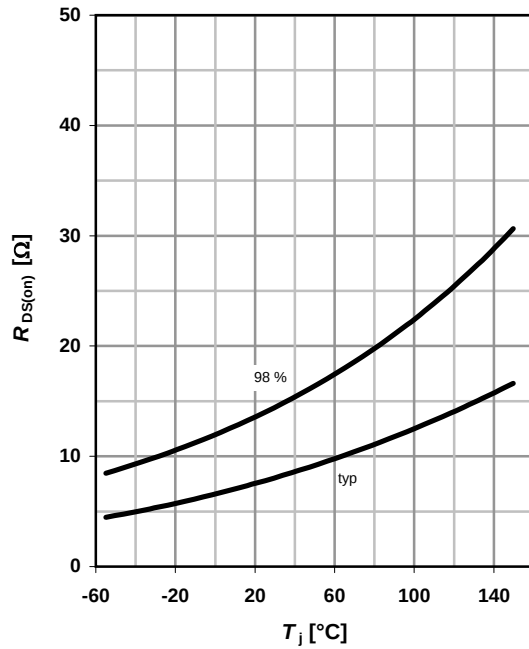
$g_{fs} = f(I_D); T_J = 25^\circ\text{C}$





9 Drain-source on-state resistance

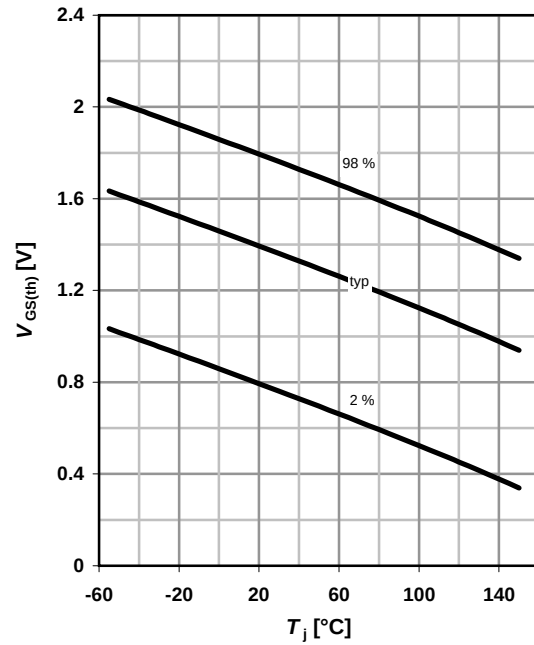
$$R_{DS(on)} = f(T_j); I_D = 0.1 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

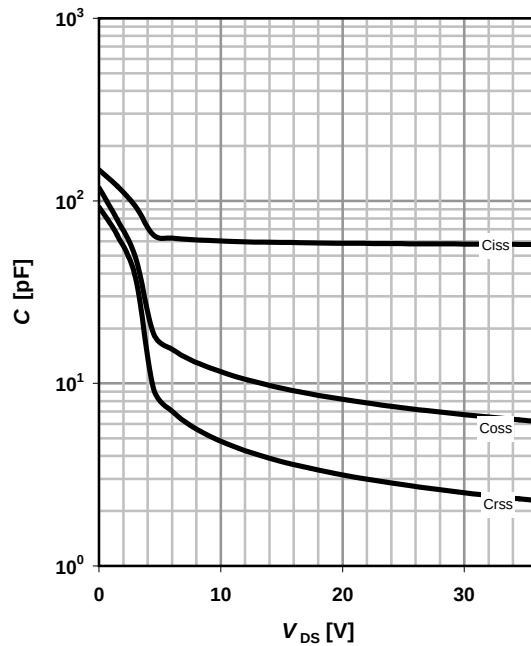
$$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 56 \mu\text{A}$$

parameter: I_D



11 Typ. capacitances

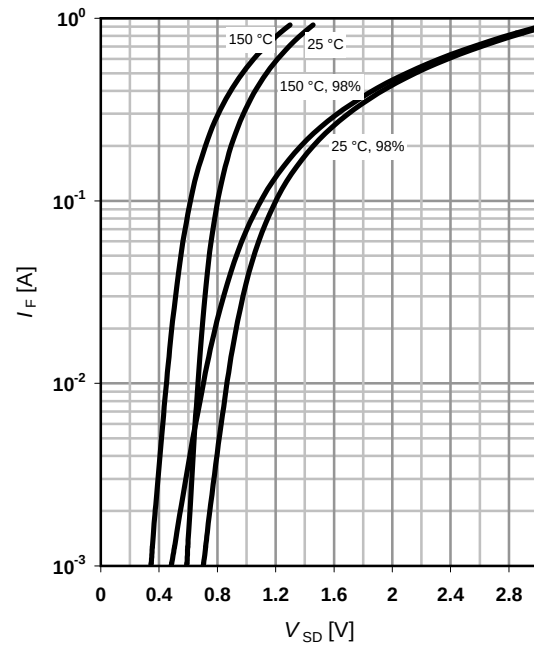
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^{\circ}\text{C}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

parameter: T_j

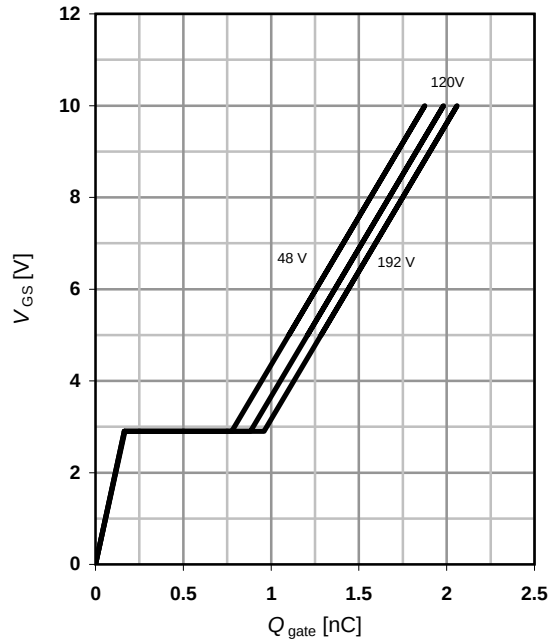




13 Typ. gate charge

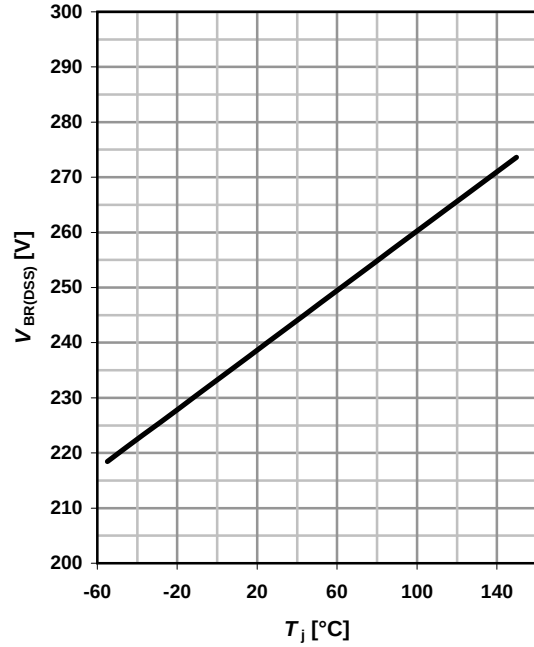
$V_{GS}=f(Q_{gate}); I_D=0.1\text{ A pulsed}$

parameter: V_{DD}



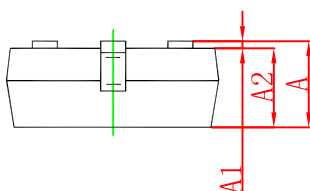
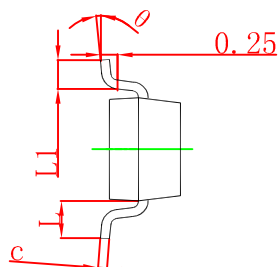
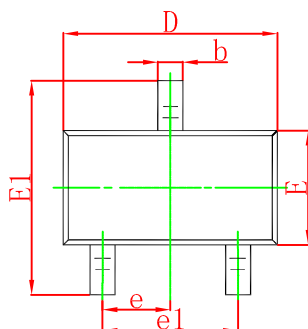
14 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250\text{ }\mu\text{A}$



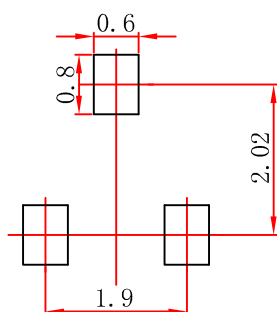


SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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