

### **General Description**

The IRFB4115PBF use advanced SGT MOSFET

technology to provide low RDS(ON), low gate charge,

fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness

# 123

### TO-220S

### **General Features**

V<sub>DS</sub> =150V I<sub>D</sub> =120A

 $R_{DS(ON)}$  < 11.5m $\Omega$  @  $V_{GS}$ =10V

# PIN1 G PIN3 S

### N-Channel MOSFET

## **Applications**

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications

### **Package Marking and Qrdering Information**

Product ID	Pack	Marking	Qty(PCS)
IRFB4115PBF	TO-220S	120N15 XXX YYYY	50

### Absolute Maximum Ratings at Tj=25℃ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	150	V
Gate source voltage	VGS	±20	V
Continuous drain current <sup>1)</sup>	ID	120	Α
Pulsed drain current <sup>2)</sup>	ID, pulse	352	Α
Power dissipation <sup>3)</sup>	PD	178.6	W
Single pulsed avalanche energy <sup>5)</sup>	EAS	204.8	mJ
Operation and storage temperature	Tstg, Tj	-55 to 150	°C
Thermal resistance, junction-case	RθJC	0.7	°C/W
Thermal resistance, junction-ambient <sup>4)</sup>	RθJA	52	°C/W

# Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0V, I_{D} = 250\mu A$	150	-	-	V
Gate-body Leakage Current	Igss	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current  T <sub>J</sub> =25°C  T <sub>J</sub> =100°C	loss	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V	-	-	100	μΑ
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
Drain-Source On-Resistance <sup>4</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	9.5	11.5	mΩ
Forward Transconductance <sup>4</sup>	<b>g</b> fs	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A	-	69	-	S
Dynamic Characteristics <sup>5</sup>	•		•	•		
Input Capacitance	Ciss		-	3310	-	pF
Output Capacitance	Coss	$V_{DS} = 75V, V_{GS} = 0V,$ $f = 1MHz$	-	268	-	
Reverse Transfer Capacitance	Crss	1 - 1Wil 12	-	9.4	-	
Gate Resistance	Rg	f = 1MHz	-	3.2	-	Ω
Switching Characteristics <sup>5</sup>	•					
Total Gate Charge Qg			-	45	-	
Gate-Source Charge	Q <sub>gs</sub>	$V_{GS} = 10V, V_{DS} = 75V,$ $I_{D} = 20A$	-	15	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	8.5	-	
Turn-On Delay Time t <sub>d(on)</sub>			-	16	-	
Rise Time	tr	$V_{GS} = 10V, V_{DD} = 75V,$ $R_{G} = 3\Omega, I_{D} = 20A$	-	12	-	ns
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	-	
Fall Time	tf		-	18	-	
Body Diode Reverse Recovery Time t <sub>rr</sub>		I <sub>F</sub> =20A, dl/dt=100A/µs	-	76	-	ns
Body Diode Reverse Recovery Charge	Qrr	- 11-20A, αι/αι-100A/μS	-	182	-	nC
Drain-Source Body Diode Characteristics						
Diode Forward Voltage <sup>4</sup>	V <sub>SD</sub>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
Continuous Source Current Tc=25°C	Is	-	-	-	120	Α

### Notes:

- 1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}$ =150°C
- 2. The EAS data shows Max. rating . The test condition is  $V_{\text{DD}}$ =50V, $V_{\text{GS}}$ =10V,L=0.4mH,  $I_{\text{AS}}$ =32A.
- 3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
- 4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
- 5. This value is guaranteed by design hence it is not included in the production test.



# **Typical Characteristics**

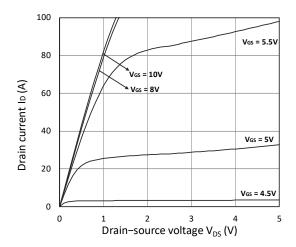


Figure 1. Output Characteristics

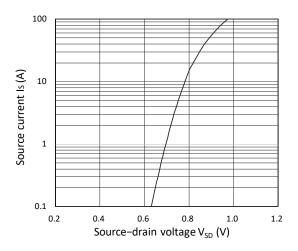


Figure 3. Forward Characteristics of Reverse

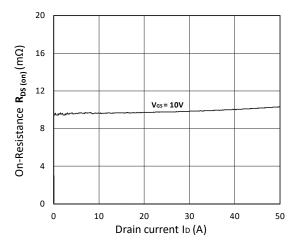


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$ 

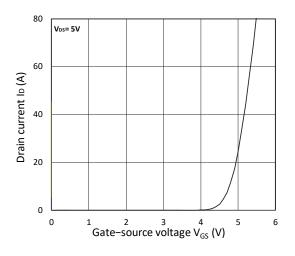


Figure 2. Transfer Characteristics

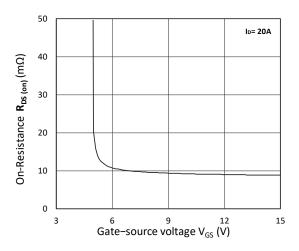


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$ 

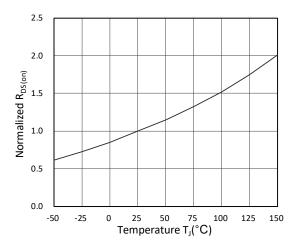
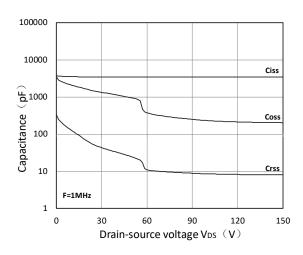


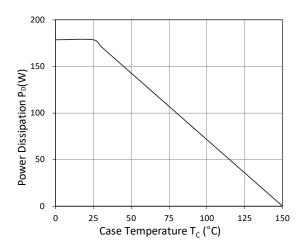
Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature



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Figure 7. Capacitance Characteristics

Figure 8. Gate Charge Characteristics



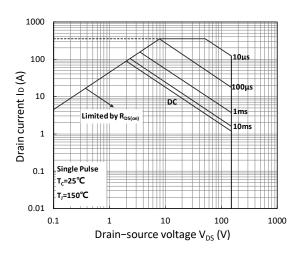


Figure 9. Power Dissipation

Figure 10. Safe Operating Area

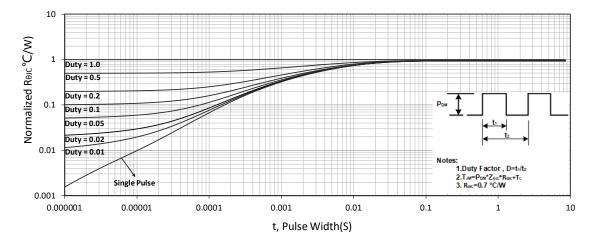


Figure 11. Normalized Maximum Transient Thermal Impedance

### **Test Circuit**

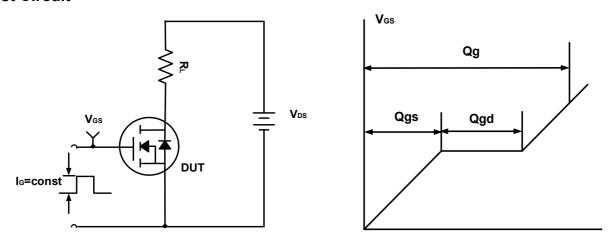


Figure A. Gate Charge Test Circuit & Waveforms

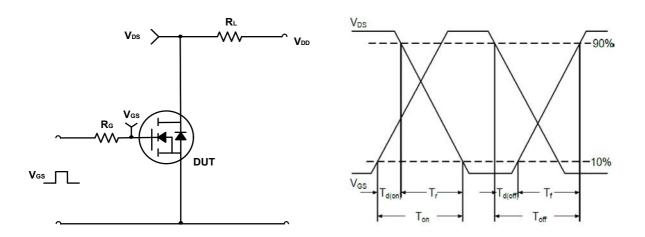


Figure B. Switching Test Circuit & Waveforms

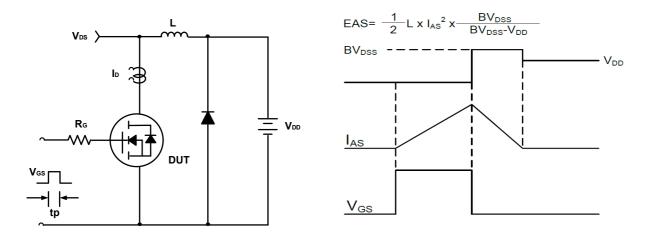
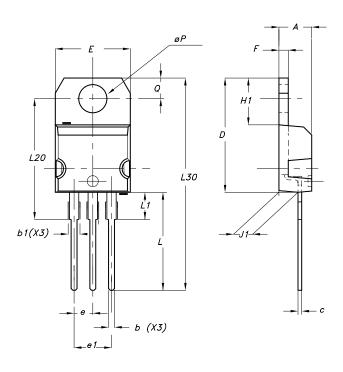


Figure C. Unclamped Inductive Switching Circuit & Waveforms



# Package Information TO-220S



DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
Е	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øΡ	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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