



Description

The HSTD60NF55LAT4 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and

operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 50A$

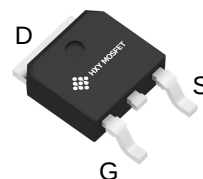
$R_{DS(ON)} < 15m\Omega$ @ $V_{GS}=10V$

Application

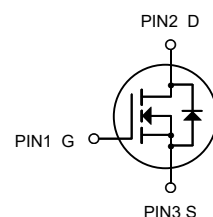
Battery protection

Load switch

Uninterruptible power supply



TO-252-2L
(TO-252(DPAK))



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
HSTD60NF55LAT4	TO-252-2L(TO-252(DPAK))	HXY MOSFET	2500

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	50	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	25	A
I_{DM}	Pulsed Drain Current ²	90	A
EAS	Single Pulse Avalanche Energy ³	39.2	mJ
I_{AS}	Avalanche Current	28	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	45	W
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.8	$^{\circ}C/W$



Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.057	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	11	15	m Ω
		$V_{GS}=4.5V$, $I_D=10A$	---	15	20	
$V_{GS(th)}$	Gate Threshold Voltage		1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=250\mu A$	---	-5.68	---	mV/ $^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=48V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=15A$	---	45	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=48V$, $V_{GS}=4.5V$, $I_D=15A$	---	19.3	---	nC
Q_{gs}	Gate-Source Charge		---	7.1	---	
Q_{gd}	Gate-Drain Charge		---	7.6	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V$, $V_{GS}=10V$, $R_G=3.3$, $I_D=15A$	---	7.2	---	ns
T_r	Rise Time		---	50	---	
$T_{d(off)}$	Turn-Off Delay Time		---	36.4	---	
T_f	Fall Time		---	7.6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1MHz$	---	2423	---	pF
C_{oss}	Output Capacitance		---	145	---	
C_{rss}	Reverse Transfer Capacitance		---	97	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	35	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	80	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=A$, $T_J=25^{\circ}\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=15A$, $dI/dt=100A/\mu s$, $T_J=25^{\circ}\text{C}$	---	16.3	---	nS
Q_{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=28A$
- 4.The power dissipation is limited by 150°C junction temperature 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation



Typical Characteristics

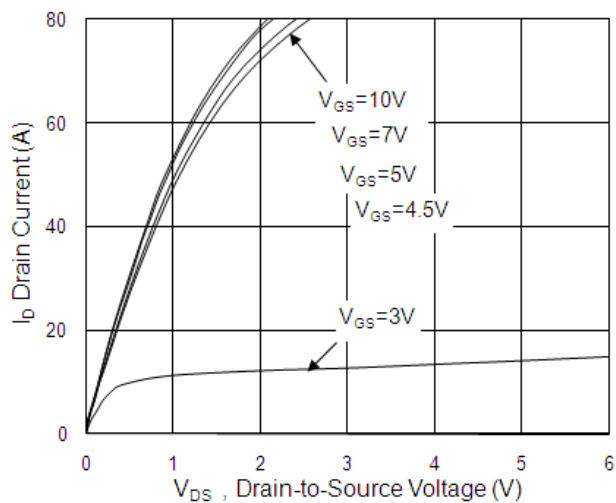


Fig.1 Typical Output Characteristics

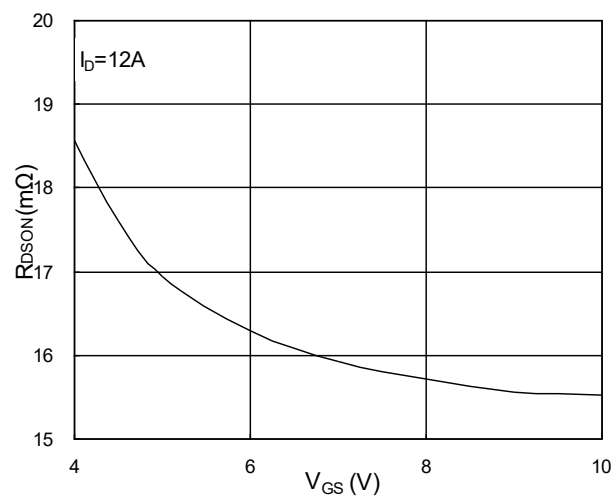


Fig.2 On-Resistance v.s Gate-Source

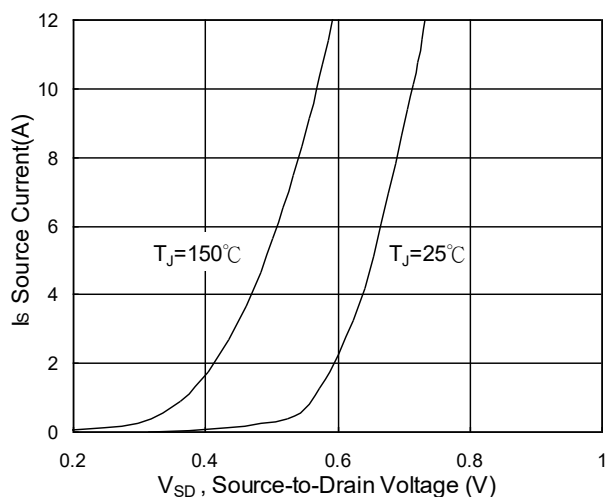


Fig.3 Forward Characteristics of Reverse

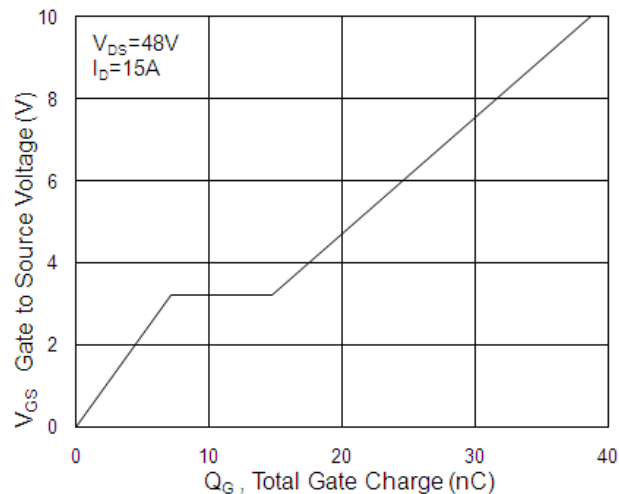


Fig.4 Gate-Charge Characteristics

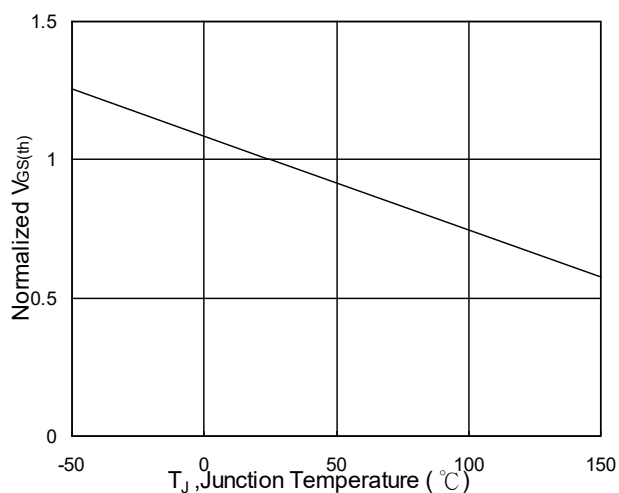


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

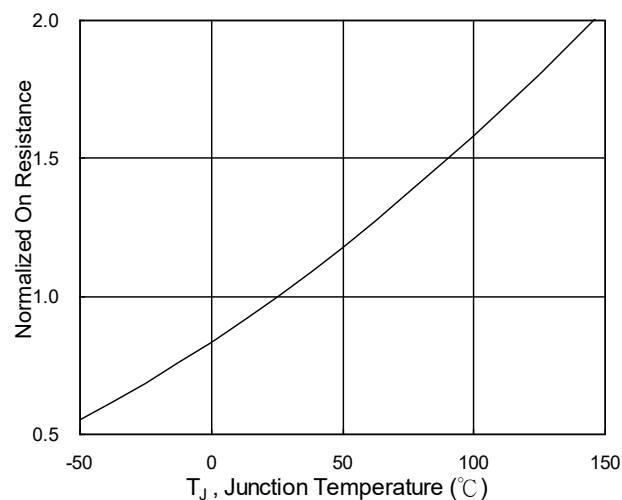


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

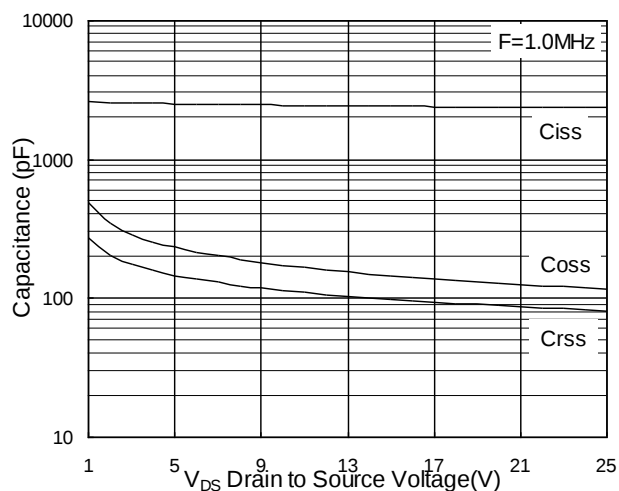


Fig.7 Capacitance

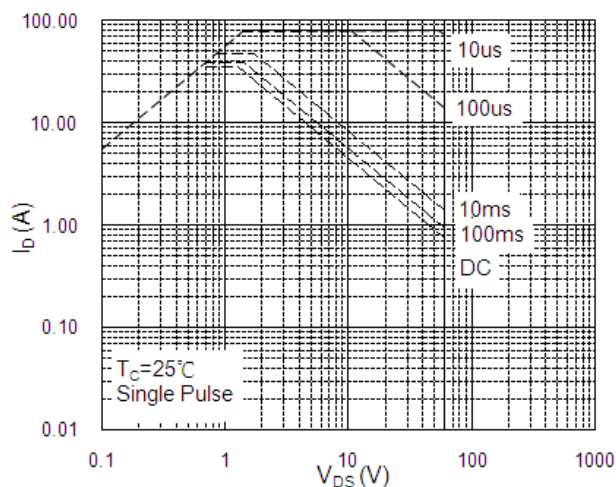


Fig.8 Safe Operating Area

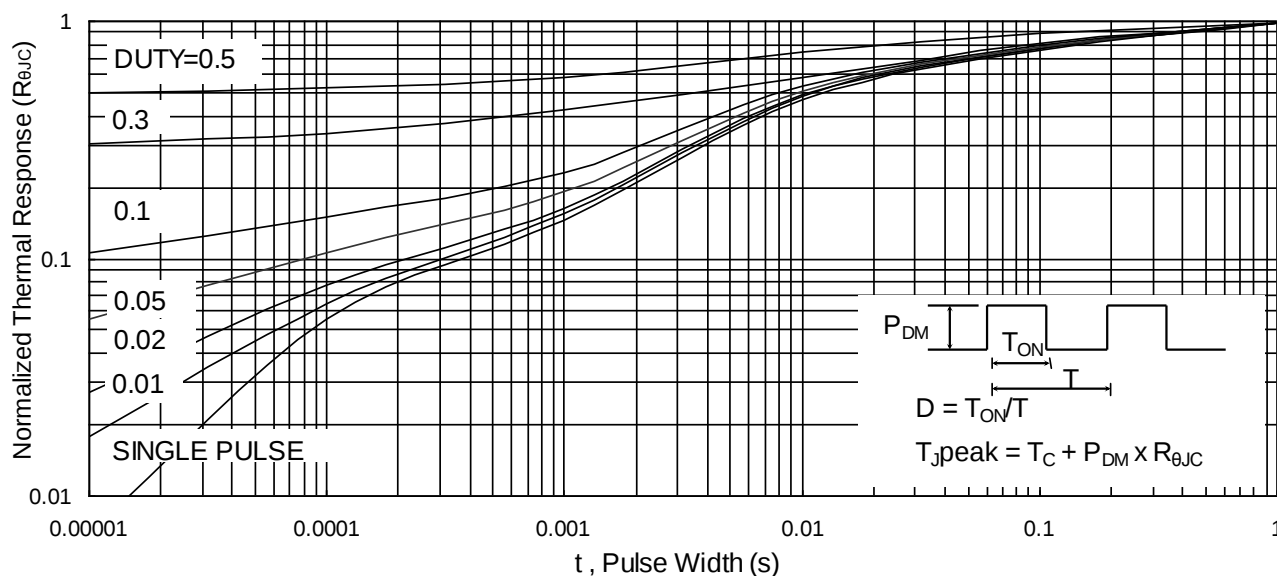


Fig.9 Normalized Maximum Transient Thermal Impedance

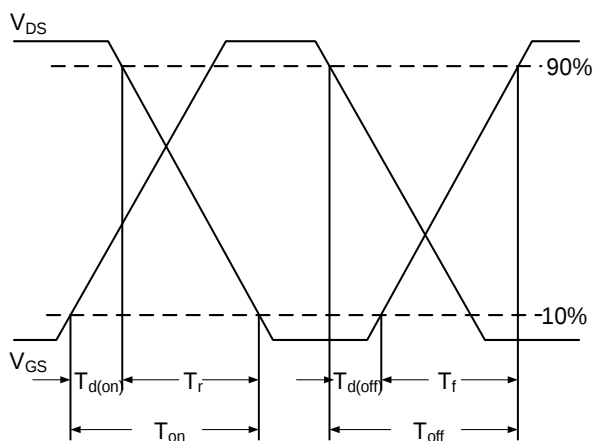


Fig.10 Switching Time Waveform

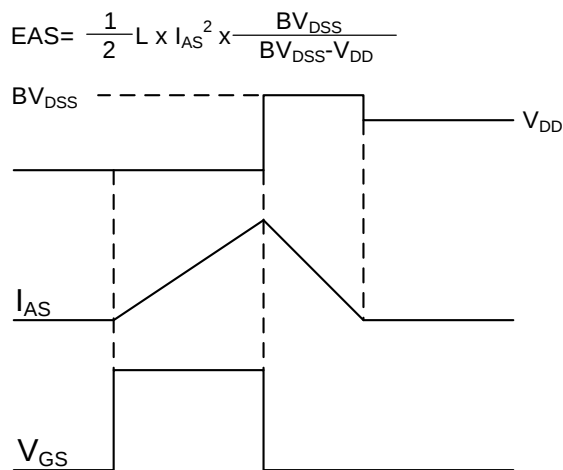
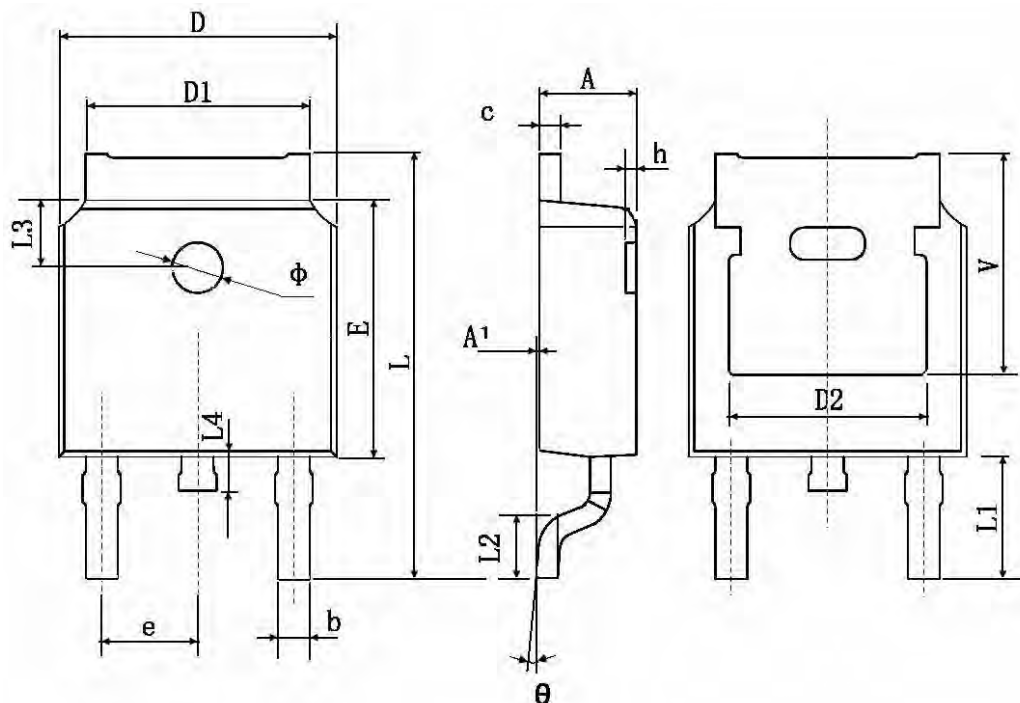


Fig.11 Unclamped Inductive Switching Waveform



N-Channel Enhancement Mode MOSFET

TO-252-2L(TO-252-2(DPAK)) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	



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