

# General Description

The NVMFD5C466NWFT1G use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness.

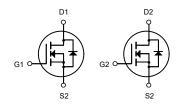
#### D1 D2 D2 S1 G1 S2 G2 S2 G2 F1 Pin 1

DFN5X6B-8L

#### **General Features**

V<sub>DS</sub> =40V I<sub>D</sub> =40 A

 $R_{DS(ON)}$  < 8.5m $\Omega$  @  $V_{GS}$ =10V



## **Applications**

Consumer electronic power supply Motor control Synchronous-rectification Isolated DC Synchronous-rectification applications

**Dual N-Channel MOSFET** 

#### **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
NVMFD5C466NWFT1G	DFN5X6B-8L	HXY MOSFET	5000

#### Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

	<u> </u>		<u> </u>	
Symbol	Parameter		Max.	Units
V <sub>DSS</sub>	Drain-Source Voltage		40	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
	Continuous Drain Current	T <sub>C</sub> = 25°C	40	А
l <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 100°C	25	А
I <sub>DM</sub>	Pulsed Drain Current note1		100	А
Eas	Single Pulsed Avalanche Energy note2		28	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	29	W
Rejc	Thermal Resistance, Junction to Case		3.2	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +175	°C

## NVMFD5C466NWFT1G

**Dual N-SGT Enhancement Mode MOSFET** 

#### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40			<b>&gt;</b>	
D	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =12A		6.9	8.5	<b></b> 0	
R <sub>DS(ON)</sub>	Static Diain-Source Off-Resistance-	V <sub>GS</sub> =4.5V , I <sub>D</sub> =10A		10.0	15	mΩ	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250uA$	1.35		3	V	
	Drain Source Leekage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1		
I <sub>DSS</sub> D	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	uA	
Igss	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V			±100	nA	
Rg	Gate Resistance V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz			1.7		Ω	
Qg	Total Gate Charge (4.5V)			5.8			
Qgs	Gate-Source Charge	V <sub>DS</sub> =20V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =12A		3		nC	
$Q_{gd}$	Gate-Drain Charge			1.2			
T <sub>d(on)</sub>	Turn-On Delay Time			14.3			
Tr	Rise Time			5.6			
$T_{d(off)}$	Turn-Off Delay Time	I <sub>D</sub> =1A		20		ns	
T <sub>f</sub>	Fall Time			11			
Ciss	Input Capacitance			690			
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		193		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			38			

#### **Diode Characteristics**

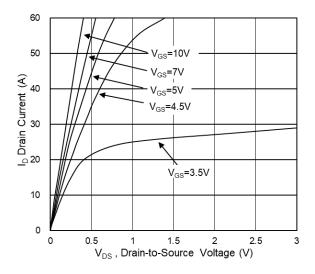
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ls	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-		40	Α
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1	٧

#### Note

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =25V,  $V_{GS}$ =10V, L=0.1mH,  $I_{AS}$ =31A
- 4. The power dissipation is limited by 150°C junction temperature
- 5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

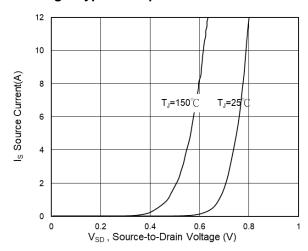


Fig.3 Source Drain Forward Characteristics

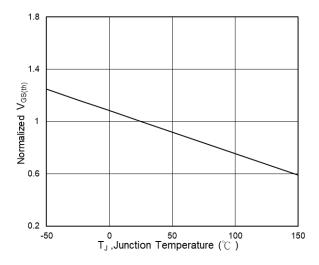


Fig.5 Normalized  $V_{\text{GS(th)}}$  vs  $T_{\text{J}}$ 

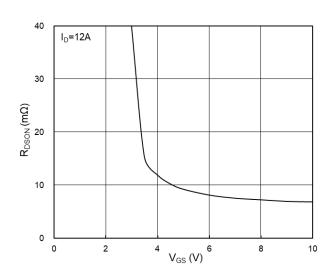


Fig.2 On-Resistance vs G-S Voltage

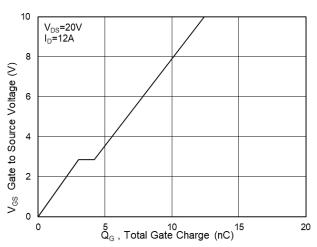


Fig.4 Gate-Charge Characteristics

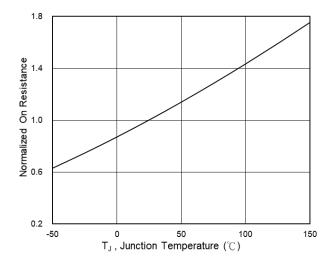
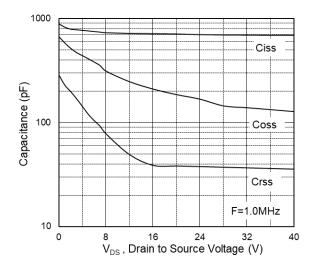


Fig.6 Normalized R<sub>DSON</sub> vs T<sub>J</sub>



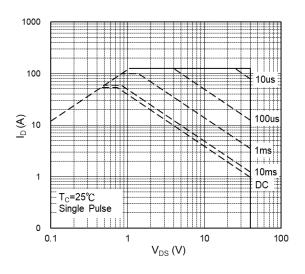
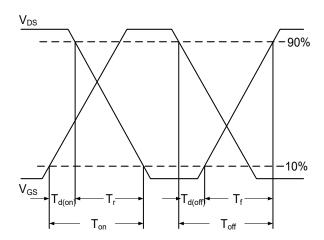


Fig.7 Capacitance Fig.8 Safe Operating Area Normalized Thermal Response (Reuc) **DUTY=0.5** 0.3 0.1 0.05 0.02 0.01  $D = T_{ON}/T$ SINGLE PUL  $T_J peak = T_C + P_{DM} x R_{\theta JC}$ 0.01 0.00001 0.0001 0.001 0.01 0.1 t, Pulse Width (s)

Fig.9 Normalized Maximum Transient Thermal Impedance





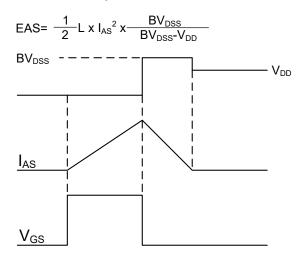
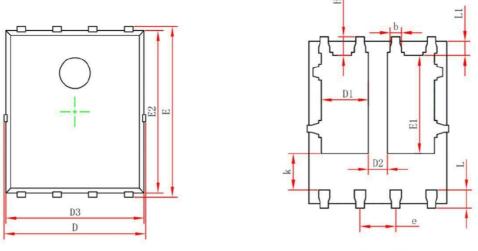


Fig.11 Unclamped Inductive Waveform

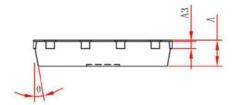


## Package Mechanical Data-DFN5X6B-8L



**Top View** 

**Bottom View** 



Side View

Symbol	Dimensions	In Millimeters	Dimension	s In Inches
	Min.	Max.	Min.	Max.
Α	0.900	1.000	0.035	0.039
A3	0.154	AREF.	0.006	REF.
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
е	1.270	TYP.	0.050	TYP.
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
Н	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

#### NVMFD5C466NWFT1G

**Dual N-SGT Enhancement Mode MOSFET** 

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