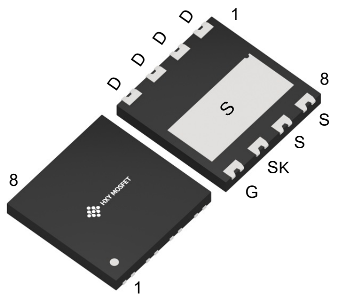
General Description

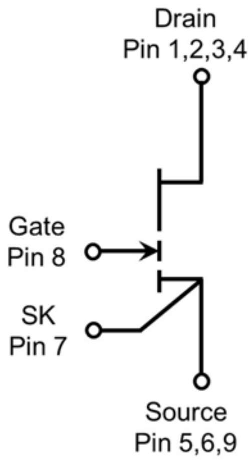
650V GaN-on-Silicon Enhancement-mode
Power Transistor in Dual Flat No-lead Package
(DFN) with 8 mm × 8 mm size .



DFN8X8
(DFN-8(8X8))

Features

- Enhancement-mode transistor - normally-OFF power switch
- Ultra-high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High-density power conversion
- High-efficiency power conversion

Gate	8
Drain	1, 2, 3, 4
Kelvin Source	7
Source	5, 6, 9

Maximum Ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum rating

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 µA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
Continuous current, drain-source	I_D	-	-	17	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	32	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	18	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous [3]	V_{GS}	-1.4	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	113	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.

2. Pulse width = 10 µs.

3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

Thermal Characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.1	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

Electrical Characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.7	2.5	V	I_D = 17.2 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 17.2 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.6	20	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	1	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	40	200	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	100	140	mΩ	V_{GS} = 6 V; I_D = 5 A; T_j = 25 °C
		-	200	-	mΩ	V_{GS} = 6 V; I_D = 5 A; T_j = 125 °C
Gate resistance	R_G	-	3.5	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	125	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	40	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.5	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	53	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	81	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	33	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	3.3	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 5 A
Gate-source charge	Q_{GS}	-	0.3	-	nC	
Gate-drain charge	Q_{GD}	-	1.25	-	nC	
Gate plateau voltage	V_{Plat}	-	2.4	-	V	V_{DS} = 400 V; I_D = 5 A

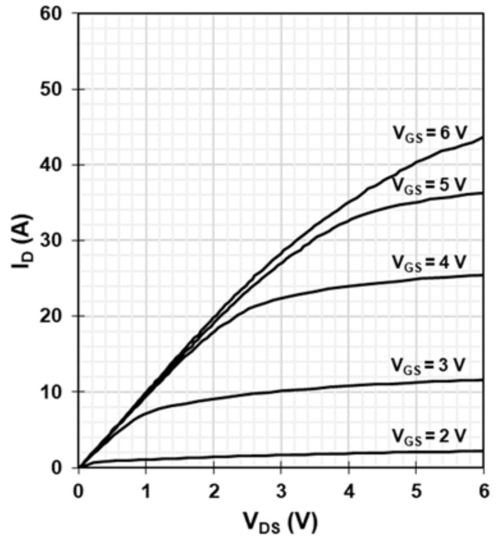
Table 8 Reverse conduction characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.5	-	V	V_{GS} = 0 V; I_{SD} = 5 A
Pulsed current, reverse	$I_{S, pulse}$	-	28	-	A	V_{GS} = 6 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} = 5 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Electrical Characteristics Diagrams

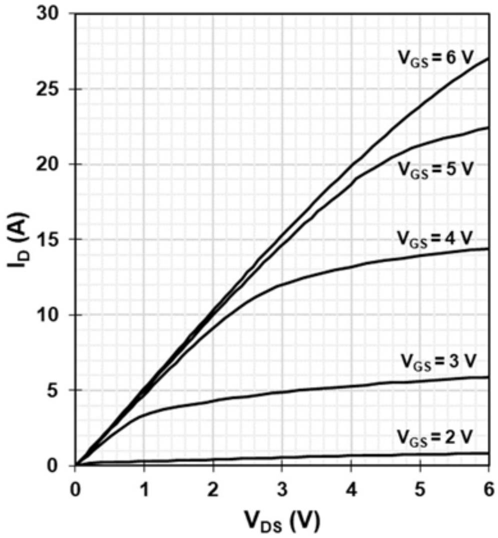
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



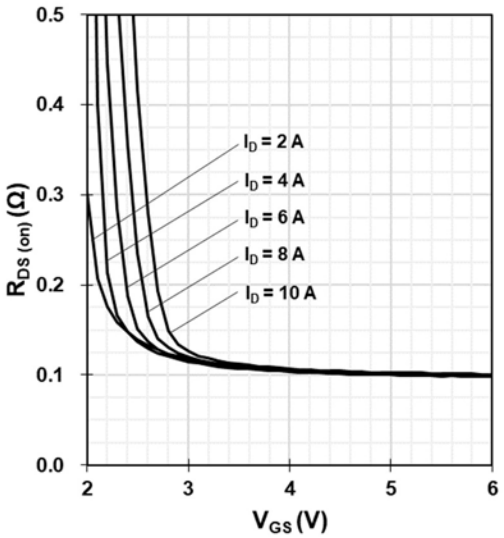
I_D = f(V_{DS}, V_{GS}); T_j = 25 °C

Figure 2 Typ. output characteristics



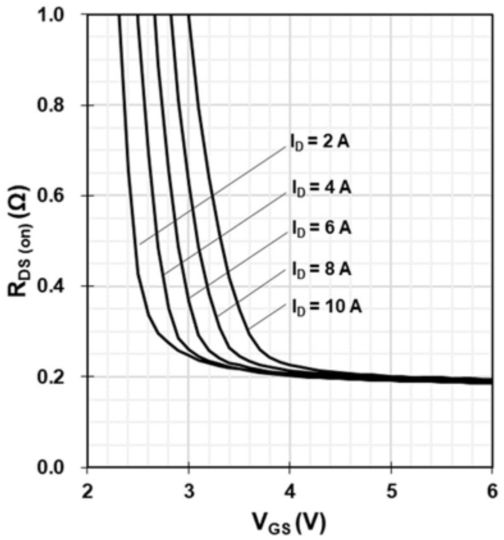
I_D = f(V_{DS}, V_{GS}); T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



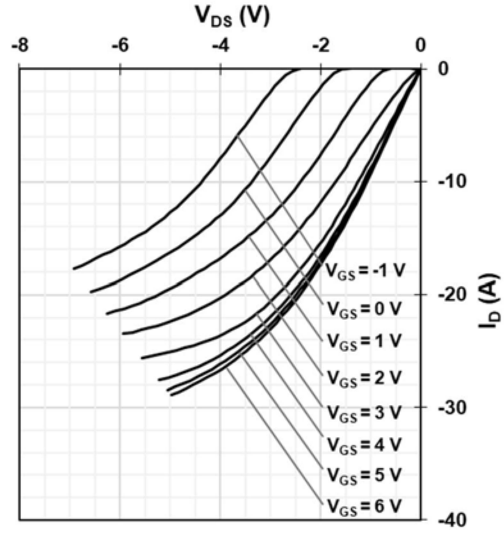
$R_{DS(on)}$ = f(I_{DS},V_{GS}); T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



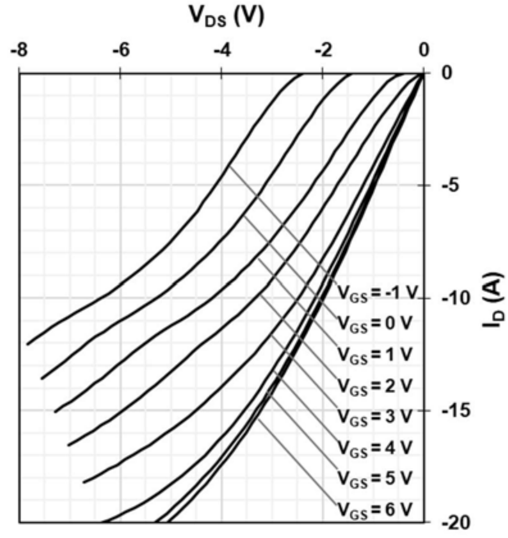
$R_{DS(on)}$ = f(I_{DS},V_{GS}); T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



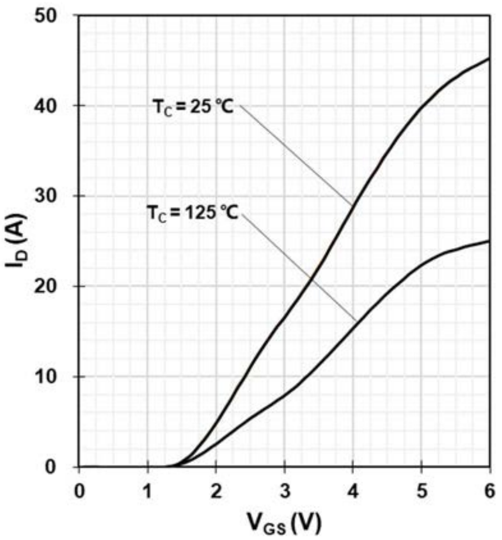
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



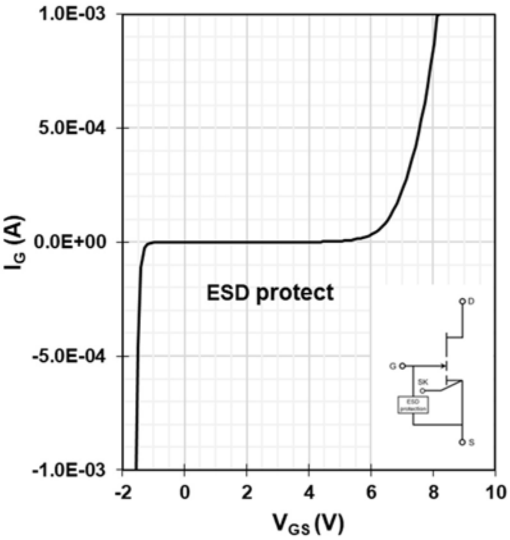
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 7 Typ. transfer characteristics



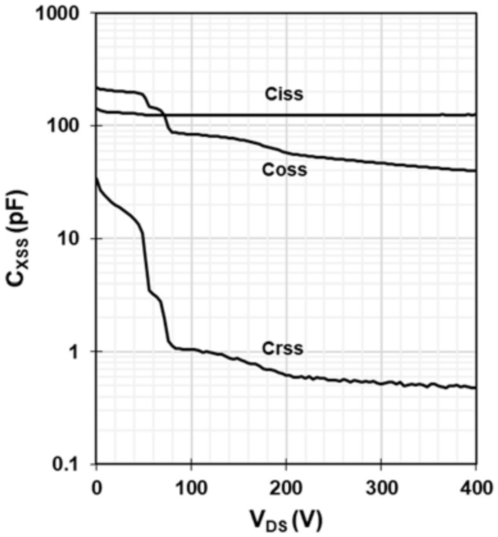
$I_D = f(V_{GS})$; V_{DS} = 5 V

Figure 8 Typ. gate-to-source leakage



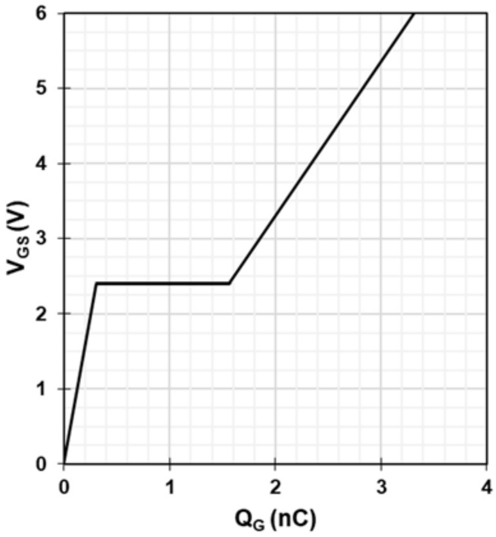
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit; V_D = open

Figure 9 Typ. capacitances



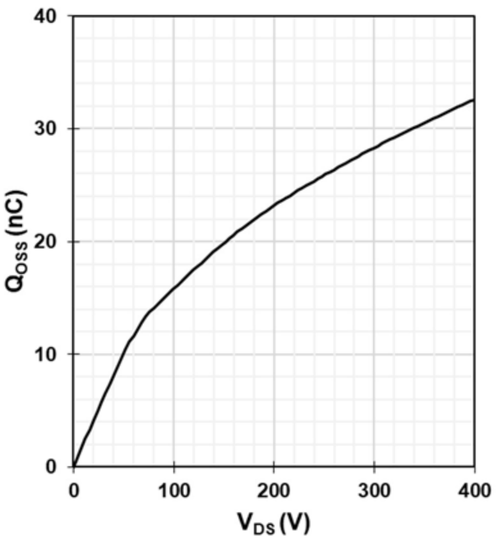
$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 10 Typ. gate charge



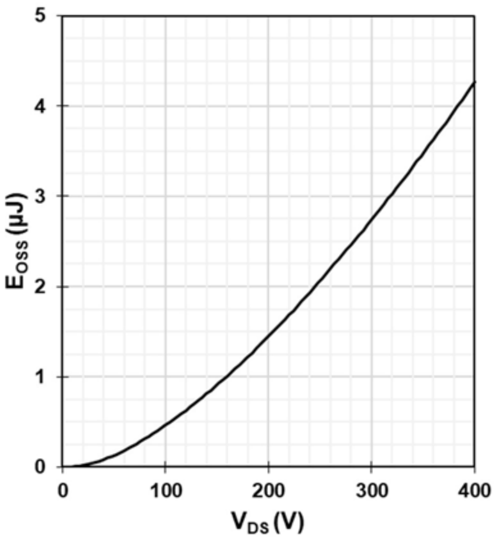
$V_{GS} = f(Q_G)$; $V_{DC\text{-}LINK} = 400$ V; $I_D = 5$ A

Figure 11 Typ. output charge



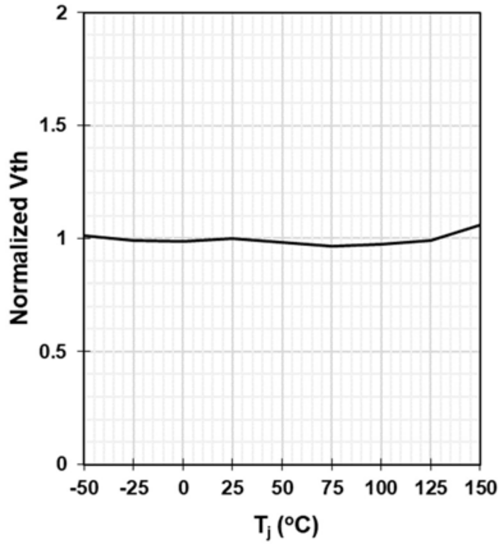
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 12 Typ. C_{OSS} stored energy



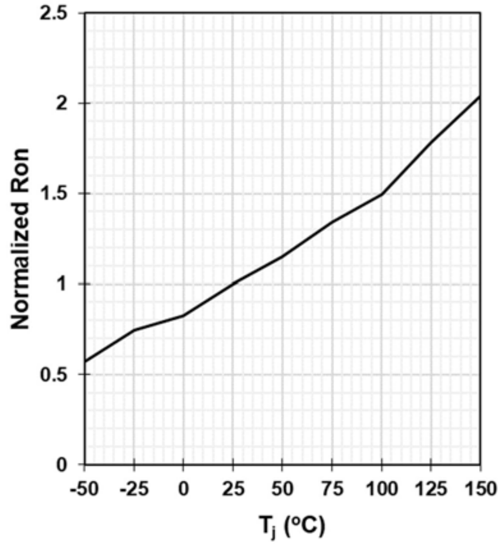
$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 13 Gate threshold voltage



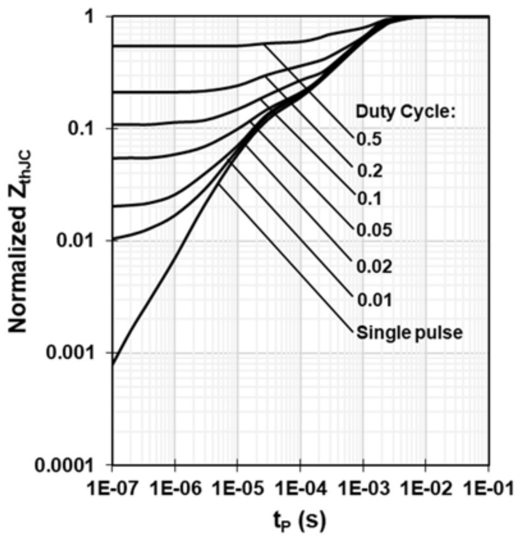
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 17.2 mA

Figure 14 Drain-source on-state resistance



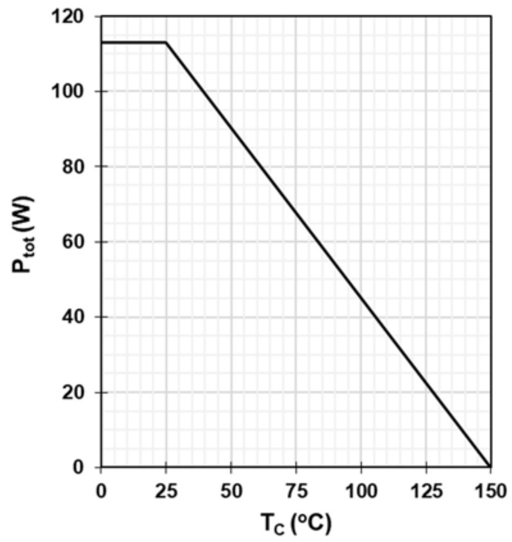
$R_{DS(on)} = f(T_j)$; I_D = 5 A; V_{GS} = 6 V

Figure 15 Max. transient thermal impedance



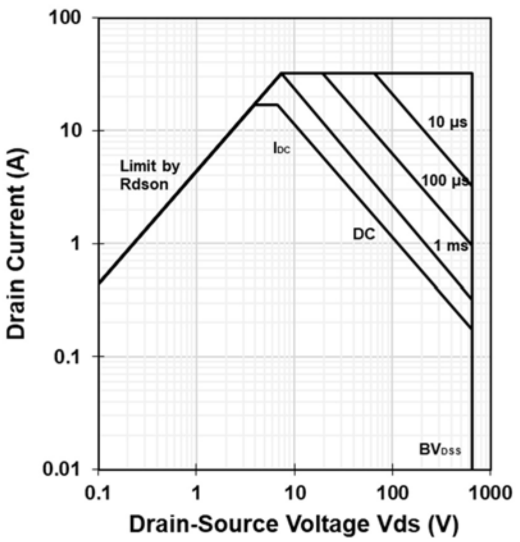
$Z_{thJC} = f(t_P, D)$

Figure 16 Power dissipation



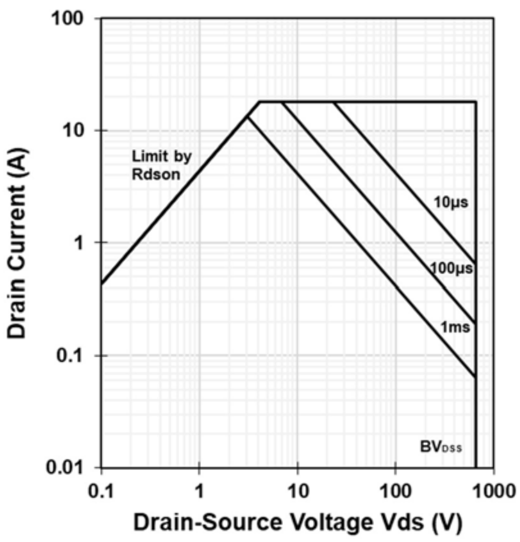
$P_{tot} = f(T_C)$

Figure 17 Safe operating area



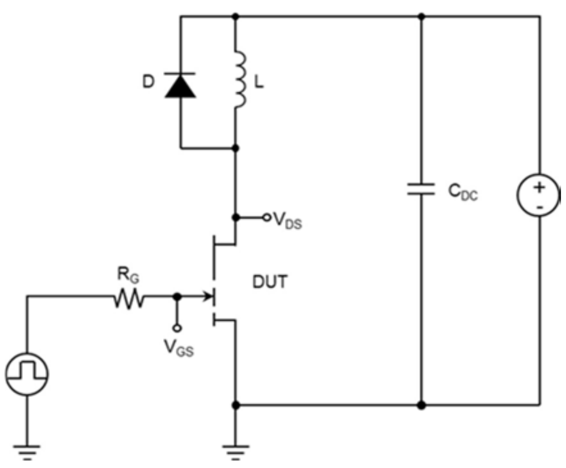
$I_D = f(V_{DS})$; T_C = 25 °C

Figure 18 Safe operating area



$I_D = f(V_{DS})$; T_C = 125 °C

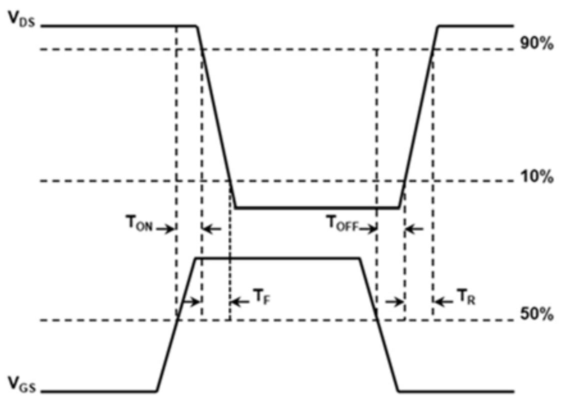
Figure 19 Max. transient thermal impedance



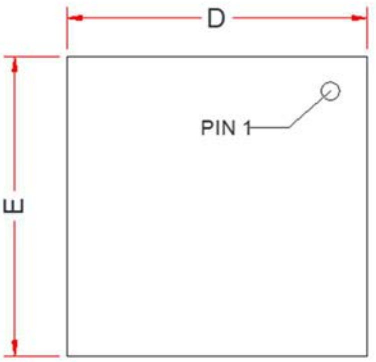
V_{DS} = 400 V, I_D = 10 A, L = 318 µH, V_{GS} = 6 V,

R_{on} = 10 Ω, R_{off} = 2 Ω

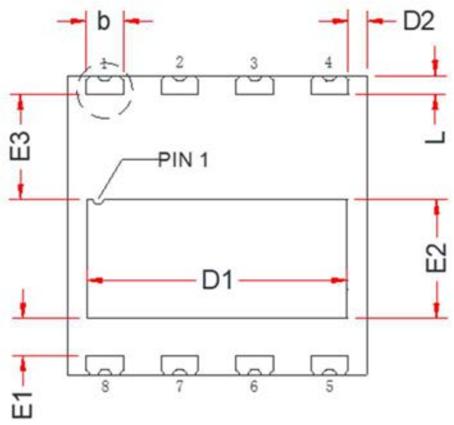
Figure 20 Typ. switching times waveform



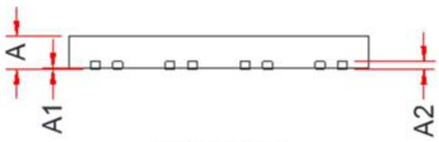
Package Outlines



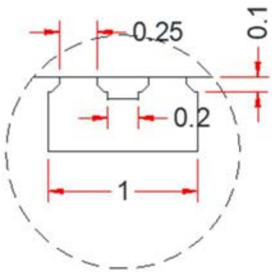
TOP VIEW



BOTTOM VIEW



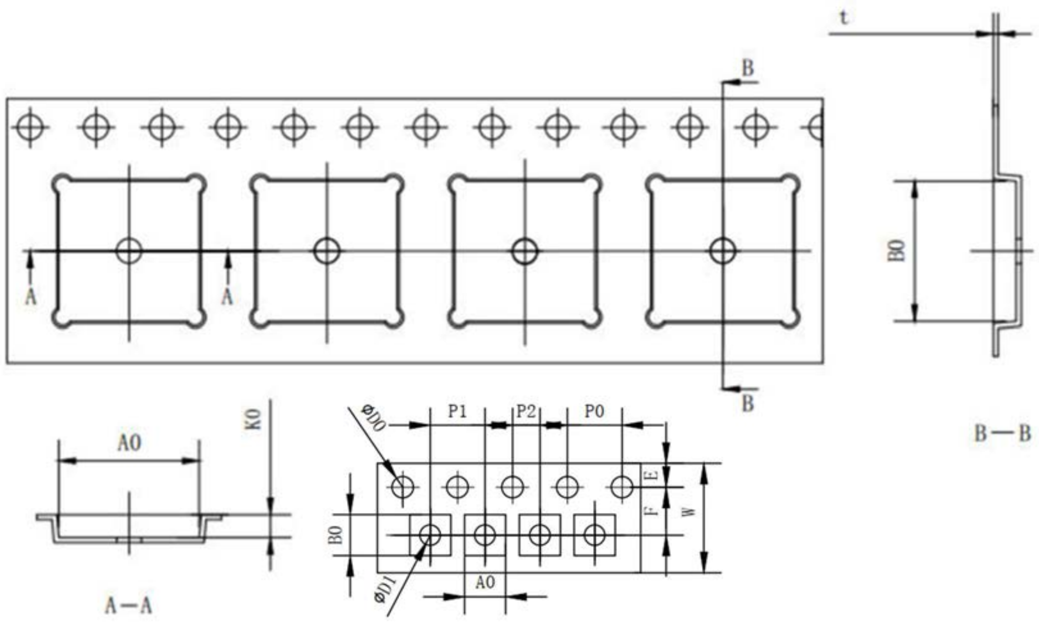
SIDE VIEW



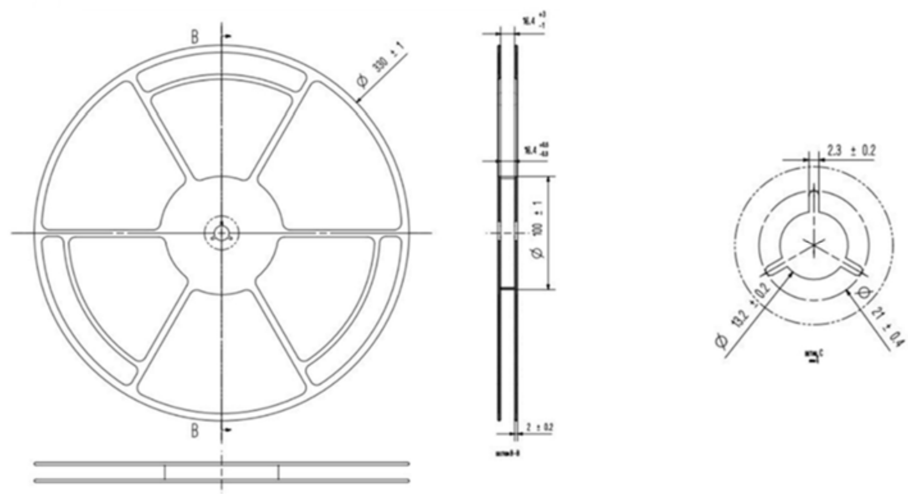
LEAD DETAIL

	MIN	MID	MAX
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.95	1.00	1.05
D	8.00BSC		
D1	6.84	6.94	7.04
D2	0.40	0.50	0.60
E	8.00BSC		
E1	0.90	1.00	1.10
E2	3.10	3.20	3.30
E3	2.70	2.80	2.90
e	2.00BSC		
L	0.40	0.50	0.60

Reel Information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	12.00±0.10
F	7.50±0.10	A0	8.30±0.10
D0	1.50±0.10	B0	8.30±0.10
D1	1.50±0.10	K0	1.10±0.10
P0	4.00±0.10	T	0.30±0.05
P2	2.00±0.10		



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