

Description

The IRF7101PBF uses advanced trench technology and design to provide excellent $R_{\text{DS(ON)}}$ with low gate charge. It can be used in a wide variety of applications.

General Features

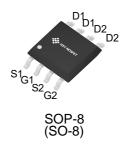
 $V_{DS} = 20V, I_{D} = 4A$

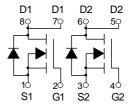
 $R_{DS(ON)} < 45m\Omega$ @ $V_{GS}=4.5V$

 $R_{DS(ON)} < 55 m\Omega$ @ $V_{GS}=2.5V$

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply





Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRF7101PBF	SOP-8(SO-8)	HXY MOSFET	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	Vgs	±10	V
Drain Current-Continuous	I_D	4	Α
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	2.8	Α
Pulsed Drain Current	I _{DM}	25	Α
Maximum Power Dissipation	P _D	1.25	W
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 150	${\mathbb C}$
Thermal Resistance, Junction-to-Ambient (Note 2)	R _{0JA}	100	°C/W



Electrical Characteristics (T_A=25 ℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	22	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} =20V, V_{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	$V_{GS}=\pm10V, V_{DS}=0V$	-	-	±100	nA
On Characteristics (Note 3)			•			•
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	0.5	0.7	1.2	V
Proje Course On Otata Projetana	5	V _{GS} =4.5V, I _D =4A	-	35	45	- mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =2.5V, I _D =2A	-	40	55	
Forward Transconductance	g FS	V _{DS} =5V,I _D =6A	20	-	-	S
Dynamic Characteristics (Note4)	<u> </u>		<u> </u>	I		I
Input Capacitance	C _{lss}	V _{DS} =10V,V _{GS} =0V,	-	290	-	PF
Output Capacitance	Coss		-	60	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	30	-	PF
Switching Characteristics (Note 4)			•			•
Turn-on Delay Time	t _{d(on)}		-	8	-	nS
Turn-on Rise Time	t _r	V_{DD} =10 V , I_{D} =1 A	-	9	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GEN} =4.5 V , R_G =6 Ω	-	15	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Qg	V _{DS} =10V,I _D =3A,	-	10	-	nC
Gate-Source Charge	Q _{gs}		-	1.5	-	nC
Gate-Drain Charge	Q_{gd}	V _{GS} =4.5V	-	1.6	-	nC
Drain-Source Diode Characteristics	· ·					
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =1.7A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	6	Α

Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production



Typical Characteristics

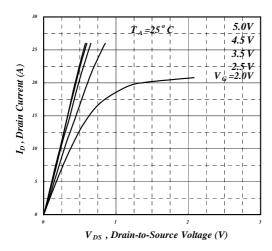


Fig 1. Typical Output Characteristics

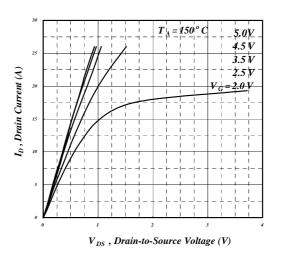


Fig 2. Typical Output Characteristics

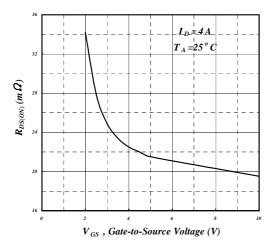


Fig 3. On-Resistance v.s. Gate Voltage

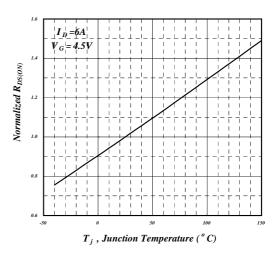


Fig 4. Normalized On-Resistance v.s. Temperature

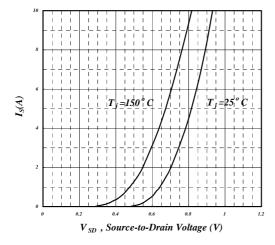


Fig 5. Forward Characteristic of Reverse Diode

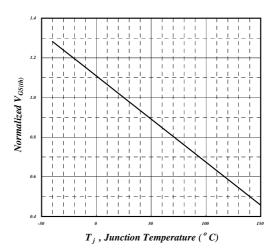


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature

=1.0MHz



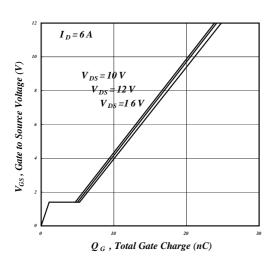


Fig 7. Gate Charge Characteristics

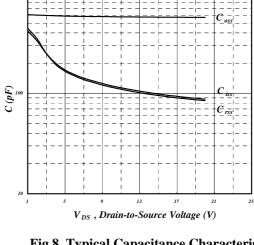


Fig 8. Typical Capacitance Characteristics

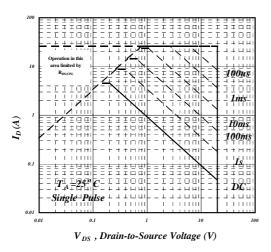


Fig 9. Maximum Safe Operating Area

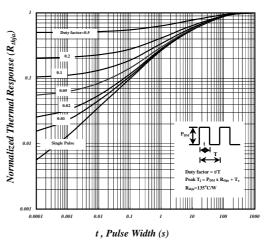


Fig 10. Effective Transient Thermal Impedance

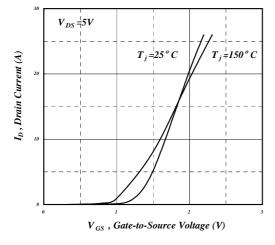


Fig 11. Transfer Characteristics

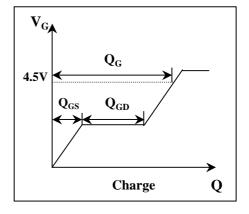
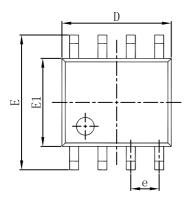
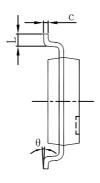


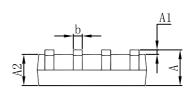
Fig 12. Gate Charge Waveform



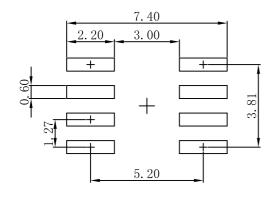
SOP-8(SO-8) Package Outline Dimensions







Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	1. 350	1. 750	0.053	0.069	
A1	0.100	0. 250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
c	0.170	0.250	0.007	0.010	
D	4.800	5.000	0.189	0.197	
e	1.270 (BSC)		0.050 (BSC)		
E	5.800	6. 200	0. 228	0. 244	
E1	3.800	4.000	0.150	0.157	
L	0.400	1. 270	0.016	0.050	
θ	0°	8°	0°	8°	



- Note: 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
 3.The pad layout is for reference purposes only.



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