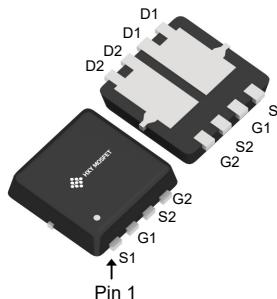




Description

The SI7218DN-T1-E3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 30V$ $I_D = 24A$

$R_{DS(ON)} < 18m\Omega$ @ $V_{GS}=10V$

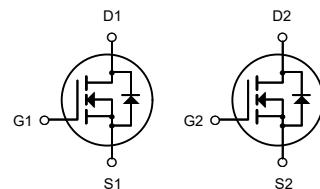
Application

Lithium battery protection

Wireless impact

Mobile phone fast charging

DFN3X3B-8L
(PowerPAK1212-8)



Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI7218DN-T1-E3	DFN3X3B-8L (PowerPAK1212-8)	HXY MOSFET	5000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	24	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	A
IMD	Pulsed Drain Current ²	56	A
EAS	Single Pulse Avalanche Energy ³	22.1	mJ
IAS	Avalanche Current	21	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	20.8	W
$P_D @ T_c=100^\circ C$	Total Power Dissipation ⁴	1.67	W
TSTG	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
R _{θJA}	Thermal Resistance Junction-Ambient ¹	75	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	6	°C/W



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
△BV _{DSS} /△T _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.022	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =10A	---	15	18	mΩ
		V _{GS} =4.5V, I _D =5A	---	25	30	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	---	2.5	V
△V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-5.1	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =10A	---	4.5	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.5	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =20V, V _{GS} =4.5V, I _D =10A	---	7.2	---	nC
Q _{gs}	Gate-Source Charge		---	1.4	---	
Q _{gd}	Gate-Drain Charge		---	2.2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =12V, V _{GS} =10V, R _G =3.3Ω	---	4.1	---	ns
T _r	Rise Time		---	9.8	---	
T _{d(off)}	Turn-Off Delay Time		---	15.5	---	
T _f	Fall Time		---	6.0	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	572	---	pF
C _{oss}	Output Capacitance		---	81	---	
C _{rss}	Reverse Transfer Capacitance		---	65	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	28	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	56	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _s =1A, T _J =25°C	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width \leq 300us, duty cycle \leq 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.



Typical Characteristics

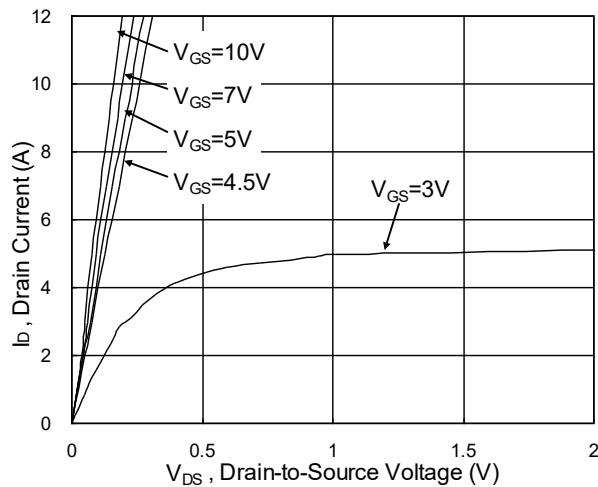


Fig.1 Typical Output Characteristics

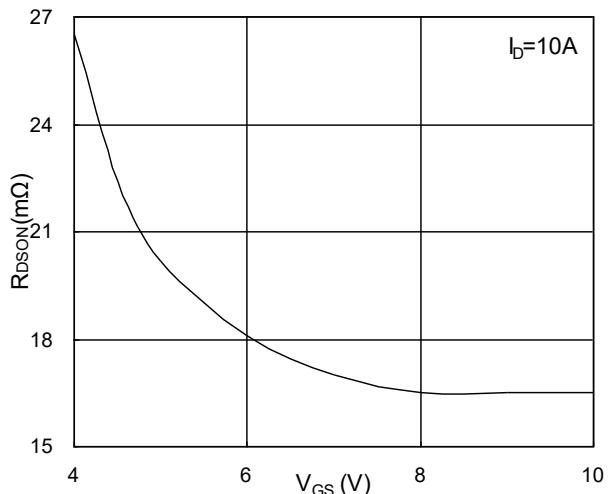


Fig.2 On-Resistance vs. Gate-Source

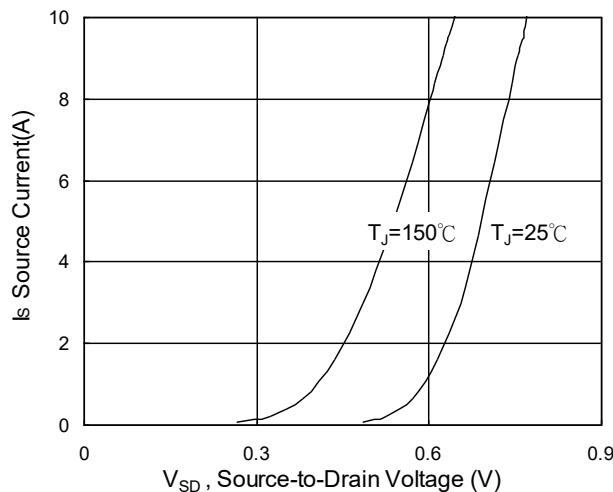


Fig.3 Forward Characteristics Of Reverse

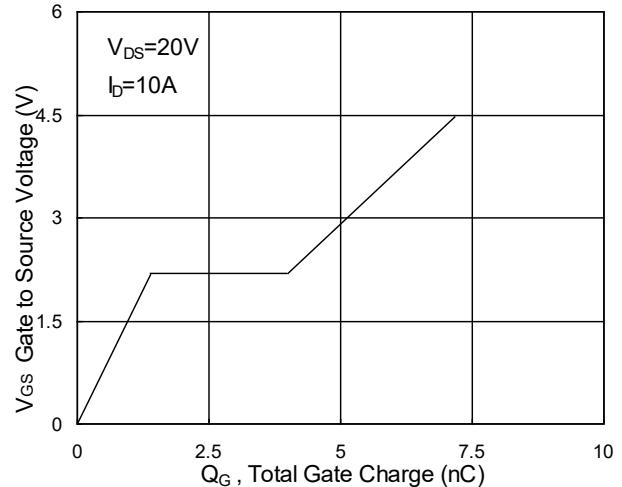


Fig.4 Gate-Charge Characteristics

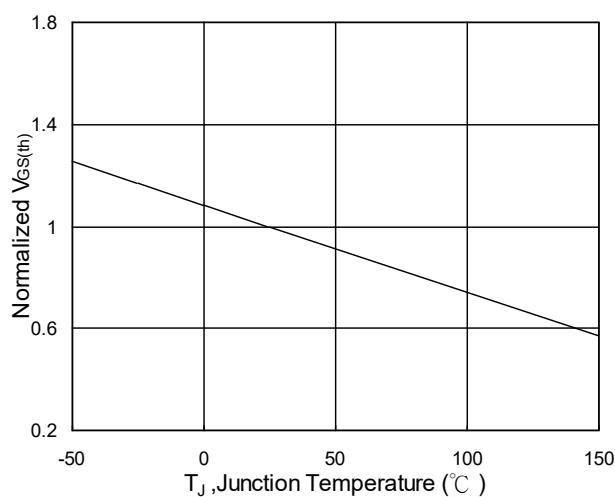


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

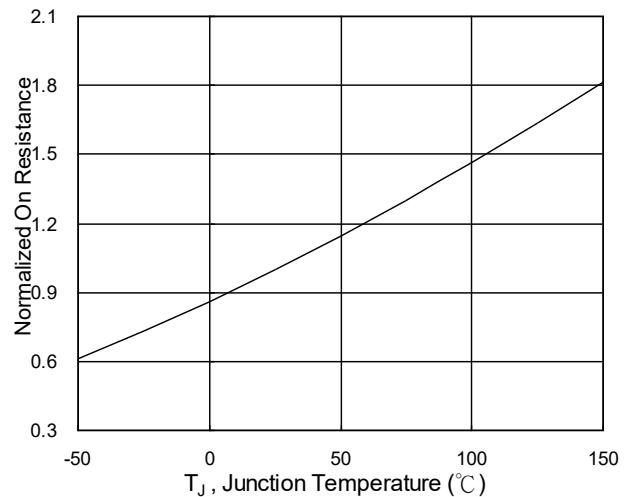


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

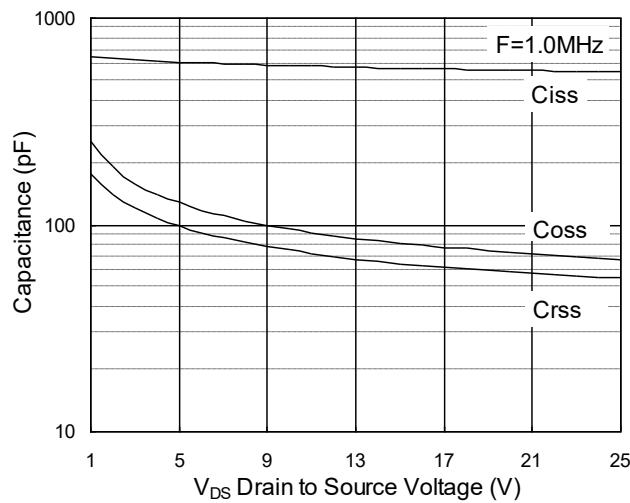


Fig.7 Capacitance

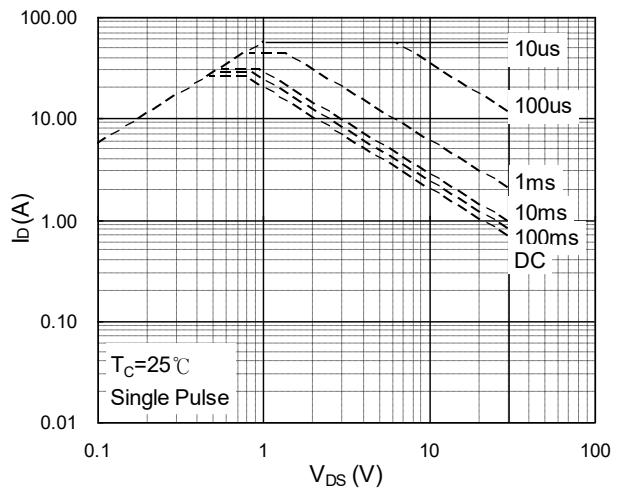


Fig.8 Safe Operating Area

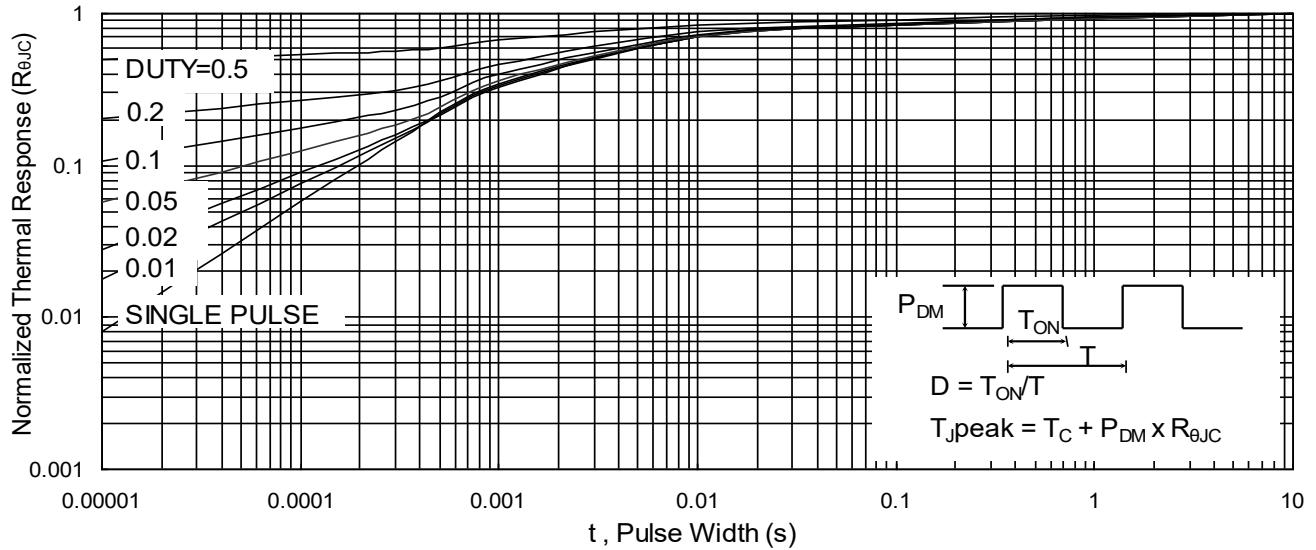


Fig.9 Normalized Maximum Transient Thermal Impedance

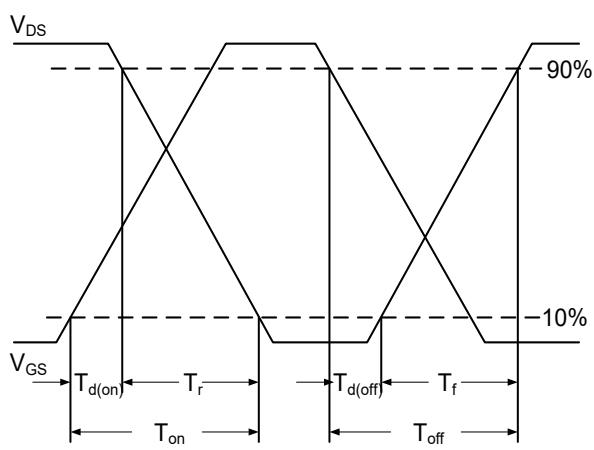


Fig.10 Switching Time Waveform

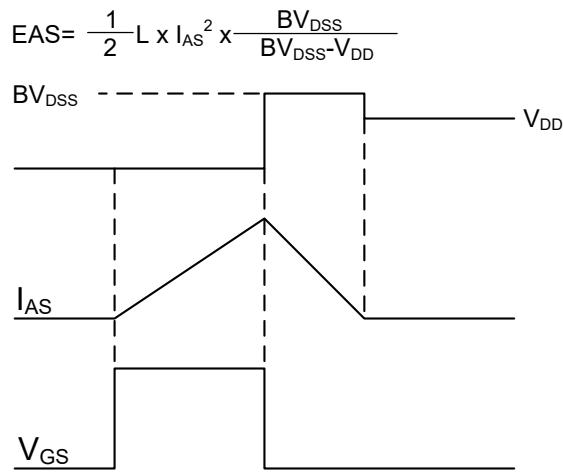
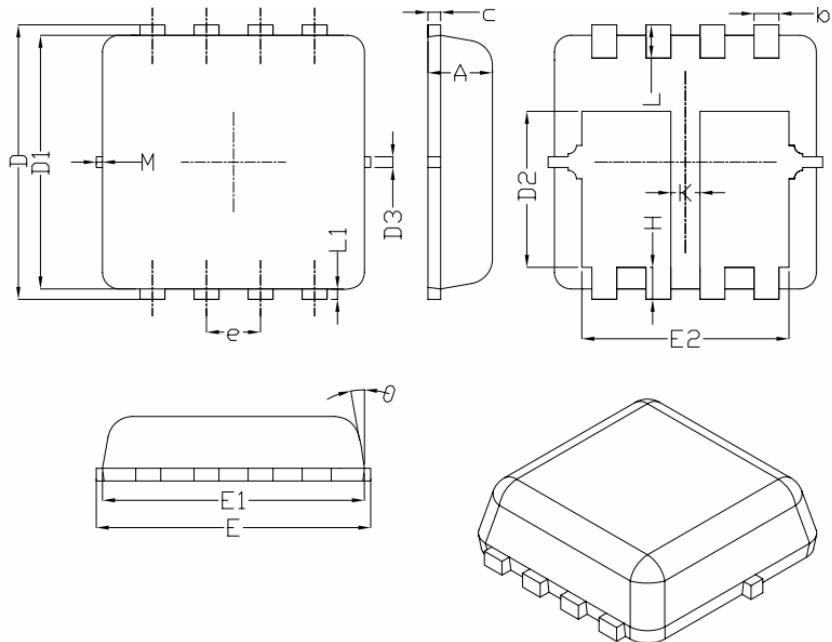


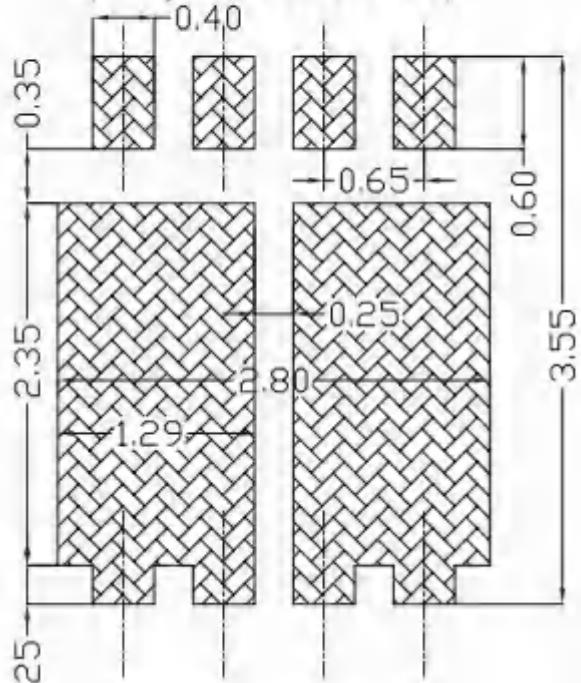
Fig.11 Unclamped Inductive Switching Waveform



DFN3X3B-8L(PowerPAK1212-8) Package Information



Land Pattern (Only for Reference)



SYMBOL	DIMENSIONAL REQUIREMENTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
K	0.30	---	---
θ	---	10°	12°
M	*	*	0.15

* Not specified



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