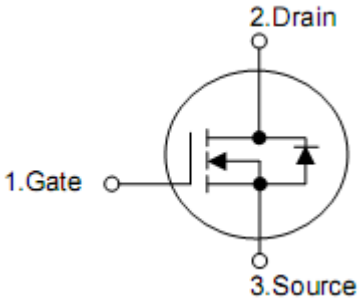
1. Features

- Advanced Trench technology
- $R_{DS(ON)}$=7.5mΩ (typ.) @ V_{GS}=10V
- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- 100% ΔVds TESTED
- 100% UIS TESTED

2. Pin configuration

TO-252



Pin	Function
1	Gate
2	Drain
3	Source

3. Ordering Information

Part Number	Package	Brand
KIA50N06DD	TO-252	KIA

4. Absolute maximum ratings

T_A=25°C unless otherwise specified

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage (V_{GS}=0V）		V_{DS}	60	V
Gate-to-Source Voltage (V_{DS}=0V）		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25°C	I_D	50	A
	T_C=100°C	I_D	37.5	A
Pulsed Drain Current @ Current-Pulsed [2]		I_{DM}	260	A
Total Power Dissipation (T_C=25°C) [4]		P_D	88	W
Avalanche Energy [3]		EAS	225	mJ
Operation Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

5. Thermal characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance, Junction-to-Case [1]	$R_{\theta JC}$	1.7	°C/W

6. Electrical characteristics

(T_A=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	60	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V,T_C=25°C	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250uA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance 2)	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	7.5	9.0	mΩ
		V_{GS}=4.5V, I_D=15A	-	9.0	12	mΩ
Gate Resistance	R_g	V_{DS}=0V, V_{GS}=0V,f=1.0MHz	-	1.5	-	Ω
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V , f=1.0MHz	-	3000	-	pF
Output Capacitance	C_{oss}		-	180	-	pF
Reverse Transfer Capacitance	C_{rss}		-	150	-	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=30V, V_{GS}=10V, R_G=3.0Ω, I_D=15A	-	14	-	ns
Rise Time	t_r		-	18	-	ns
Turn-Off DelayTime	$t_{d(off)}$		-	95	-	ns
Fall Time	t_f		-	30	-	ns
TotalGate Charge	Q_g	V_{DS}=30V, V_{GS}=10V , I_D=15A	-	64	-	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain Charge	Q_{gd}		-	16	-	nC
Source-Drain Current (Body Diode) 1),5)	I_{SD}	—	-	-	50	A
Diode Forward Voltage 2)	V_{SD}	V_{GS}=0V, I_{SD}=20A,T_J=25°C	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=20A, di/dt=100A/μs	-	25	-	nS
Reverse Recovery Charge	Q_{rr}		-	23	-	nC
Forward Turn-on Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS +LD)				

Notes:
1) The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2) The data tested by pulsed, pulse width≤300us, duty cycle≤2%.
3) The test condition is V_{DD}=36V, V_{GS}=10V, L=0.5mH, I_{AS}=30A.
4) The power dissipation is limited by 175°C junction temperature.
5) The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

7. Typical Characteristics

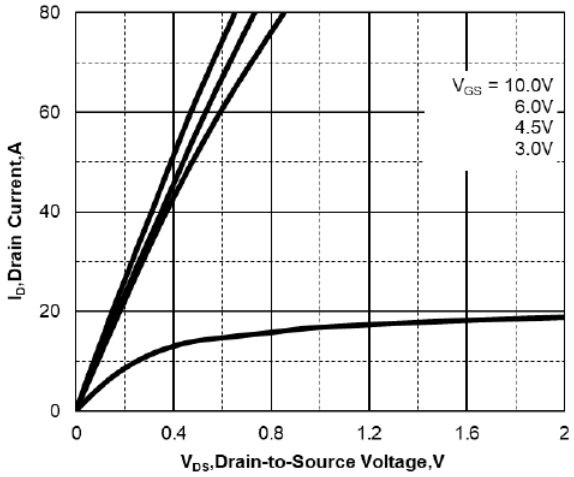


Fig1: Typical Output Characteristics

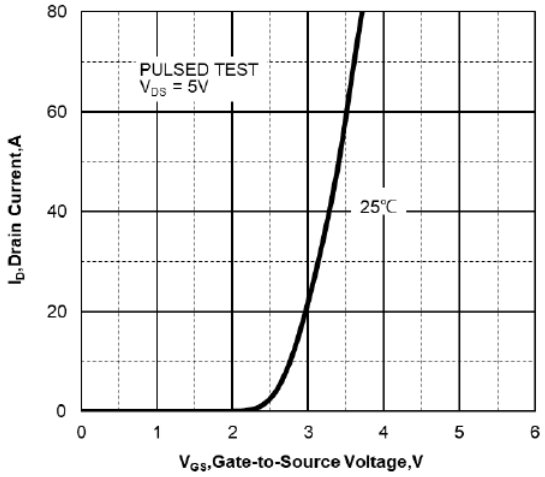


Fig 2: Typical Transfer Characteristics

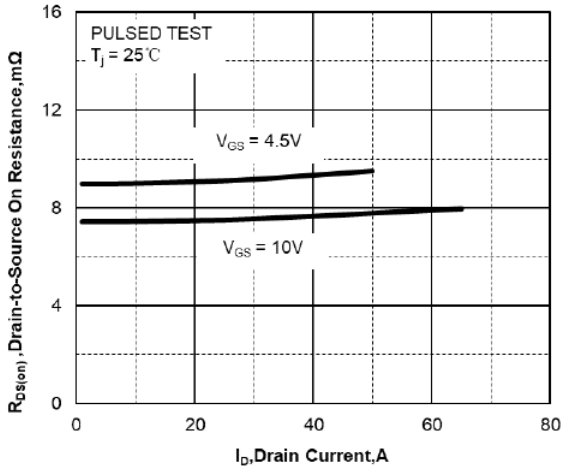


Fig 3: On-Resistance VS. Drain Current

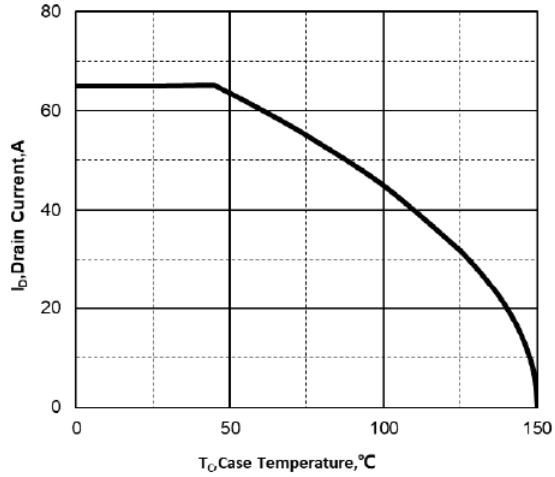


Fig 4: Maximum Continuous Drain Current VS. Case Temperature

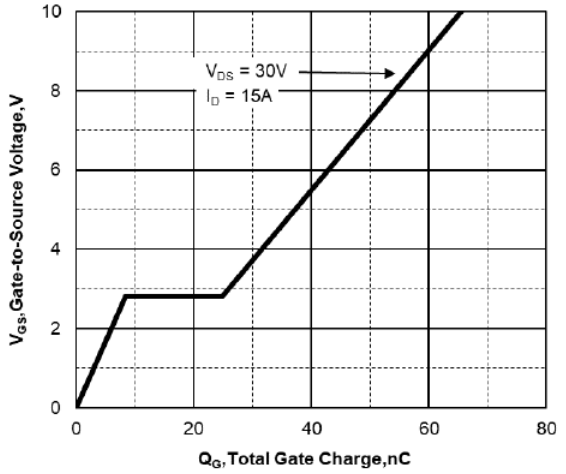


Fig 5: Gate Charge Characteristics

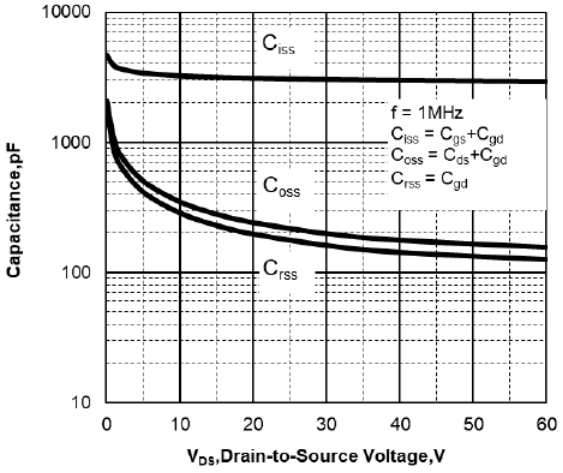


Fig 6: Capacitance Characteristics

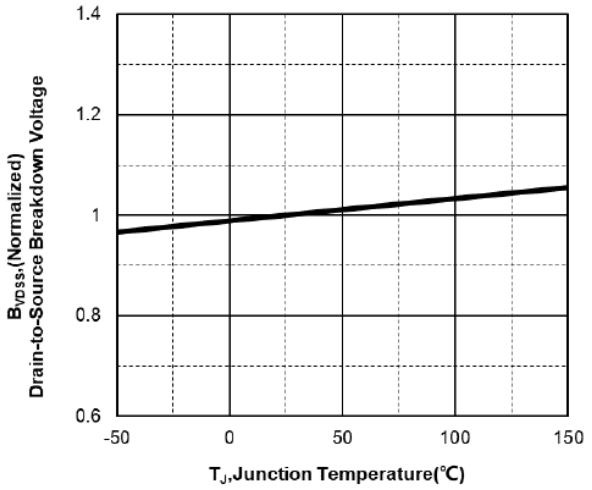


Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

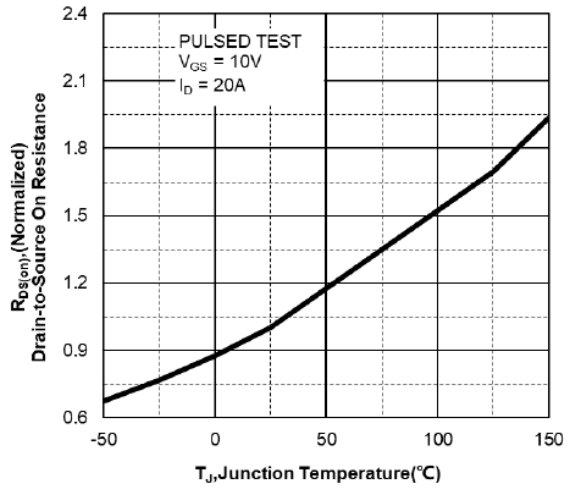


Fig 8: Normalized on Resistance VS. Junction Temperature

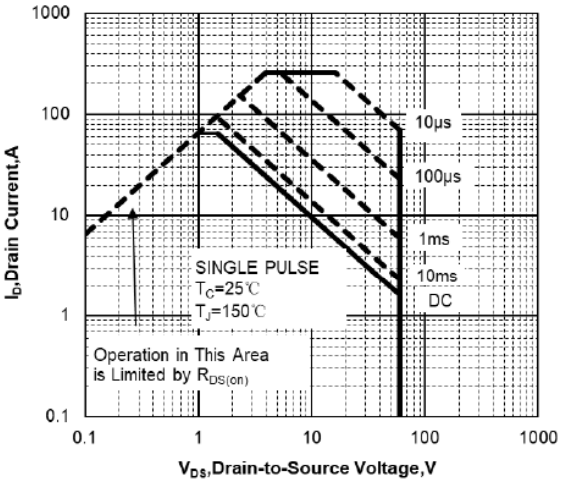


Fig 9: Maximum Safe Operating Area

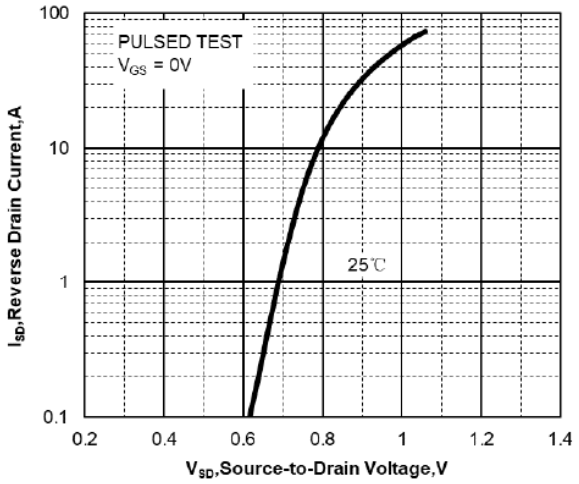


Fig 10: Body Diode Forward Characteristics

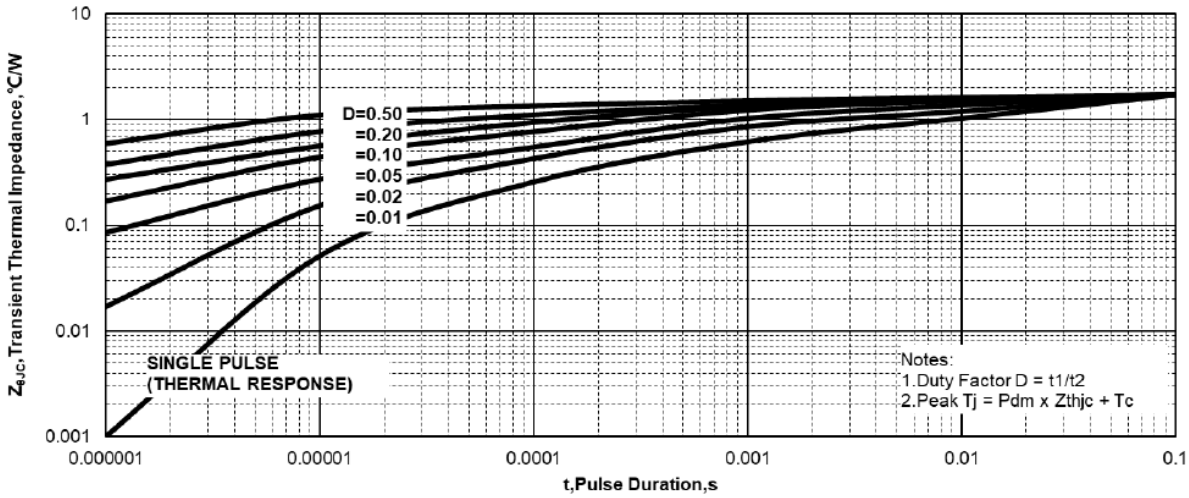


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

8. Test Circuit & Waveform

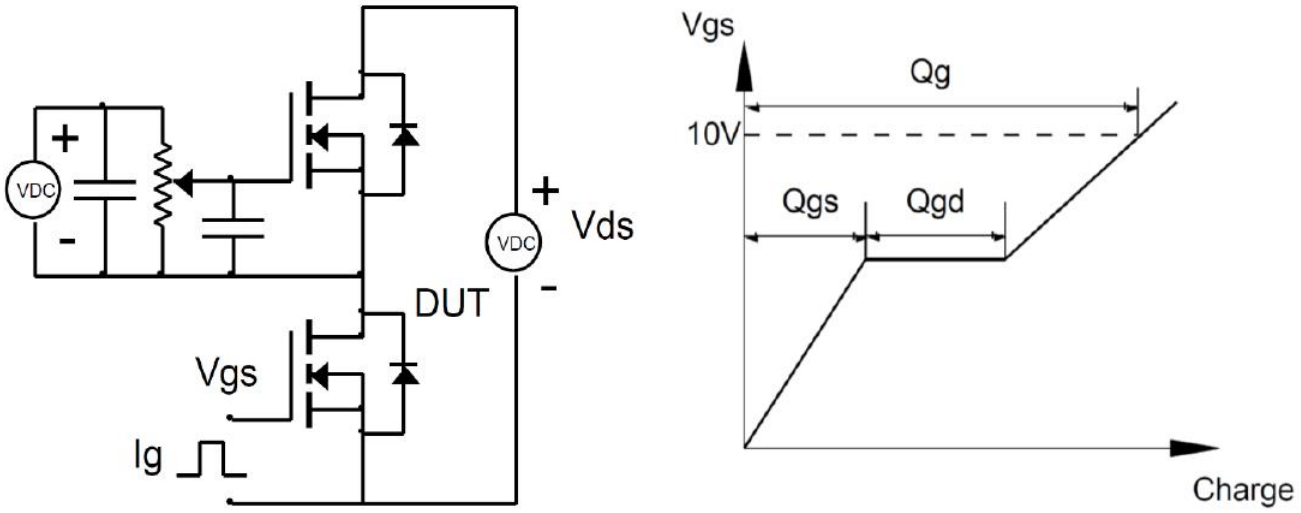


Fig 12: Gate Charge Test Circuit and Waveforms

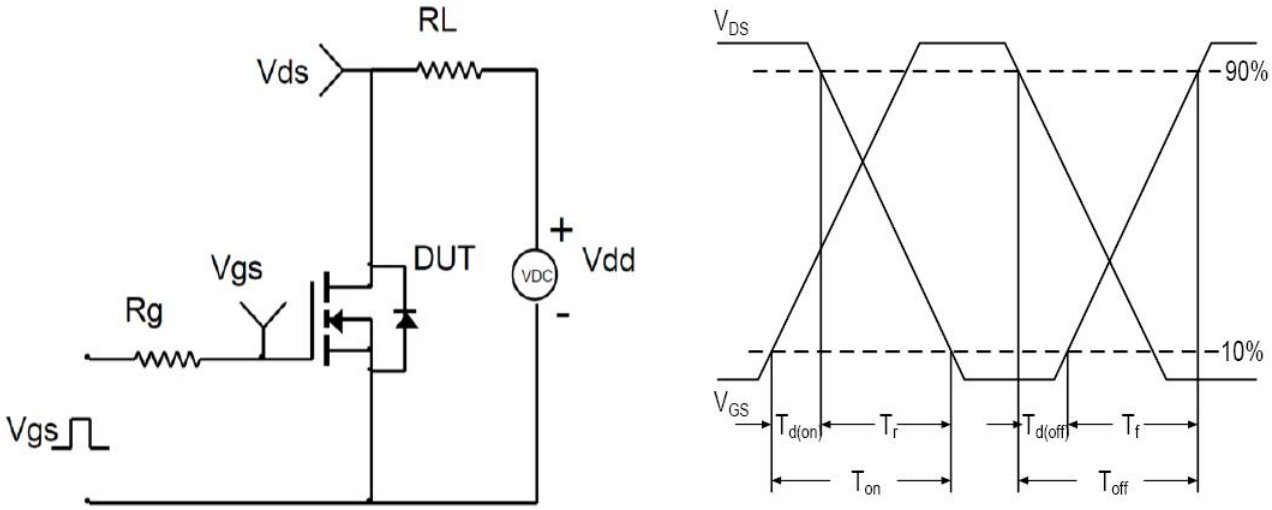


Fig 13: Resistive Switching Test Circuit and Waveforms

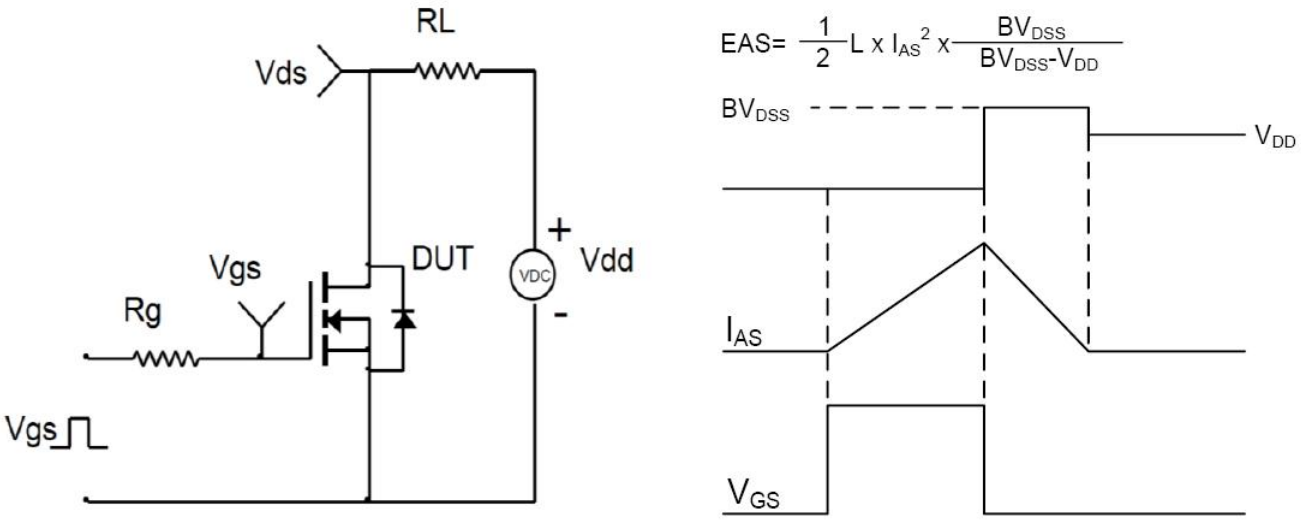


Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms