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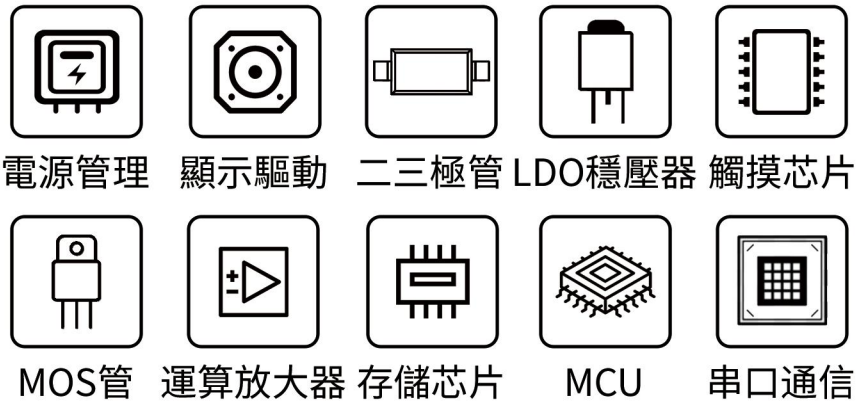


TJA1049T-3-1Z-TD

產品規格說明書

1. DESCRIPTION

The TJA1049 highspeed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, supplying the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1049 belongs to the second generation of high-speed CAN transceivers from XINLUDA Semiconductors, offering significant improvements over first-and second-generation devices such as the TJA1040. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability
- TJA1049T-3-1Z-

TDcan be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

The TJA1049 implements the CAN physical layer as defined in ISO 11898-2:2016.This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the TJA1049 an excellent choice for all types of HS-CAN networks, in nodes that require a low-power mode with wake-up capability via the CAN bus.

2. FEATURES

- Compatible with ISO 11898-2:2016
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- VIO input on TJA1049T-3-1Z-
- TDallows for direct interfacing with 3 V to 5 V microcontrollers Very low-
- current Standby mode with host and bus wake-up capability
- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)
- High ESD handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Bus-dominant time-out function in Standby mode
- Undervoltage detection on pins VCC and VIO

  Thermally protected

3. QUICK REFERENCE DATA

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	-	5.25	V
V_{IO}	supply voltage on pin V_{IO}		2.9	-	5.25	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.75	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
I_{CC}	supply current	Standby mode: TJA1049T-3-1Z-TD	-	-	10	µA
		Normal mode; bus recessive	2.5	5	10	mA
		Normal mode; bus dominant	20	45	65	mA
I_{IO}	supply current on pin V_{IO}	Standby mode	5	-	20	µA
		Normal mode; bus recessive	15	80	200	µA
		Normal mode; bus dominant	-	350	1000	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	−8	-	+8	kV
V_{CANH}	voltage on pin CANH		−58	-	+58	V
V_{CANL}	voltage on pin CANL		−58	-	+58	V
T_{vj}	virtual junction temperature		−40	-	+125	°C

4. BLOCK DIAGRAM

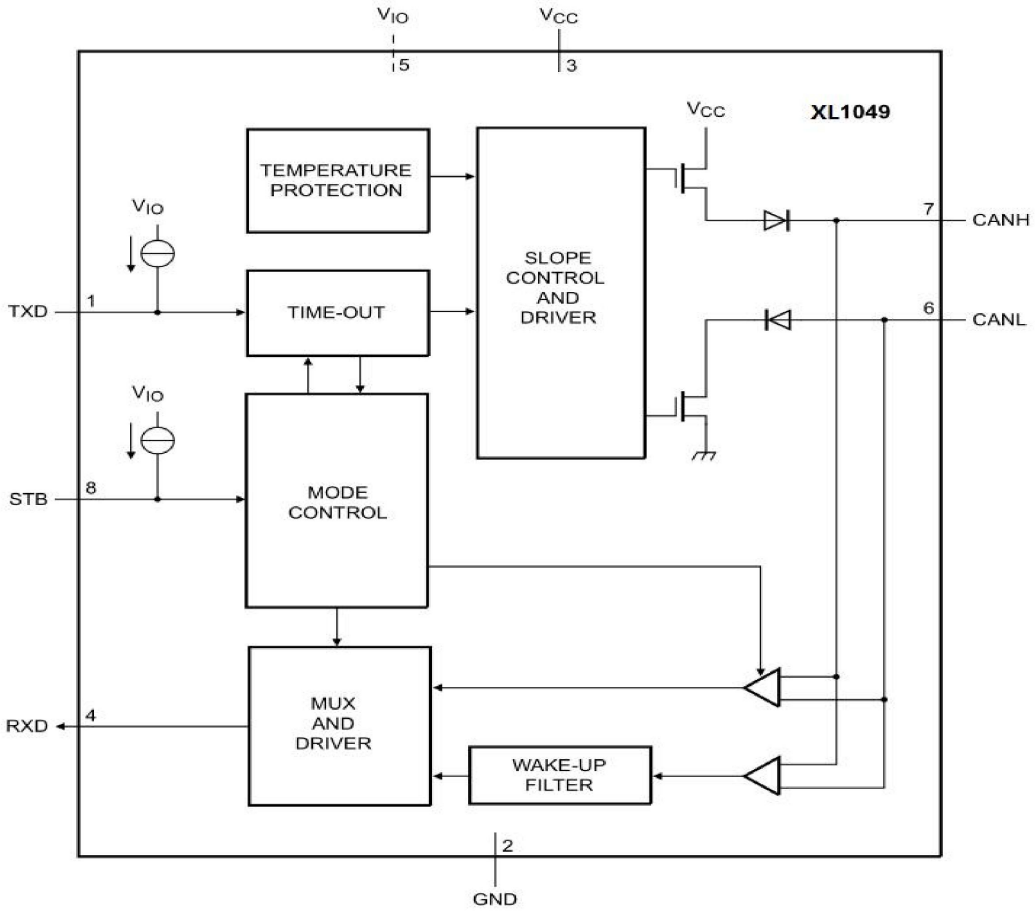


Figure 1. Block diagram

5. PINNING INFORMATION

5.1 Pinning

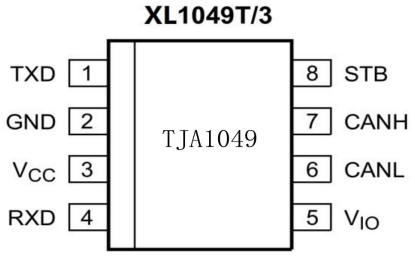


Figure 2. Pin configuration diagrams

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
V_{IO}	5	I/O supply voltage
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
STB	8	Standby mode control input

6. FUNCTIONAL DESCRIPTION

The TJA1049 is a HS-CAN stand-alone transceiver with Standby mode.
It combines the functionality
of the TJA1040 transceivers with improved EMC and ESD handling capability and quiescent curren tperformanceImproved slope control and high DC handling capability on the bus pins provide additional application flexibility.

6.1 Operating modes

The TJA1049 supports two operating modes, Normal and Standby, which are selectable via pin STB. See Table 3 for a description of the operating modes under normal supply conditions.

Table 3. Operating modes

Mode	Pin STB	Pin RXD	
		LOW	HIGH
Normal	LOW	bus dominant	bus recessive
Standby	HIGH	wake-up request detected	no wake-up request detected

6.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than tfltr(wake)bus are reflected on pin RXD, as shown in Figure 3.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by VIO, and is capable of detecting CAN bus activity even if VIO is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

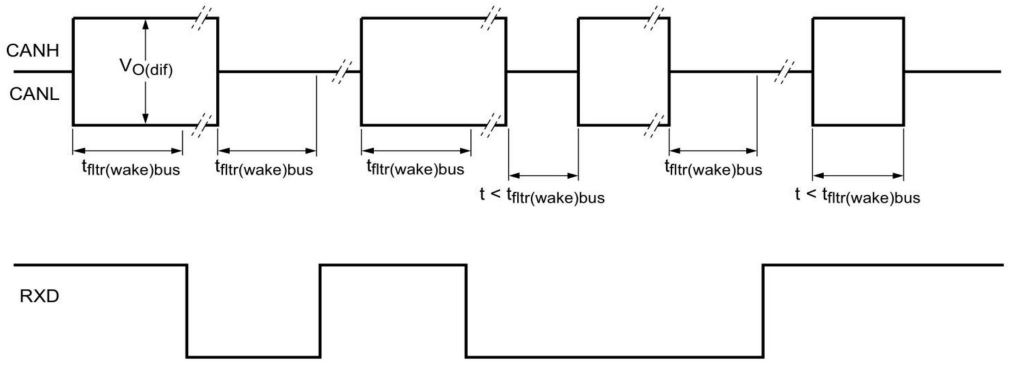


Figure 3. Wake-up timing

6.2 Fail-safe features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

6.2.2 Bus dominant time-out function

In Standby mode, a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than tto(dom)bus, the RXD pin is forced HIGH. This prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

6.2.3 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state in case one (or both) of these pins is left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

6.2.4 Undervoltage detection on pins VCC and VIO

Should VCC drop below the VCC undervoltage detection level, Vuvd(VCC), the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered.

Should VIO drop below the VIO undervoltage detection level, Vuvd(VIO), the transceiver will switch off and disengage from the bus (zero load) until VIO has recovered.

6.2.5 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), the output drivers will be disabled until the virtual junction temperature falls below Tj(sd) and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

6.3 VIO supply pin

Pin VIO on the TJA1049T-3-1Z-TDshould be connected to the microcontroller supply voltage (see Figure 6).This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller.Pin VIO also provides the internal supply voltage for the low-power differential receiver of thetransceiver. For applications running in low-power mode, this allows the bus lines to be monitoredfor activity even if there is no supply voltage on pin VCC.

7. LIMITING VALUES

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	on pins CANH, CANL and SPLIT	−58	+58	V
		on any other pin	−0.3	+7	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		−27	+27	V
V_{trt}	transient voltage	on pins CANH, CANL			
		pulse 1	−75	-	V
		pulse 2a	-	60	V
		pulse 3a	−100	-	V
		pulse 3b	-	75	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω)			
		at pins CANH and CANL	−8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ			
		at pins CANH and CANL	−8	+8	kV
		at any other pin	−4	+4	kV
		Machine Model (MM); 200 pF, 0.75 μH, 10 Ω			
		at any pin	−250	+250	V
		Charged Device Model (CDM); field Induced charge; 4 pF			
		at corner pins	−500	+500	V
		at any pin	−300	+300	V
T_{vj}	virtual junction temperature		−40	+125	°C
T_{stg}	storage temperature		−55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

[3] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

[4] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

8. THERMAL CHARACTERISTICS

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	150	K/W

9. STATIC CHARACTERISTICS

Table 6. Static characteristics

T_{vj} = −40 °C to +125 °C; V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.9 V to 5.25 V[1]; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground. Positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.75	-	5.25	V
I_{CC}	supply current	Standby mode				
		TJA1049T-3-1Z-TD	-	-	10	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$ [3]	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	20	45	65	mA
		dominant; V_{TXD} = 0 V; short circuit on bus lines; −3 V < (V_{CANH} = V_{CANL}) < +18 V	2.5	77.5	107.5	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.75	V
I/O level adapter supply; pin V_{IO} [1]						
V_{IO}	supply voltage on pin V_{IO}		2.9	-	5.25	V
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	5	-	20	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	15	80	200	µA
		dominant; V_{TXD} = 0 V	-	350	1000	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
Standby mode control input; pin STB						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3V_{IO}	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{IO}$	−1	-	+1	µA
I_{IL}	LOW-level input current	V_{STB} = 0 V	−15	-	−1	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	0.3V_{IO}	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3V_{IO}	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}$	−5	-	+5	µA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	−260	−150	−30	µA
C_i	input capacitance		-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ − 0.4 V	−9	−3	−1	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	10	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	−600	-	+600	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 45 Ω to 70 Ω	1.5	-	3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; no load				
		Normal mode: $V_{TXD} = V_{IO}$	−80	-	+80	mV
		Standby mode	−0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{IO}$; no load	2	$0.5V_{CC}$	3	V
		Standby mode; no load	−0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		Normal mode	0.5	-	0.9	V
		Standby mode	0.4	-	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		Normal mode	−4	-	0.5	V
		Standby mode	−4	-	0.4	V
$V_{dom(RX)}$	receiver dominant voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		Normal mode	0.9	-	9.0	V
		Standby mode	1.15	-	9.0	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V; Normal mode	100	-	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = −15 V to +40 V	−100	−70	−40	mA
		pin CANL; V_{CANL} = −15 V to +40 V	40	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; $V_{TXD} = V_{IO}$ $V_{CANH} = V_{CANL}$ = −27 V to +32 V	−5	-	+5	mA
I_L	leakage current	$V_{CC} = V_{IO}$ = 0 V or $V_{CC} = V_{IO}$ = shorted to GND via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	−3	-	+3	µA
R_i	input resistance	−2V ≤ V_{CANL} ≤ +7 V; −2V ≤ V_{CANH} ≤ +7 V	-	-	55	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔR_i	input resistance deviation	$0\ V \le V_{CANL} \le +5\ V$; $0\ V \le V_{CANH} \le +5\ V$	−5	-	+5	%
$R_{i(dif)}$	differential input resistance	$-2\ V \le V_{CANL} \le +7\ V$; $-2\ V \le V_{CANH} \le +7\ V$	18	49	60	kΩ
$C_{i(cm)}$	common-mode input capacitance		-	-	20	pF
$C_{i(dif)}$	differential input capacitance		-	-	10	pF
Common mode stabilization output, pin SPLIT; only relevant for TJA1049						
V_O	output voltage	Normal mode; $I_{SPLIT} = -500\ \mu A$ to $+500\ \mu A$	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal mode; $R_L = 1\ M\Omega$	$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
I_L	leakage current	Standby mode; $V_{SPLIT} = -58\ V$ to $+58\ V$	−5	-	+5	µA
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature		-	175	-	°C

[1] Only TJA1049T-3-1Z-TDhavepin V

[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] Maximum value assumes $V_{CC} < V_{IO}$; if $V_{CC} > V_{IO}$, the maximum value will be V_{CC} + 0.3 V.

[4] Not tested in production; guaranteed by design.

10. DYNAMIC CHARACTERISTICS

Table 7. Dynamic characteristics

T_{vj} = −40 °C to +125 °C; V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.9 V to 5.25 V[1]; R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD;						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	70	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	95	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	66	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	70	-	ns
$t_{d(TXDL-RXDL)}$	propagation delay from TXD to RXD	versions with V_{IO} pin Normal mode	60	-	300	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(TXDH-RXDH)}$	propagation delay from TXD to RXD	Normal mode	60	-	300	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	600	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	250	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	600	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	300	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	−65	-	+50	ns
		$t_{bit(TXD)}$ = 200 ns	−45	-	+25	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode	0.3	2	5	ms
$t_{to(dom)bus}$	bus dominant time-out time	Standby mode	0.3	2	5	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	Standby mode	0.5	1.5	5	µs
$t_{d(stb-norm)}$	standby to normal mode delay time		7	25	60	µs

[1] Only TJA1049T-3-1Z-TDhave pin V_{IO}

[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

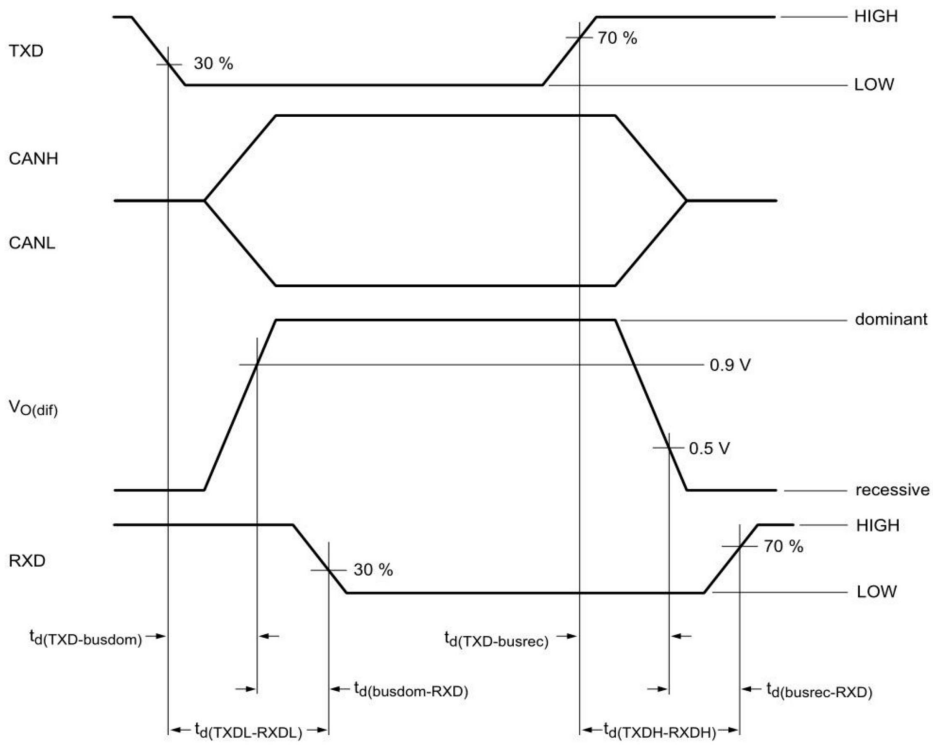


Figure 4. CAN transceiver timing diagram

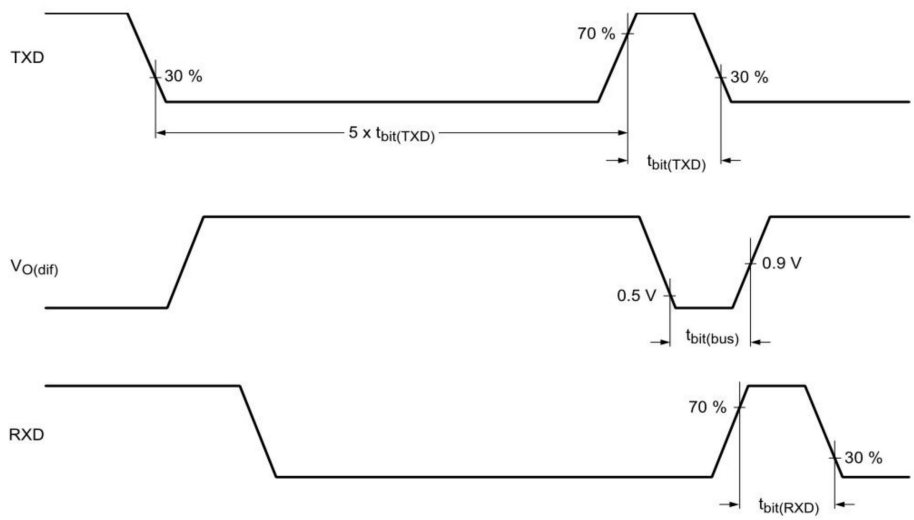
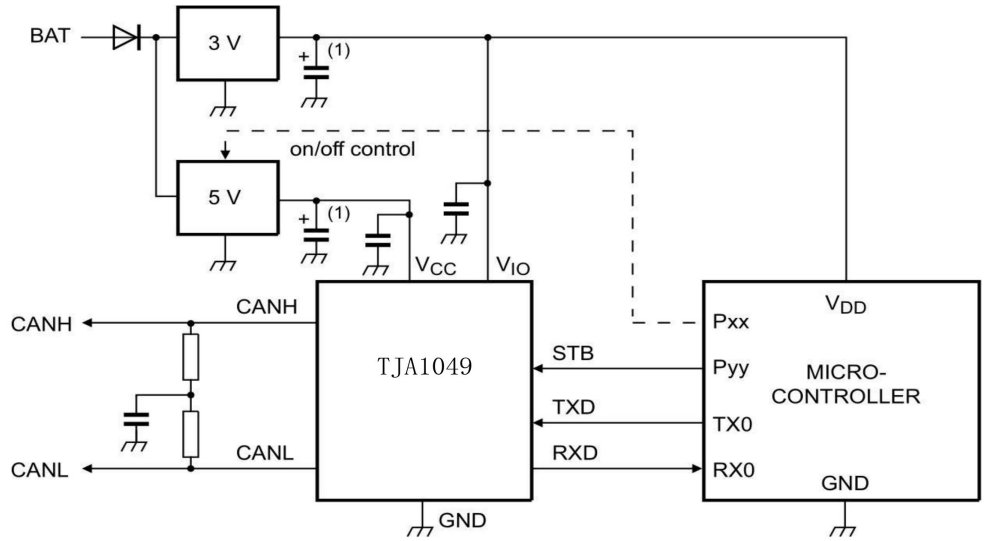


Figure 5. CAN FD timing definitions according to ISO 11898-2:2016

11. APPLICATION INFORMATION

11.1 Application diagrams



(1) Optional, depends on regulator.

Figure 6. Typical application with TJA1049T-3-1Z-TD**and a 3 V microcontroller.**

12. TEST INFORMATION

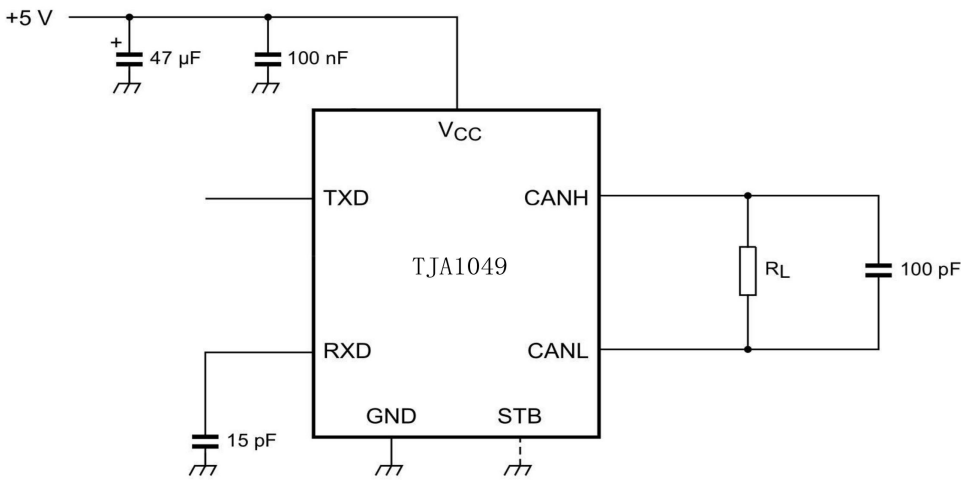


Figure 7.Timing test circuit for CAN transceiver

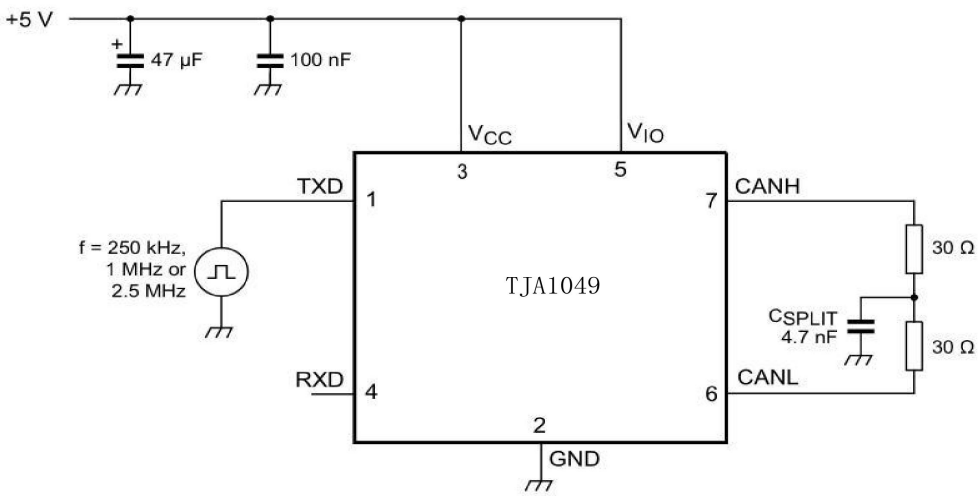


Figure 8. Test circuit for measuring transceiver driver symmetry

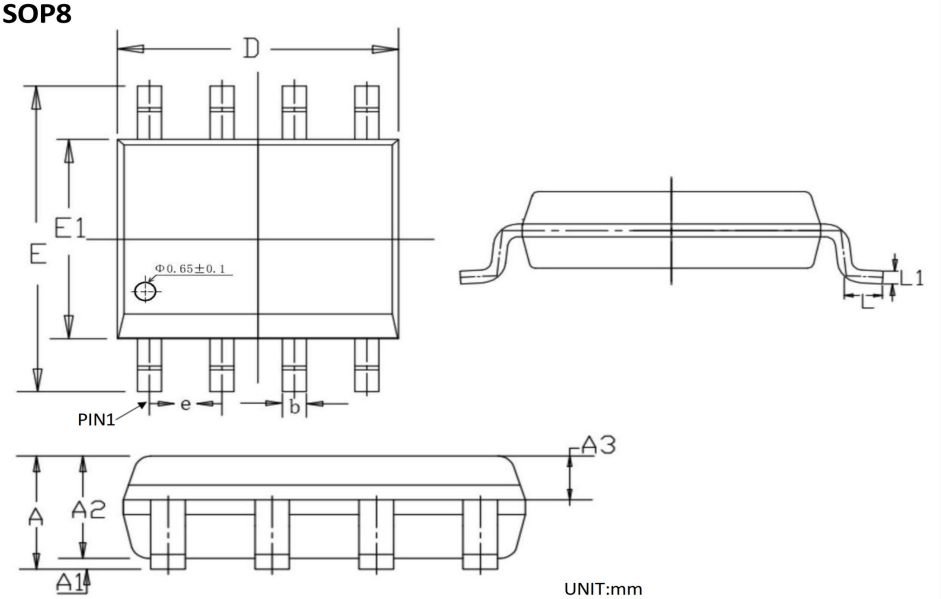
13. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
TJA1049T/3	TJA1049T3	SOP8	4.90 * 3.90	-40 to +125	MSL3	T&R	2500

14. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—