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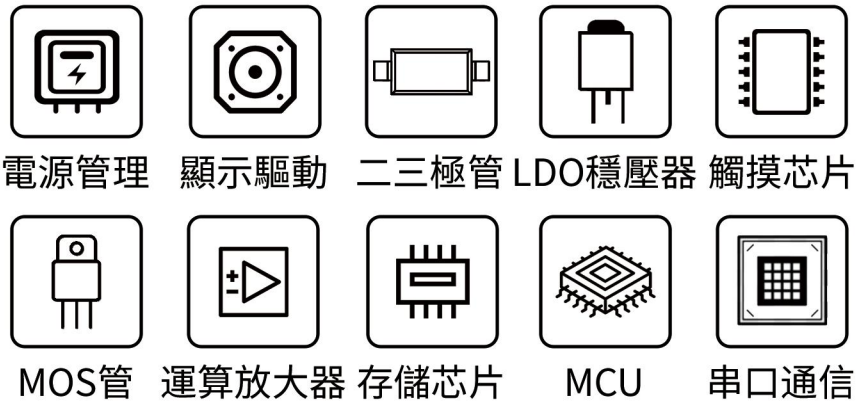


TJA1042T-3,118-TD

產品規格說明書

TJA1042T-3,118-
TDCAN transceiver with CAN FD and fail-safe features

1. DESCRIPTION

The TJA1042T-3,118-TD CAN transceiver complies with the ISO 11898-2 (2016) standard for the high- speed CAN (Controller Area Network) physical layer. The device is specifically designed for CAN FD networks capable of data rates up to 5 Mbps (Megabits per second). The TJA1042T-3,118-TD transceivers incorporate an auxiliary power input for I/O level adjustment, allowing for the setting of input pin thresholds and RXD output levels. It can be interfaced directly with microcontrollers with supply voltages from 2.7V to 5V.

The TJA1042T-3,118-TD boasts a standby mode for energy efficiency. Furthermore, it also offers a comprehensive range of protection features to enhance the durability of both the devices themselves and the network. These protection features contribute to the overall reliability and resilience of the CAN communication system.

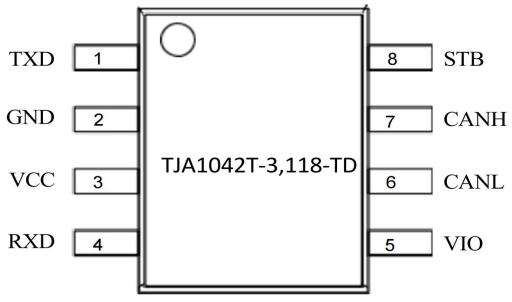
2. FEATURES

- Compliance with physical layer standards: ISO 11898-2(2016)
- In the CAN FD fast phase at data rates up to 5 Mbit/s.
- Supports SAE J2962-2 and IEC 62228-3 (up to 500kbps) without the need for common-mode chokes
- VCC operates on a single supply voltage range of +4.5V to +5.5V
- I/O voltage and VCC are separated, and VIO range is +2.7V to+ 5.0V
- Undervoltage protection on VCC and VIO power supplies
- Low power standby mode (10uA Typical) with host and bus wake-up capability
- Transmitter dominant timeout (TXD DTO) for data rates as low as 10kbps
- Support thermal shutdown protection (TSD) function
- Ideal passive behavior when unpowered: high-impedance state on bus and logic pins (no load), enabling seamless power-up/power-down operation on the bus and RXD output
- CANH/CANL HBM (Human Body Model) rating: ±8kV,CDM (Charged Device Model) ±2KV
- CAN Bus fault protection: ±58V
- Receiver Common-Mode input voltage range: ±30V
- Operating junction Temperature range: –40°C to 125°C
- Available in SOP8 package

3. APPLICATIONS

- High-Speed CAN BUS communication system
- Automotive, such as Two-wheeled vehicle
- Industrial automation
- Energy storage

4. PIN CONFIGURATIONS AND FUNCTIONS



(TOP VIEW)

Pin Functions			
NAME	**TYPE**	**DESCRIPTION**	
1	TXD	Digital Input	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Ground connection
3	VCC	Power	supply voltage for transceiver (+5.0V typical)
4	RXD	Digital Output	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Power	Transceiver I/O level shifting supply voltage (+2.7V to 5.5V)
6	CANL	Bus I/O	Low-level CAN bus input/output line
7	CANH	Bus I/O	High-level CAN bus input/output line
8	STB	Digital Input	Standby Mode control input (active high)

5. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VCC, VIO	-0.3	6	V	
Logic I/O Voltage	TXD, RXD, STB	-0.3	6	V	
Differential input voltage	V_{ID}	-30	30	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-58	+58	V	
Operating Temperature	Topr	-40	125	℃	
Junction Temperature	Tj	-40	150	℃	
Storage Temperature	Tstg	-65	150	℃	
IC Junction-to-Air Thermal Resistance	θ_{JA}	145 (TYP)		℃/W	Thermal parameters can not exceed Tj value
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	50 (TYP)		℃/W	
Junction-to-board thermal resistance	θ_{JB}	45 (TYP)		℃/W	
System level Electro-Static Discharge (IEC61000-4-2: Powered contact discharge)	ESD		±5	kV	CAN bus terminals to GND
Human Body Model (HBM) ESD stress voltage			±8	kV	All terminals
Charged Device Model (CDM)ESD stress voltage			±2	kV	All terminals

Note:

1、Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

2、 All voltage values, except differential I/O bus voltages, are with respect to ground terminal

6. Recommended Operating Conditions

Parameters	*Symbol*	*min*	*max*	*unit*
Power Supply Voltage	VCC	4.5	5.5	V
	VIO	2.7	5.5	V
Differential input voltage	V_{ID}	-3	8	V
CAN bus terminal HIGH level output current	$I_{OH(CAN)}$	-50		mA
CAN bus terminal LOW level output current	$I_{OL(CAN)}$		50	mA
RXD terminal HIGH level output current	$I_{OH(RXD)}$	-2		mA
RXD terminal LOW level output current	$I_{OL(RXD)}$		2	mA

7. Specifications

7-1. Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=2.7V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V,Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Voltage	V_{CC}	4.5		5.5	V	
undervoltage detection voltage on pin VCC	$V_{uvd(VCC)}$	3.5		4.5	V	
supply voltage on pin VIO	V_{IO}	2.7		5.5	V	
undervoltage detection voltage on pin VIO	$V_{uvd(VIO)}$	1.5		2.7	V	
supply current	I_{CC}		45	70	mA	Normal mode, dominant, TXD=0, STB=0, R_L=60Ω
			1.3	5	mA	Normal mode, recessive, TXD=V_{IO}, STB=0
			0.4	5	uA	Standby mode, STB=V_{IO}, TXD=V_{IO}
supply current on pin VIO	I_{IO}			900	uA	Normal mode, dominant, V_{TXD}=0V
				100	uA	Normal mode, recessive, V_{TXD}=V_{IO}
			10	20	uA	Standby mode; VTXD=V_{IO}
Thermal-Shutdown Threshold	T_{TS}	155	165	180	℃	
Logic Side						
High level input voltage	V_{IH}	0.7*V_{IO}			V	TXD &STB pin
Low level input voltage	V_{IL}			0.3*V_{IO}	V	TXD &STB pin
High level input current	I_{IH}	-5		5	uA	TXD &STB pin
Low level input current	I_{IL}	-200		-30	uA	TXD pin
		-15		-1	uA	STB pin
Output High Voltage	V_{OH}	0.8*V_{IO}			V	RXD, IO=-2mA
Output Low Voltage	V_{OL}			0.2*V_{IO}	V	RXD, IO=2mA
Input Capacitance	C_{IN}		5		pF	TXD pin
Driver Unit						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4.5	V	STB=0, TXD=0V, R_{Load} =60Ω

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5	1.33	2.25	V	STB=0, TXD=0V, R_{Load} =60Ω
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	0.5*VCC	3	V	TXD=V_{IO}; recessive; no load
		-0.1		0.1	V	Standby mode, no load
Differential output voltage (Dominant)	$V_{OD(D)}$	1.5		3	V	VCC=5V, TXD=0, R_{Load} =60Ω see Figure 7.1
Differential output voltage (Recessive)	$V_{OD(R)}$	-0.05		0.05	V	VCC=5V, TXD=VIO, R_{Load} =60Ω see Figure 7.1
		-0.1		0.1	V	VCC=5V, TXD=V_{IO}, no Load see Figure 7.1
Short- circuit output current	I_{OS}	-110	-45		mA	Dominant, CANH=-30V, CANL open see Figure 7.9
			3	6	mA	Recessive, CANH=30V, CANL open see Figure 7.9
		-6	-3		mA	Recessive, CANL=-30V, CANH open see Figure 7.9
			45	110	mA	Dominant, CANL=30V, CANH open see Figure 7.9
Receiver Unit						
Positive-going bus input threshold voltage	V_{IT+}		750	900	mV	$V_{COM(CAN)}$=0V
Negative-going bus input threshold voltage	V_{IT-}	500	650		mV	$V_{COM(CAN)}$=0V
Hysteresis voltage	V_{HYS}		100		mV	
Power-off (unpowered) bus input leakage current	$I_{OFF(LKG)}$	-3		3	uA	V_{CANH} or V_{CANL} = 5 V, VCC = 0V, VIO= 0 V
Input capacitance to ground	C_I		13		pF	CANH or CANL
Differential input	C_{ID}		5		pF	
Differential input resistance	R_{ID}	30	48	80	kΩ	
Input resistance	R_{IN}	15	24	40	kΩ	
Input resistance matching	R_{Imatch}	-5		+5	%	CANH=CANL
Common-mode voltage range	V_{COM}	-30		+30	V	

7-2. Switching Electrical Characteristics

(V_{CC}=4.5V~5.5V,V_{IO}=2.7V~5.5V, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at VCC=5V, VIO=3.3V,Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Loop delay1	T_{loop1}		90	220	ns	Driver input to receiver output, Recessive to Dominant, see Figure 7.7
Loop delay2	T_{loop2}		100	220	ns	Driver input to receiver output, Dominant to Recessive, see Figure 7.7
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)}$ = 500 ns
		155		210	ns	$t_{bit(TXD)}$ = 200 ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)}$ = 500 ns
		120		220	ns	$t_{bit(TXD)}$ = 200 ns
Driver Unit						
Propagation delay time from TXD to bus dominant	t_{PLH}		90		ns	Normal mode, see Figure 7.4
Propagation delay time from TXD to bus recessive	t_{PHL}		65		ns	Normal mode, see Figure 7.4
Differential output signal rise time	t_r		20		ns	see Figure 7.4
Differential output signal fall time	t_f		42		ns	see Figure 7.4
Bus dominant time-out time	t_{TXD_DTO}	0.5	2.2	5.0	ms	see Figure 7.8
Receiver Unit						
Propagation delay time from bus dominant to RXD	t_{PLH}		21		ns	see Figure 7.6
Propagation delay time from bus recessive to RXD	t_{PHL}		27		ns	see Figure 7.6
RXD signal rise time	t_r		10		ns	see Figure 7.6
RXD signal fall time	t_f		10		ns	see Figure 7.6
Receiver dominant time out	t_{RXD_DTO}	0.5	2.2	5.0	ms	Standby mode
bus wake-up filter time	$t_{fltr(wake)bus}$	0.5		10	us	Standby mode
standby to normal mode delay time	$t_{d(stb-norm)}$	7		60	us	standby to normal mode delay time

7-3. Parameter Measurement Information

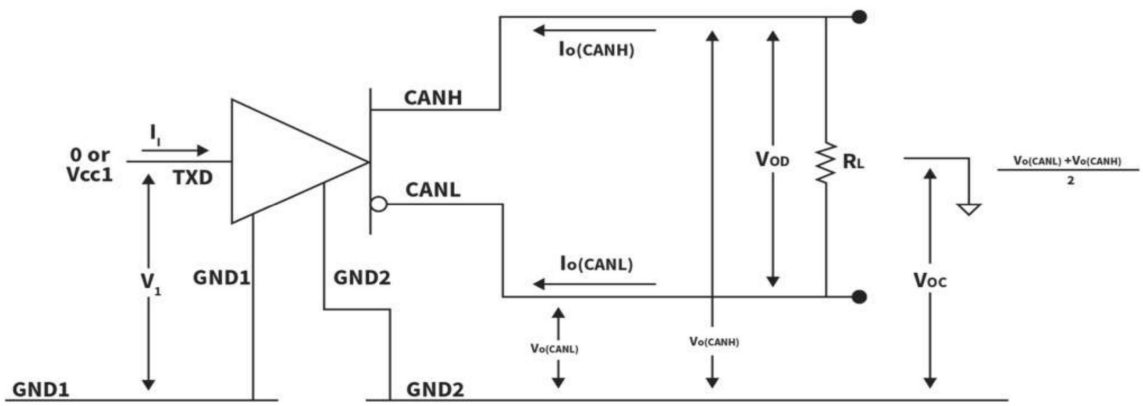


Figure 7.1. Driver Voltage, Current and Test Definitions

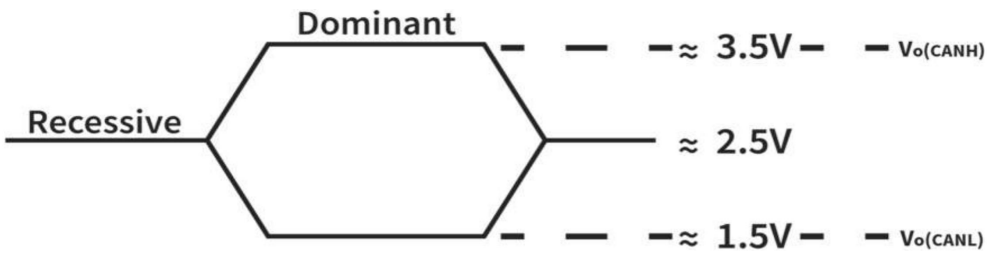


Figure 7.2. Bus Logic State Voltage Definitions

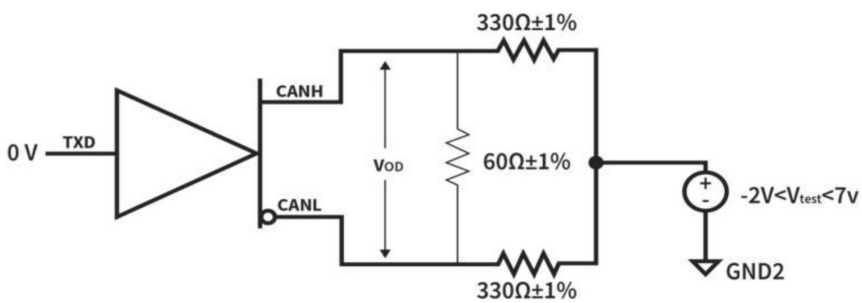
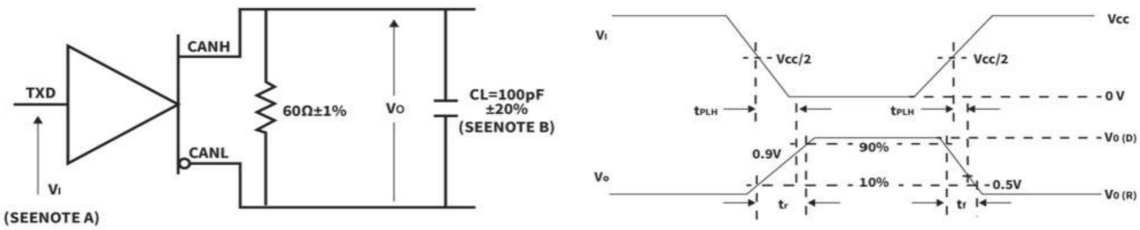


Figure 7.3. Driver V_{OD} With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 7.4. Driver Test Circuit and Voltage Waveforms

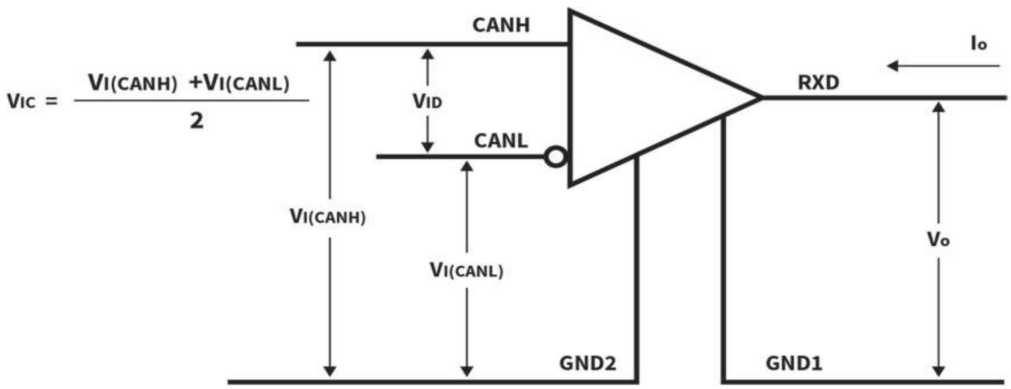
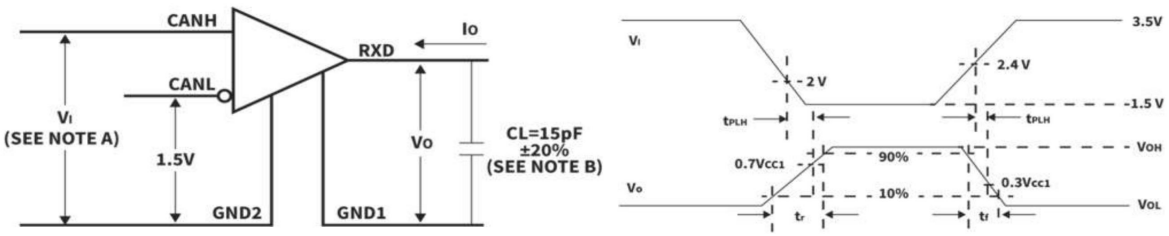


Figure 7.5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7.6. Receiver Test Circuit and Voltage Waveforms

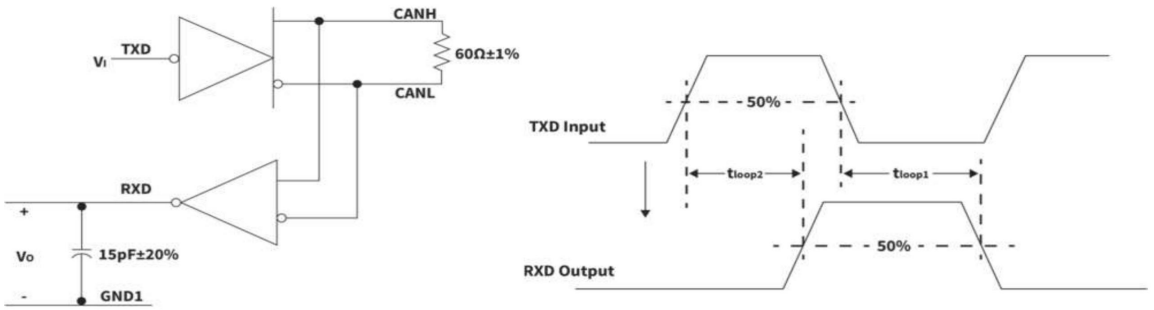
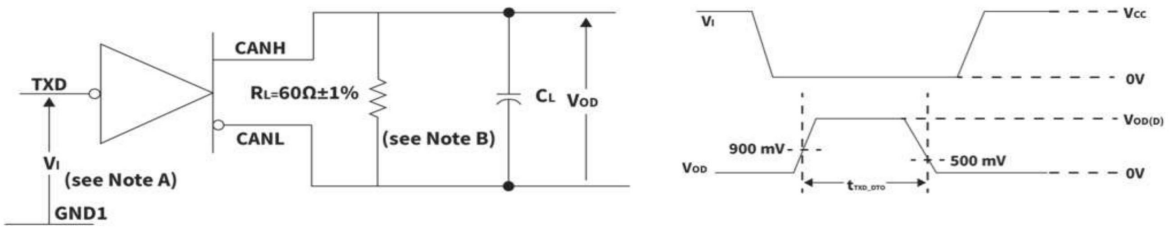


Figure 7.7. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics:

PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7.8. Dominant Time-out Test Circuit and Voltage Waveforms

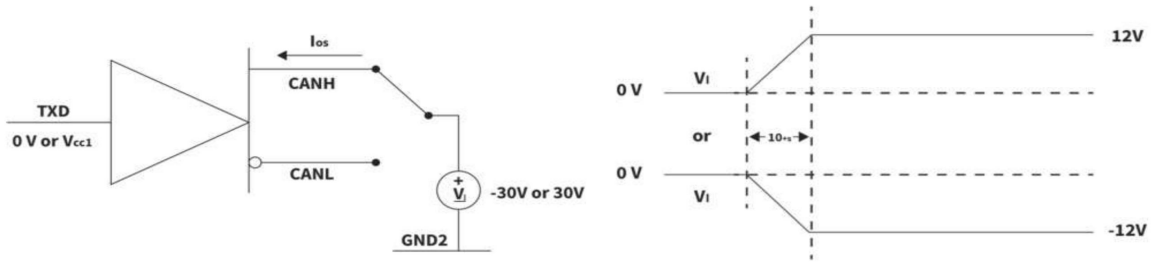


Figure 7.9. Driver Short-Circuit Current Test Circuit and Waveforms

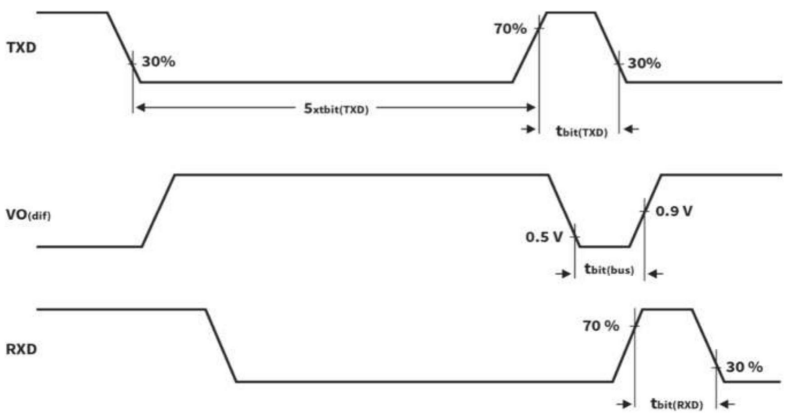


Figure 7.10. $t_{bit(RXD)}$ Test Circuit and Waveforms

8. FUNCTIONAL DESCRIPTION

Equivalent block diagram inside the TJA1042T-3,118-TD is shown as following figure 8. The TJA1042T-3, 118-TD is a high speed CAN transceiver with standby mode, designed for all types of high speed CAN networks in nodes that require a low-power mode. It provides an interface between a Controller Area Network (CAN) protocol
controller and the physical two-wire CAN bus. It fully compatibles with the ISO11898-2(2016) standard, and enable reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The TJA1042T-3,118-TD provides thermal protection and transmit data dominant time out function. In addition, it has a VIO pin, which can be interfaced directly with microcontrollers with supply voltages from 2 .7 V to 5 V.

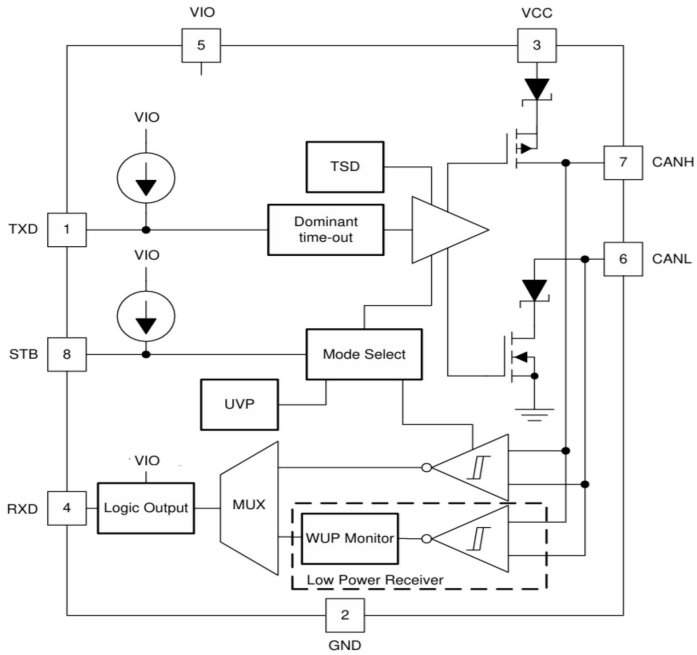


Figure 8. Equivalent block diagram

8-1. Operating modes

The TJA1042T-3,118-TDsupports two operating modes: Normal and Standby, which are selected via pin STB. See Table 4 for a description of the operating modes under normal supply conditions.

MODE	STB Pin Level	RXD Pin Level	
		LOW	HIGH
Normal Mode	LOW	bus dominant	bus recessive
STB Mode	HIGH	wake-up request detected	no wake-up request detected

Table 4. Operating modes

8-1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 8 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

8-1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than tfltr(wake)bus are reflected on pin RXD. In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by VIO, and is capable of detecting CAN bus activity even if VIO is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

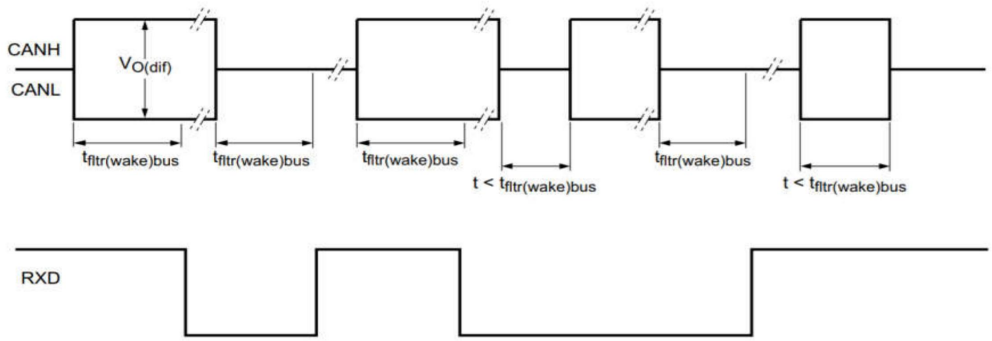


Figure 9. Wake-up timing

8-2. Fail-safe features

8-2.1 TXD dominant time-out function

A ‘TXD dominant time-out’ timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

8-2.2 Bus dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than tto(dom)bus, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

8-2.3 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

8-2.4 Undervoltage detection on pins VCC and VIO

Should VCC drop below the VCC undervoltage detection level, Vuvd(VCC), the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered. Should VIO drop below the VIO undervoltage detection level, Vuvd(VIO), the transceiver will switch off and disengage from the bus (zero load) until VIO has recovered.

8-2.5 Over Temperature Protection

The TJA1042T-3,118-TDfeatures a thermal shutdown temperature (TSD) function. If the virtual junction temperature exceeds the shutdown junction temperature TTS, the output drivers will be disabled until the virtual junction temperature becomes lower than TTS and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

8-3. VIO supply pin

Pin VIO on the TJA1042T-3,118-TDshould be connected to the microcontroller supply voltage (see Figure 8). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin VIO also
provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

9. APPLICATION CIRCUIT EXAMPLE

As shown in the figure below (Figure 9), U1 and U2 form a minimal application system for a CAN-BUS bus. In this circuit, U1 (2515) is an independent CAN bus controller with SPI interface, while U2 (TJA1042T-3,118-TD) is a CAN-BUS interface transceiver chip. Any MCU (DSP or FPGA) with a SPI interface can connected to P1 will be able to transmit and receive CAN-BUS bus frame data. The normal operating voltage range of MCU-VDD is

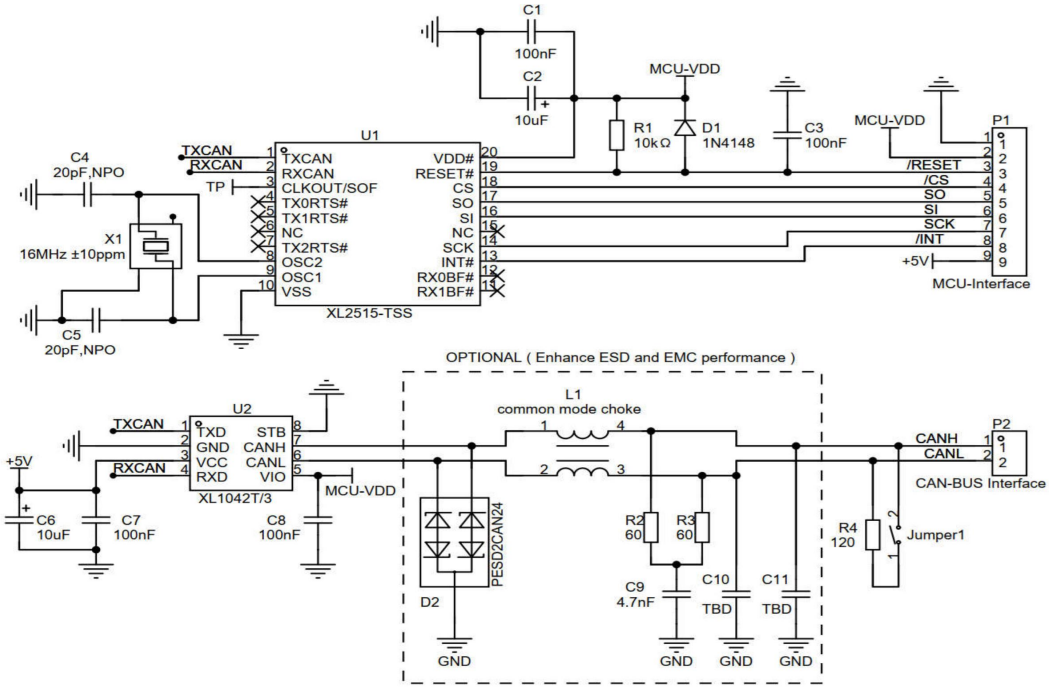


Figure 9. CAN-BUS application circuit example

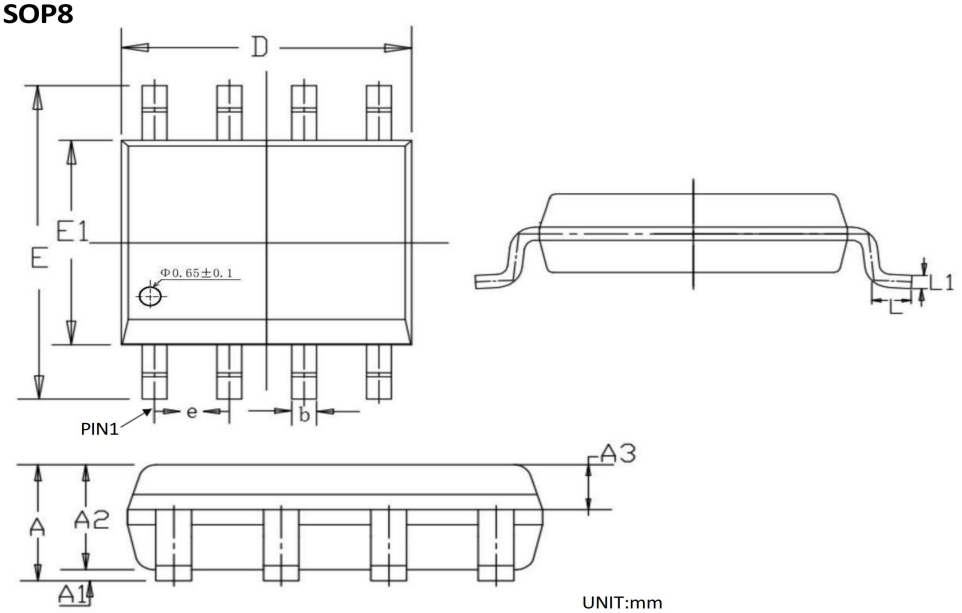
10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
TJA1042T-3,118-TD	1042T3	SOP8	4.90 * 3.90	-40 to +125	MSL3	T&R	2500

11. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—