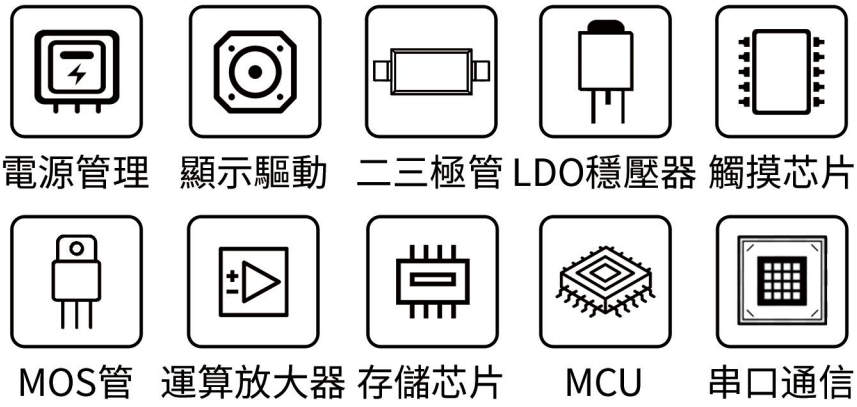
TDSEMIC
拓電半導體

自主封測 品質把控 售後保障

WEB | WWW.TDSEMIC.COM




# PCA82C250T-YM-TD

產品規格說明書

# PCA82C250T/YM-TD

**CAN controller interface chip**

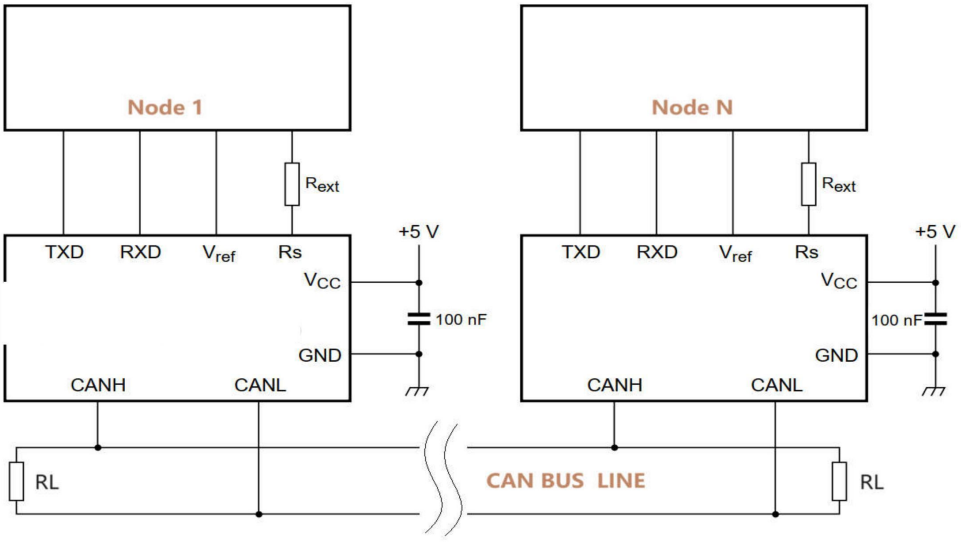
## 1. DESCRIPTION

The PCA82C250 and PCA82C250 are CAN controller interface chips. As a CAN transceiver, The devices provide transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

## 2. FEATURES

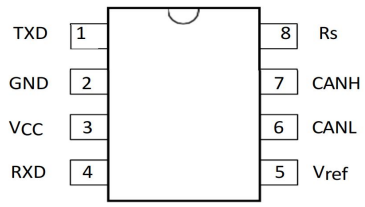
- Fully compatible with the “ISO 11898” standard
- Slope control to reduce Radio Frequency Interference (RFI)
- Short-circuit proof to battery and ground in 12 V powered systems
- Low-current Standby mode
- An unpowered node does not disturb the bus lines
- CAN bus communication speed up to 1 Mbps
- High immunity against electromagnetic interference
- Thermally protected
- Package option: PCA82C250 (SOP8), PCA82C250 (DIP8)

## 3. TYPICAL APPLICATION



## 4. PIN CONFIGURATIONS AND FUNCTIONS

**PCA82C250 PCA82C250**




**(TOP VIEW)**

**Pin Functions**

| Symbol | Pin | Description |
|---|---|---|
| TXD | 1 | transmit data input |
| GND | 2 | ground |
| $V_{CC}$ | 3 | supply voltage |
| RXD | 4 | receive data output |
| $V_{ref}$ | 5 | reference voltage output |
| CANL | 6 | LOW-level CAN voltage input/output |
| CANH | 7 | HIGH-level CAN voltage input/output |
| Rs | 8 | slope resistor input |

### 4.1. Functional description

The PCA82C250 and PCA82C250 are the interface between a CAN protocol controller and the physical bus. It is primarily intended for applications up to 1 MBd in trucks and buses. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible with the “ISO 11898” standard.

A current-limiting circuit protects the transmitter output stage against short-circuits to positive and negative battery voltage. Although power dissipation will increase as a result of a short circuit fault condition, this feature will prevent destruction of the transmitter output stage.

If the junction temperature exceeds approximately 150 °C, the limiting current of both transmitter outputs is decreased. Because the transmitter is responsible for most of the power dissipated, this will result in reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operational. The thermal protection is needed, in particular, when a bus line is short-circuited.

The CANH and CANL lines are also protected against electrical transients which may occur in an automotive environment.

Pin 8 (Rs) allows three different modes of operation to be selected: High-speed, Slope control and Standby.

For high-speed operation, the transmitter output transistors are simply switched on and off as fast as possible. In this mode, no measures are taken to limit the rise and fall slopes. A shielded cable is recommended to avoid RFI problems. High-speed mode is selected by connecting pin 8 to ground.

Slope control mode allows the use of an unshielded twisted pair or a parallel pair of wires as bus lines. To reduce RFI, the rise and fall slopes should be limited. The rise and fall slopes can be programmed with a resistor connected from pin 8 to ground. The slope is proportional to the current output at pin 8.

If a HIGH level is applied to pin 8, the circuit enters a low-current Standby mode. In this mode, the transmitter is switched off and the receiver is switched to a low current. If dominant bits are detected (differential bus voltage >0.9 V), RXD will be switched to a LOW level. The microcontroller should react to this condition by switching the transceiver back to normal operation (via pin 8). Because the receiver is slower in Standby mode, the first message will be lost at higher bit rates.

**Table 4-1. Truth table of the CAN transceiver**

| Supply | TXD | CANH | CANL | Bus state | RXD |
|---|---|---|---|---|---|
| 4.5 V to 5.5 V | 0 | HIGH | LOW | dominant | 0 |
| 4.5 V to 5.5 V | 1 (or floating) | floating | floating | recessive | 1 |
| <2V (not powered) | X[1] | floating | floating | recessive | X[1] |
| 2 V < Vcc < 4.5 V | >0.75 $V_{CC}$ | floating | floating | recessive | X[1] |
| 2 V < Vcc < 4.5 V | X[1] | floating<br>if $V_{Rs} > 0.75V_{CC}$ | Floating<br>If $V_{Rs} > 0.75V_{CC}$ | recessive | X[1] |

[1] X = don't care.

**Table 4-2. Pin Rs summary**

| Condition forced at pin Rs | Mode | Resulting voltage or current at pin Rs |
|---|---|---|
| $V_{Rs} > 0.75V_{CC}$ | Standby | $I_{Rs} < \lvert 10\ \mu A \rvert$ |
| -10 µA< $I_{Rs}$ < -200 µA | Slope control | $0.4V_{CC} < V_{Rs} < 0.6V_{CC}$ |
| $V_{Rs} < 0.3V_{CC}$ | High-speed | $I_{Rs}$ < -500 µA |

## 5. BLOCK DIAGRAM

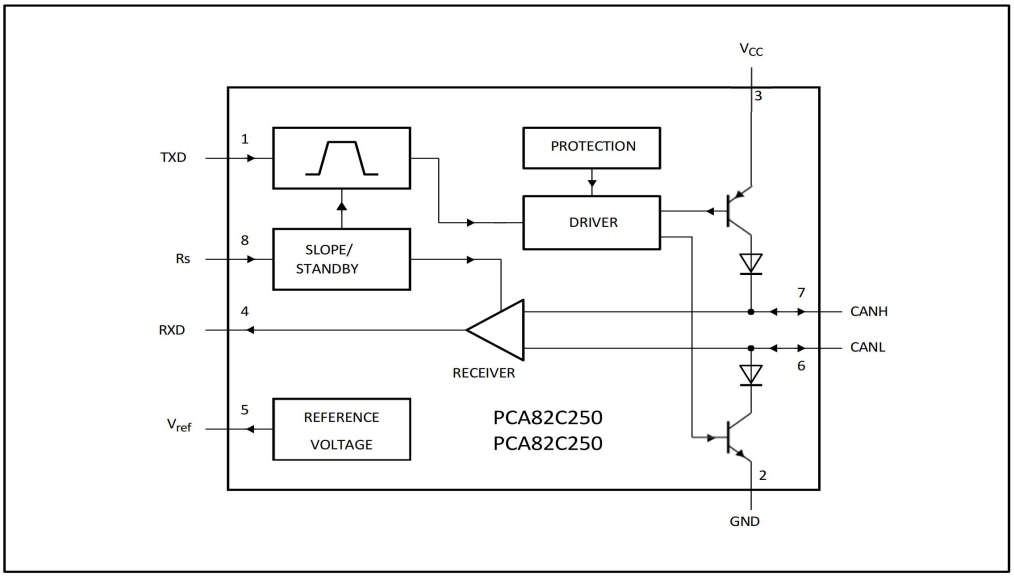



**Fig 5-1. Block Diagram**

# 6. SPECIFICATIONS

## 6.1 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin 2（GND）; positive input current.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| VCC | supply voltage | | - 0.3 | +7.0 | V |
| Vn | DC voltage at pins 1, 4, 5 and 8 | | - 0.3 | $V_{CC}$ + 0.3 | V |
| V6,7 | DC voltage at pin 6 and 7 | 0 V < $V_{CC}$ < 5.5 V; no time limit | -8 | +18 | V |
| Vtrt | transient voltage at pins 6 and 7 | see Figure 6-6 | - 150 | +100 | V |
| Tstg | storage temperature | | - 50 | +150 | ℃ |
| Tamb | ambient temperature | | - 40 | +85 | ℃ |
| Tvj | virtual junction temperature | [2] | - 40 | +150 | ℃ |
| VESD | electrostatic discharge voltage | [3] | - 2000 | +2000 | V |
| | | [4] | - 150 | +150 | V |

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] An alternative definition of virtual junction temperature is: Tvj = Tamb + Pd × Rth(vj-a), where Rth(j-a) is a fixed value to be used for the calculation of Tvj. The rating for Tvj limits the allowable combinations of power dissipation (Pd) and ambient temperature (Tamb).

[3] Classification A: human body model; C = 100 pF; R = 1500 Ω; V = ±2000 V.

[4] Classification B: machine model; C = 200 pF; R = 25 Ω; V = ±150 V.

## 6.2 Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| VCC | supply voltage | | 4.5 | 5.5 | V |
| ICC | supply current | Standby mode | - | 210 | μA |
| 1/tbit | maximum transmission speed | non-return-to-zero | - | 1 | MBd |
| VCAN | CANH, CANL input/output voltage | | -8 | +18 | V |
| Vdiff | differential bus voltage | | 1.5 | 3.0 | V |
| tPD | propagation delay | High-speed mode | - | 60 | ns |
| Tamb | ambient temperature | | -40 | +85 | °C |

## 6.3 Thermal Data

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| Rth(j-a) | thermal resistance from junction to ambient | in free air | 165 | K/W |

## 6.4 Characteristics

VCC = 4.5 V to 5.5 V; Tamb = -40° C to +85° C; RL = 60 Ω; I8 > -10 µA; unless otherwise specified; all voltages referenced to ground (pin 2); positive input current; all parameters are guaranteed over the ambient temperature range by design, but only 100 % tested at +25 ° C.

| Sym. | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply consumption** | | | | | | |
| I3 | Supply current | Dominant; $V_1$ = 1 V | - | - | 75 | mA |
| | | Recessive; $V_1$ = 4 V; $R_8$ = 47 kΩ | - | - | 18 | mA |
| | | Recessive; $V_1$ = 4 V; $V_8$ = 1V | - | - | 22 | mA |
| | | Standby; Tamb < 80° C [1] | - | 168 | 210 | µA |
| **DC bus transmitter** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | output recessive | 0.7$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | output dominant | -0.3 | - | 0.3$V_{CC}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_1$ = 4 V | -220 | - | +40 | µA |
| $I_{IL}$ | LOW-level input current | $V_1$ = 1 V | -110 | - | -650 | µA |
| $V_{6,7}$ | recessive bus voltage | $V_1$ = 4 V; no load | 2.0 | - | 3.0 | V |
| $I_{LO}$ | off-state output leakage current | 2 V < ($V_6$, $V_7$) < 7 V | -2 | - | +1 | mA |
| | | 5 V < ($V_6$, $V_7$) < 18V | -5 | - | +12 | mA |
| $V_7$ | CANH output voltage | $V_1$ = 1 V | 2.75 | - | 4.5 | V |
| $V_6$ | CANL output voltage | $V_1$ = 1 V | 0.5 | -- | 2.25 | V |
| △$V_{6,7}$ | difference between output voltage at pins 6 and 7 | $V_1$ = 1 V | 1.5 | - | 3.0 | V |
| | | $V_1$ = 1 V; $R_L$ = 45Ω; $V_{CC}$ ⩾ 4.9V | 1.5 | - | - | V |
| | | $V_1$ = 4 V; no load | -500 | - | +50 | mV |
| $I_{sc7}$ | short-circuit CANH current | $V_7$ = -5 V ; $V_{CC}$ ⩽ 5V | - | - | -120 | mA |
| | | $V_7$ = -5 V ; $V_{CC}$ = 5.5V | - | - | -130 | mA |
| $I_{sc6}$ | short-circuit CANL current | $V_6$ = 18 V | - | - | 170 | mA |
| **DC bus receiver: V1 = 4 V; pins 6 and 7 externally driven; - 2V< (V6, V7) < 7 V; unless otherwise specified** | | | | | | |
| $V_{diff(r)}$ | differential input voltage (recessive) | | -1.0 | - | +0.5 | V |
| | | 7 V < ($V_6$, $V_7$) <12 V, non-Standy mode | -1.0 | - | +0.4 | V |
| $V_{diff(d)}$ | differential input voltage (dominant) | | 0.9 | - | 5.0 | V |
| | | 7 V < ($V_6$, $V_7$) <12 V, non-Standy mode | 1.0 | - | 5.0 | V |
| Vdiff (hys) | differential input hysteresis | see Figure 6-3 | - | 160 | - | mV |
| VOH | HIGH-level output voltage | pin 4; I4 = -100 µA | 0.8VCC | - | VCC | V |
| VOL | LOW-level output voltage | pin 4; I4 = 1 mA | 0 | - | 0.2VCC | V |
| | | I4 = 10 mA | 0 | - | 1.5 | V |
| Ri | input resistance | CANH, CANL | 4.7 | - | 30 | kΩ |
| Rdiff | differential input resistance | | 19.2 | - | 120 | kΩ |
| Ci | input capacitance | CANH, CANL | - | - | 20 | pF |
| Cdiff | differential input capacitance | | - | - | 10 | pF |
| **Reference output** | | | | | | |
| Vref | reference output voltage | $V_8$ = 1 V; \|I5\| < 50 µA | 0.45VCC | - | 0.55VCC | V |
| | | $V_8$ = 4 V; \|I5\| <5 µA | 0.4VCC | - | 0.6VCC | V |
| **Timing (CL = 100 pF; see Figure 6-1, Figure 6-2, Figure 6-4 and Figure 6-5)** | | | | | | |
| tbit | minimum bit time | Rs = 0 Ω | - | - | 1 | µs |
| tonTXD | delay TXD to bus active | Rs = 0 Ω | - | - | 60 | ns |

**[1] I1 = I4 = I5 = 0 mA; 0 V < V6 < VCC; 0 V < V7 < VCC; V8 = VCC**

## 6.4 Characteristics (continued)

| Sym. | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Timing (CL = 100 pF; see Figure 6-1, Figure 6-2, Figure 6-4 and Figure 6-5)** | | | | | | |
| toffTXD | delay TXD to bus inactive | Rs = 0 Ω | - | 45 | 90 | ns |
| tonRXD | delay TXD to receiver active | Rs = 0 Ω | - | 65 | 130 | ns |
| toffRXD | delay TXD to receiver inactive | Rs = 0 Ω; VCC < 5.1V ; Tamb < 85 °C | - | 90 | 160 | ns |
| | | Rs = 0 Ω; VCC < 5.5V ; Tamb < 85 °C | - | 105 | 180 | ns |
| tonRXD | delay TXD to receiver active | Rs = 47 kΩ | - | 400 | 550 | ns |
| | | Rs = 24 kΩ | - | 280 | 350 | ns |
| toffRXD | delay TXD to receiver inactive | Rs = 47 kΩ | - | 280 | 500 | ns |
| | | Rs = 24 kΩ | - | 230 | 350 | ns |
| \|SR\| | differential output voltage slew rate | Rs = 47 kΩ | - | 16 | - | V/us |
| tWAKE | wake-up time from Standby | via pin 8 | - | - | 25 | us |
| tdRXDL | bus dominant to RXD LOW | $V_8$ = 4 V; Standby mode | - | - | 10 | us |
| **Standby/Slope Control (pin 8)** | | | | | | |
| $V_8$ | input voltage for high-speed | | - | - | 0.3VCC | V |
| $I_8$ | input current for high-speed | $V_8$ = 0V | - | - | -500 | uA |
| Vstb | input voltage for Standby mode | | 0.75VCC | - | - | V |
| Islope | slope control mode current | | -10 | - | -200 | uA |
| Vslope | slope control mode voltage | | 0.4VCC | - | 0.6VCC | V |

[1] I1 = I4 = I5 = 0 mA; 0 V < V6 < VCC; 0 V < V7 < VCC; V8 = VCC;
[2] This is valid for the receiver in all modes: High-speed, Slope control and Standby.

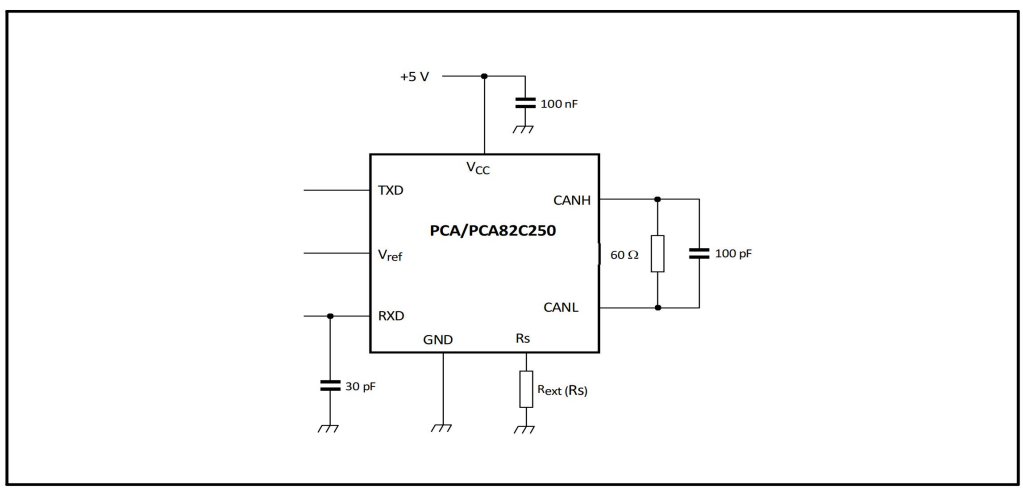



**Figure 6-1 : Test circuit for dynamic characteristics**

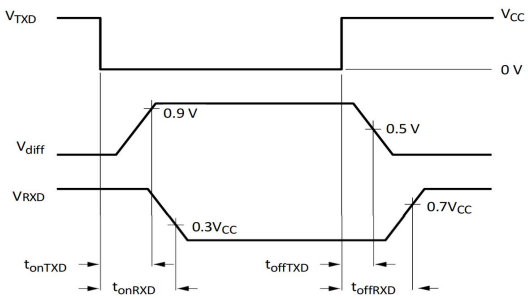



**Figure 6-2 : Switching Times Test Circuits.**

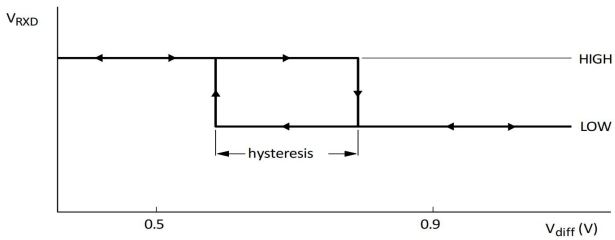



**Figure 6-3. Sink Current Delay Times vs. Input 0 V Enable Switching**

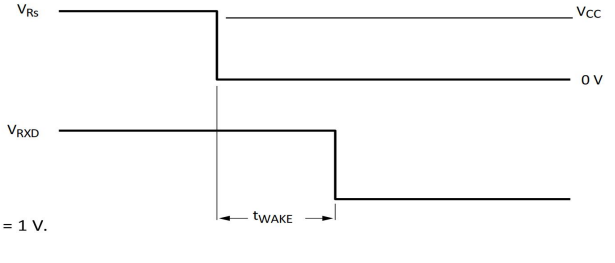



**Figure 6-4. Bidirectional DC Motor Control**

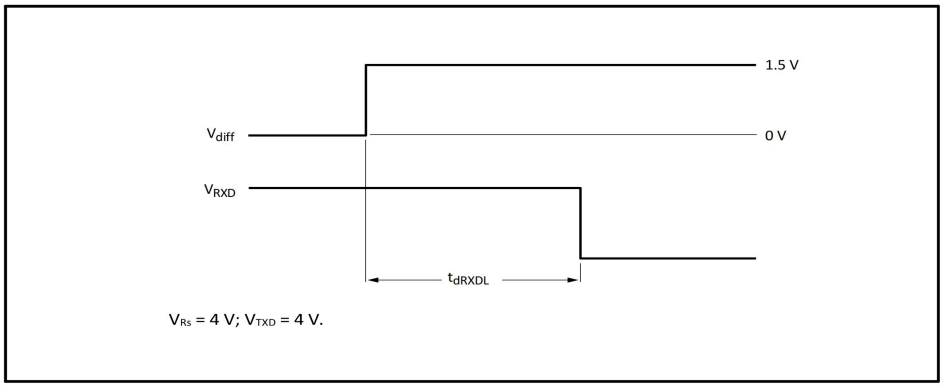



**Figure 6-5. Timing diagram for bus dominant to RXD LOW**

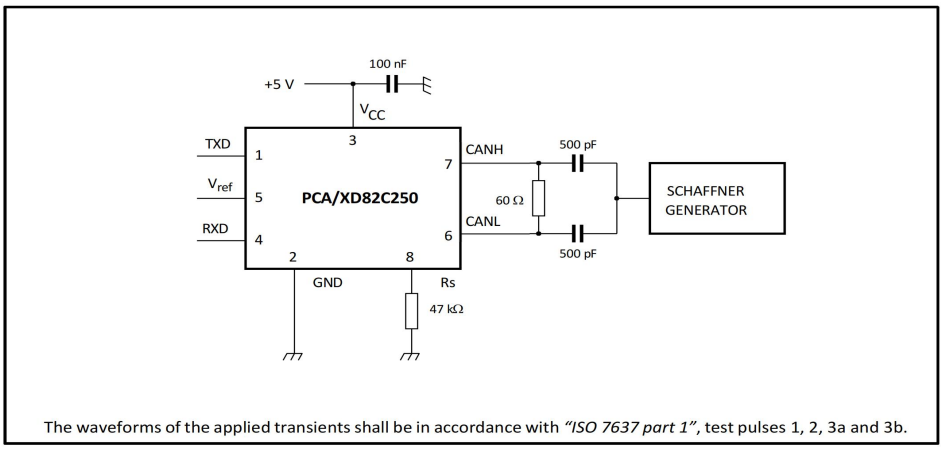



**Figure 6-6. Test circuit for transients**

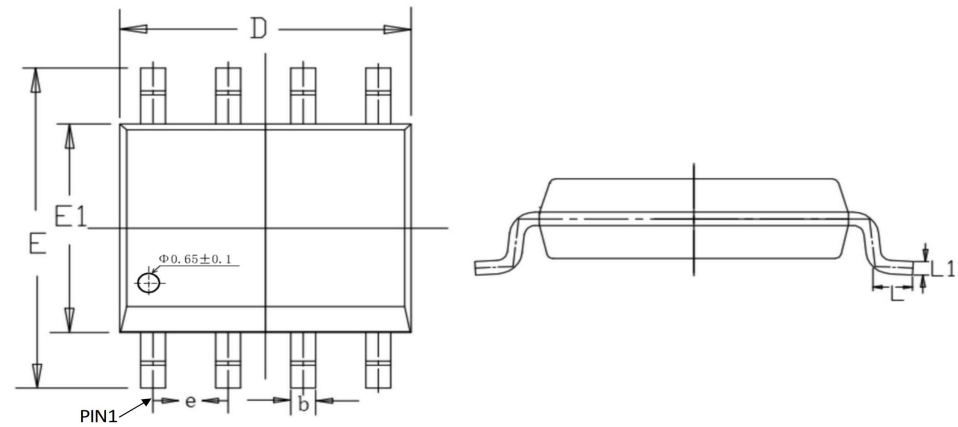
## 7. ORDERING INFORMATION

**Ordering Information**

| Part Number | Device Marking | Package Type | Body size (mm) | Temperature (°C) | MSL | Transport Media | Package Quantity |
|---|---|---|---|---|---|---|---|
| PCA82C250 | PCA82C250 | SOP8 | 4.90 * 3.90 | - 40 to 85 | MSL3 | T&R | 2500 |
| | | | | | | | |

## 8. DIMENSIONAL DRAWINGS

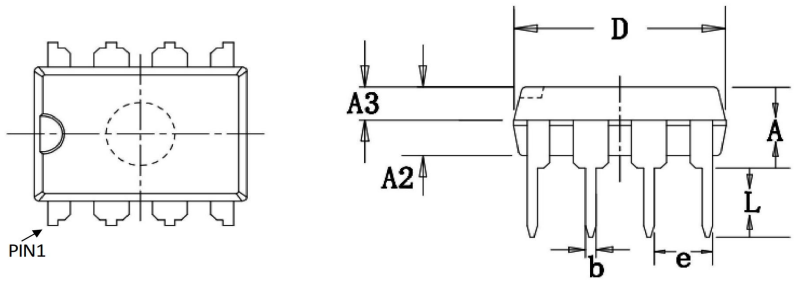
**SOP8**

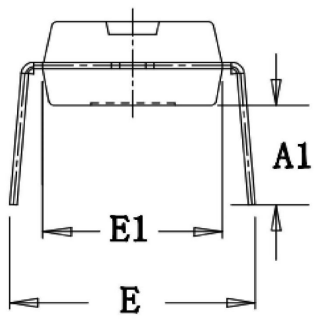



UNIT:mm

| | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.450 | 1.550 | 1.650 |
| A1 | 0.100 | 0.150 | 0.200 |
| A2 | 1.300 | 1.400 | 1.500 |
| A3 | 0.600 | 0.650 | 0.700 |
| b | 0.380 | – | 0.510 |
| e | 1.240 | 1.270 | 1.300 |
| D | 4.800 | 4.900 | 5.000 |
| E | 5.800 | 6.000 | 6.200 |
| E1 | 3.800 | 3.900 | 4.000 |
| L | 0.450 | 0.600 | 0.750 |
| L1 | — | 0.25BSC | — |

## DIP8




UNIT:mm

| | MIN | NOM | MAX |
|---|---|---|---|
| A | 3.600 | 3.800 | 4.000 |
| A1 | 3.786 | 3.886 | 3.986 |
| A2 | 3.200 | 3.300 | 3.400 |
| A3 | 1.550 | 1.600 | 1.650 |
| b | 0.440 | — | 0.490 |
| e | 2.510 | 2.540 | 2.570 |
| D | 9.150 | 9.250 | 9.350 |
| E | 7.800 | 8.500 | 9.200 |
| E1 | 6.280 | 6.380 | 6.480 |
| L | 3.000 | — | — |