

Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, H-PDSO-F8, 750 V, 18 mohm UJ4SC075018L8S

Description

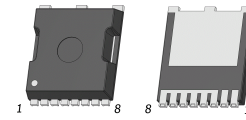
The UJ4SC075018L8S is a 750 V, 18 mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal re-design when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving H-PDSO-F8 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-Resistance $R_{DS(on)}$: 18 mΩ (typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery: Q_{rr} = 128 nC
- Low Body Diode V_{FSD} : 1.14 V
- Low Gate Charge: Q_G = 37.8 nC
- Threshold Voltage $V_{G(th)}$: 4.8 V (typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2
- H-PDSO-F8 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

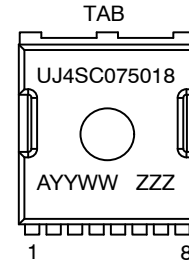
Typical Applications

- Solid State Relays and Circuit-Breakers
- Line Rectification and Active-Bridge Rectification Circuits in AC-DC Front-Ends
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



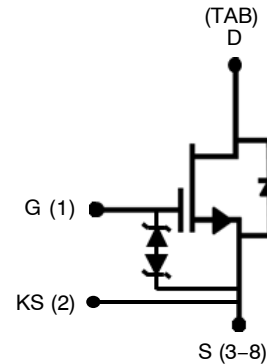
H-PDSO-F8
CASE 740AA

MARKING DIAGRAM



UJ4SC075018 = Specific Device Number
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

UJ4SC075018L8S

MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value	Unit
V_{DS}	Drain-Source Voltage		750	V
V_{GS}	Gate-Source Voltage	DC	-20 to +20	V
		AC ($f > 1$ Hz)	-25 to +25	V
I_D	Continuous Drain Current (Note 1)	$T_C < 118$ °C	53	A
I_{DM}	Pulsed Drain Current (Note 2)	$T_C = 25$ °C	208	A
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	$L = 15$ mH, $I_{AS} = 3.6$ A	97.2	mJ
dv/dt_{rug}	SiC FET dv/dt Ruggedness	$V_{DS} < 500$ V	200	V/ns
P_{tot}	Power Dissipation	$T_C = 25$ °C	349	W
$T_{J,max}$	Maximum Junction Temperature		175	°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to 175	°C
T_{solder}	Reflow Soldering Temperature	Reflow MSL 1	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by bondwires.
2. Pulse width t_p limited by $T_{J,max}$.
3. Starting $T_J = 25$ °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		–	0.33	0.43	°C/W

UJ4SC075018L8S

ELECTRICAL CHARACTERISTICS (T_J = +25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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TYPICAL PERFORMANCE – STATIC

BV _{DS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA	750	–	–	V
I _{DSS}	Total Drain Leakage Current	V _{DS} = 750 V, V _{GS} = 0 V, T _J = 25 °C	–	1.3	45	μA
		V _{DS} = 750 V, V _{GS} = 0 V, T _J = 175 °C	–	20	–	
I _{GSS}	Total Gate Leakage Current	V _{DS} = 0 V, T _J = 25 °C V _{GS} = –20 V / +20 V	–	4.7	20	μA
R _{DS(on)}	Drain-Source On-resistance	V _{GS} = 12 V, I _D = 50 A				
		T _J = 25 °C	–	18	23	mΩ
		T _J = 125 °C	–	29	–	
		T _J = 175 °C	–	37	–	
V _{G(th)}	Gate Threshold Voltage	V _{DS} = 5 V, I _D = 10 mA	4	4.8	6	V
R _G	Gate Resistance	f = 1 MHz, open drain	–	4.5	–	Ω

TYPICAL PERFORMANCE – REVERSE DIODE

I _S	Diode Continuous Forward Current (Note 1)	T _C < 118 °C	–	–	53	A
I _{S,pulse}	Diode Pulse Current (Note 2)	T _C = 25 °C	–	–	208	A
V _{FSD}	Forward Voltage	V _{GS} = 0 V, I _S = 20 A, T _J = 25 °C	–	1.14	1.46	V
		V _{GS} = 0 V, I _S = 20 A, T _J = 175 °C	–	1.35	–	
Q _{rr}	Reverse Recovery Charge	V _{DS} = 400 V, I _S = 50 A, V _{GS} = 0 V, R _G = 50 Ω, di/dt = 1500 A/μs, T _J = 25 °C	–	128	–	nC
t _{rr}	Reverse Recovery Time		–	26.4	–	ns
Q _{rr}	Reverse Recovery Charge	V _{DS} = 400 V, I _S = 50 A, V _{GS} = 0 V, R _G = 50 Ω, di/dt = 1500 A/μs, T _J = 150 °C	–	138	–	nC
t _{rr}	Reverse Recovery Time		–	28	–	ns

TYPICAL PERFORMANCE – DYNAMIC

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 100 kHz	–	1414	–	pF
C _{oss}	Output Capacitance		–	118	–	
C _{rss}	Reverse Transfer Capacitance		–	2	–	
C _{oss(er)}	Effective Output Capacitance, Energy Related	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	150	–	pF
C _{oss(tr)}	Effective Output Capacitance, Time Related		–	280	–	pF
E _{oss}	C _{oss} Stored Energy	V _{DS} = 400 V, V _{GS} = 0 V	–	12	–	μJ
Q _G	Total Gate Charge	V _{DS} = 400 V, I _D = 50 A, V _{GS} = 0 V to 15 V	–	37.8	–	nC
Q _{GD}	Gate-Drain Charge		–	8	–	
Q _{GS}	Gate-Source Charge		–	11.8	–	
t _{d(on)}	Turn-on Delay Time	(Note 4) V _{DS} = 400 V, I _D = 50 A, Gate Driver = 0 V, to +15 V, Turn-on R _{G,EXT} = 1 Ω, Turn-off R _{G,EXT} = 50 Ω, Inductive Load,	–	13.6	–	ns
t _r	Rise Time		–	26.4	–	
t _{d(off)}	Turn-off Delay Time		–	134	–	
t _f	Fall Time		–	18.4	–	
E _{ON}	Turn-on Energy	FWD: same device with V _{GS} = 0 V, R _G = 50 Ω, T _J = 25 °C	–	234	–	μJ
E _{OFF}	Turn-off Energy		–	216	–	
E _{TOTAL}	Total Switching Energy		–	450	–	
t _{d(on)}	Turn-on Delay Time	(Note 4) V _{DS} = 400 V, I _D = 50 A, Gate Driver = 0 V, to +15 V, Turn-on R _{G,EXT} = 1 Ω, Turn-off R _{G,EXT} = 50 Ω, Inductive Load,	–	13	–	ns
t _r	Rise Time		–	31	–	
t _{d(off)}	Turn-off Delay Time		–	136	–	
t _f	Fall Time		–	18.4	–	
E _{ON}	Turn-on Energy	FWD: same device with V _{GS} = 0 V, R _G = 50 Ω, T _J = 150 °C	–	272	–	μJ
E _{OFF}	Turn-off Energy		–	258	–	
E _{TOTAL}	Total Switching Energy		–	530	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the half-bridge mode switching test circuit in Figure 23.

TYPICAL PERFORMANCE DIAGRAMS

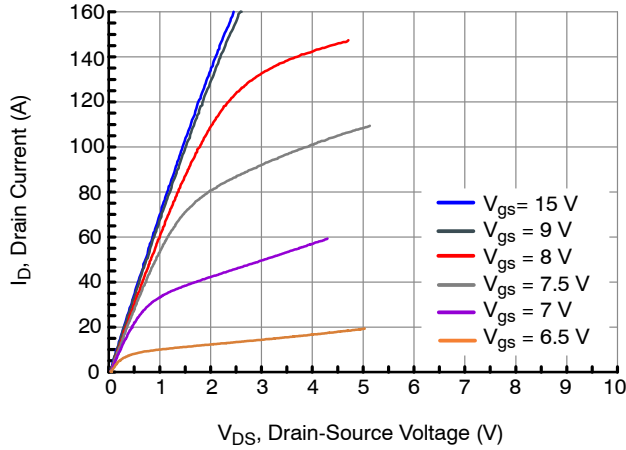


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

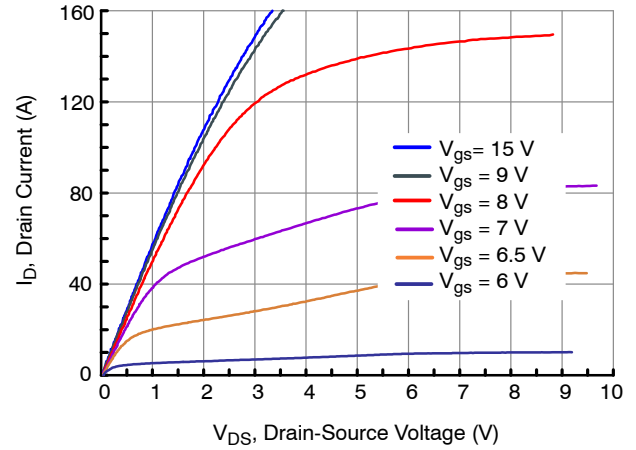


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

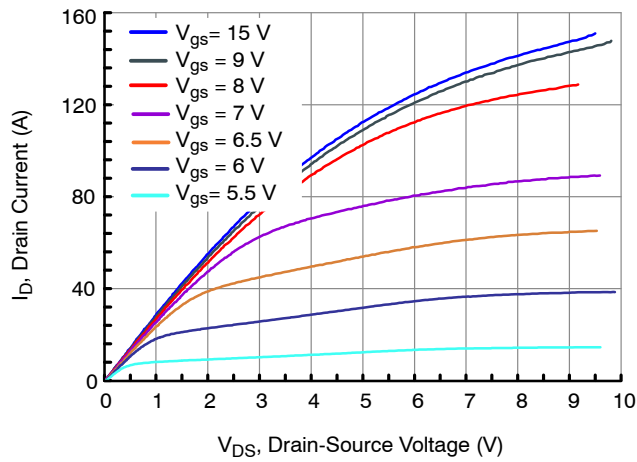


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

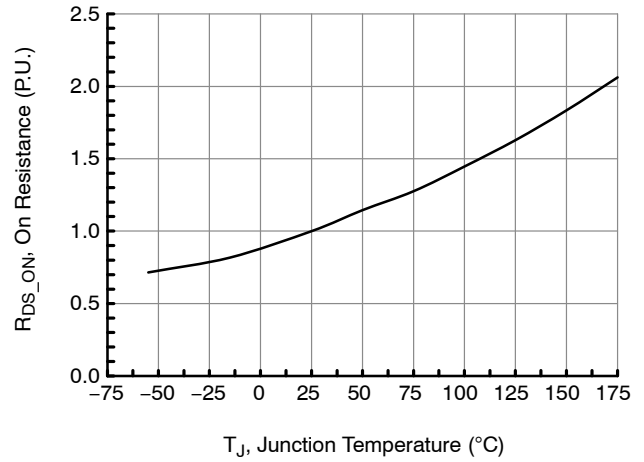


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12\text{ V}$ and $I_D = 50\text{ A}$

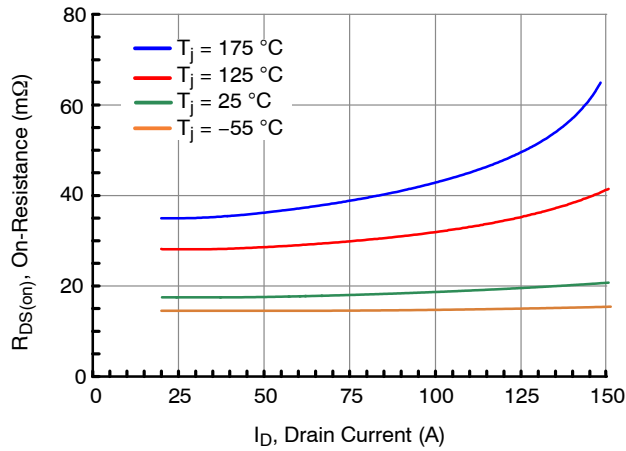


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12\text{ V}$

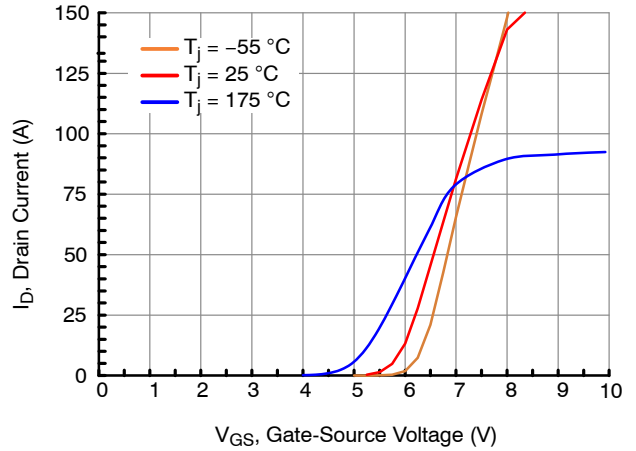


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

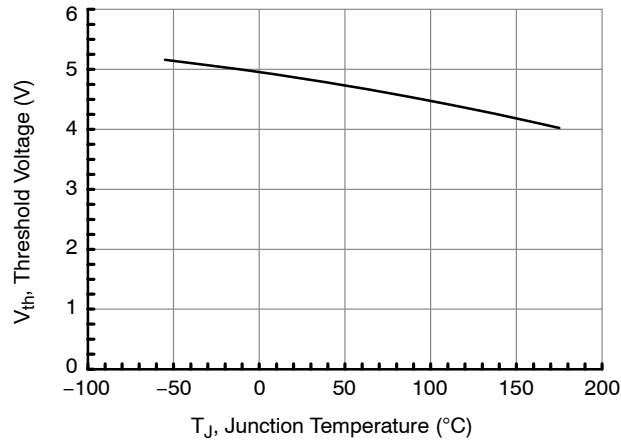


Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

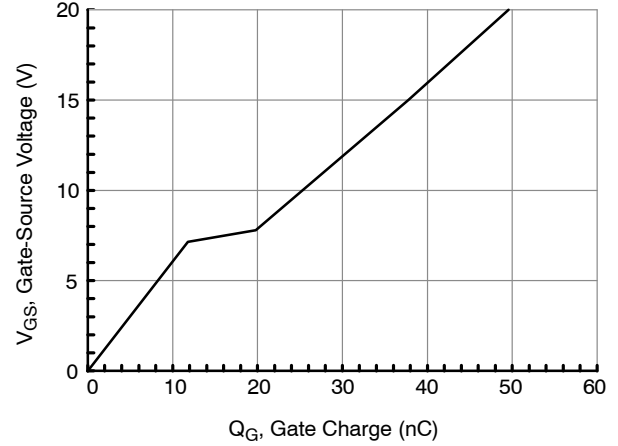


Figure 8. Typical Gate Charge at $V_{DS} = 400\text{ V}$ and $I_D = 50\text{ A}$

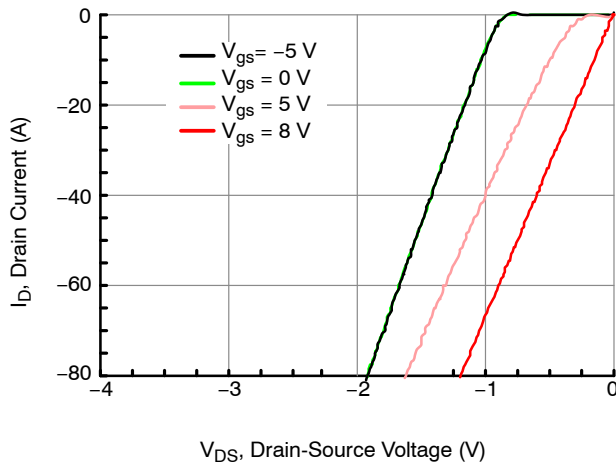


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ °C}$

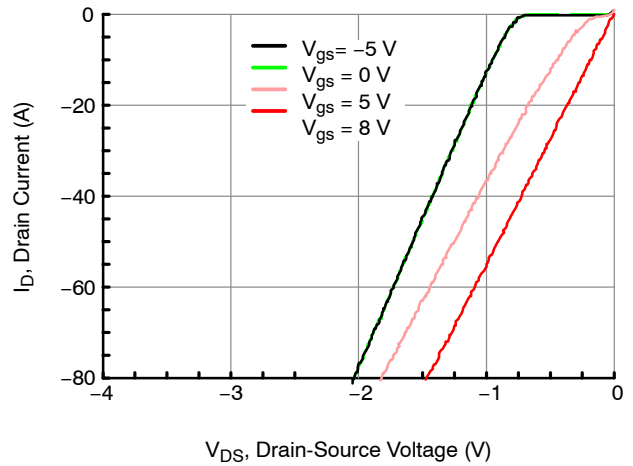


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ °C}$

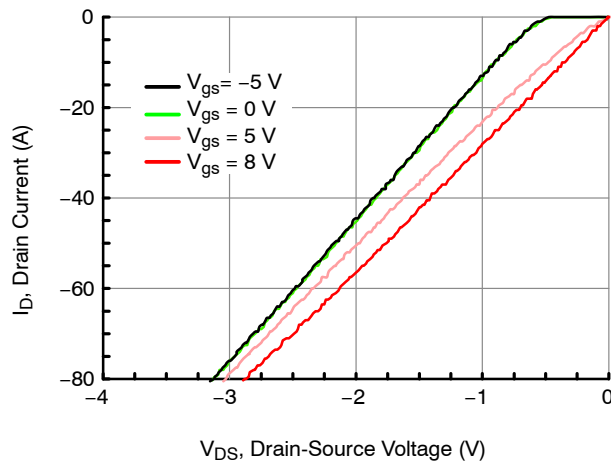


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ °C}$

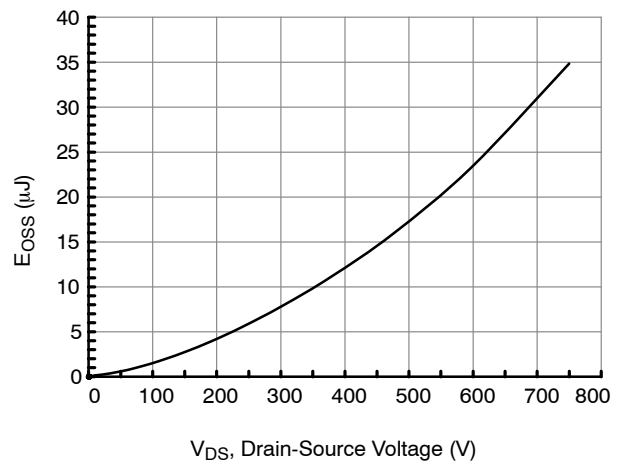


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

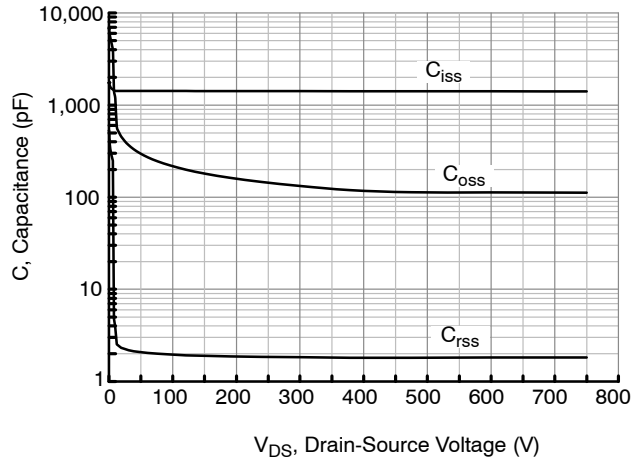


Figure 13. Typical Capacitances at $f = 100 \text{ kHz}$ and $V_{GS} = 0 \text{ V}$

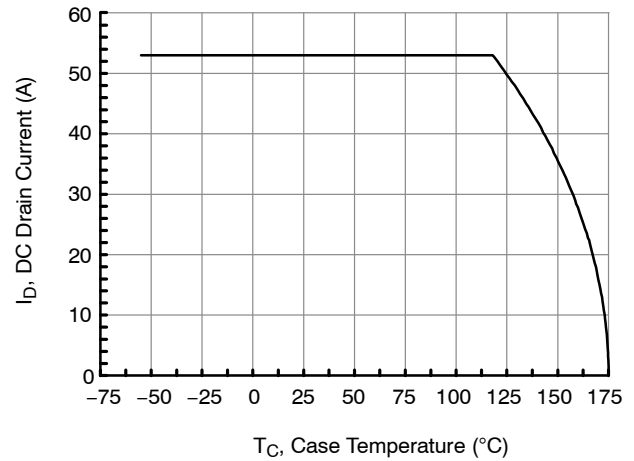


Figure 14. DC Drain Current Derating

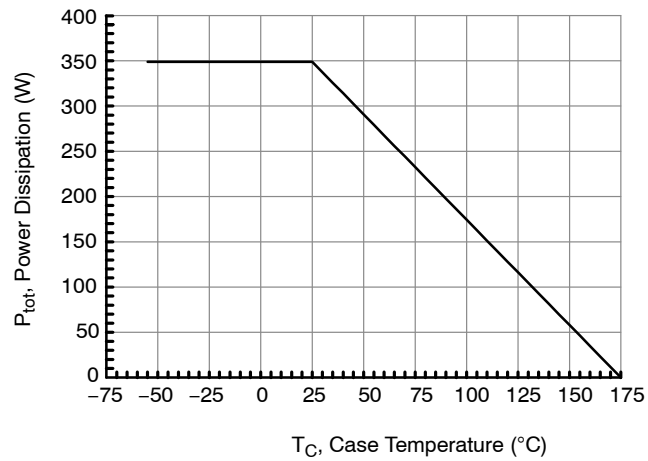


Figure 15. Total Power Dissipation

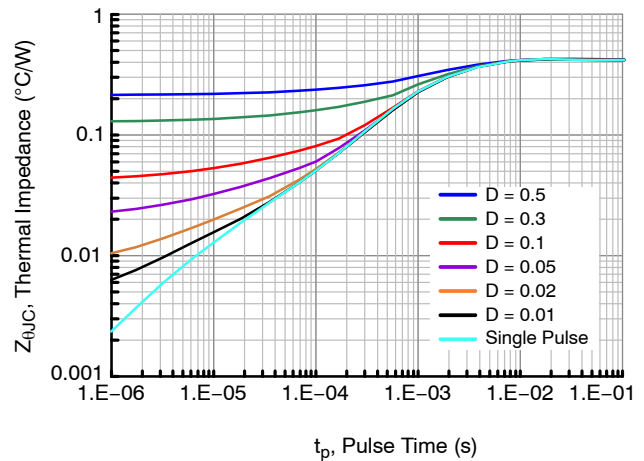


Figure 16. Maximum Transient Thermal Impedance

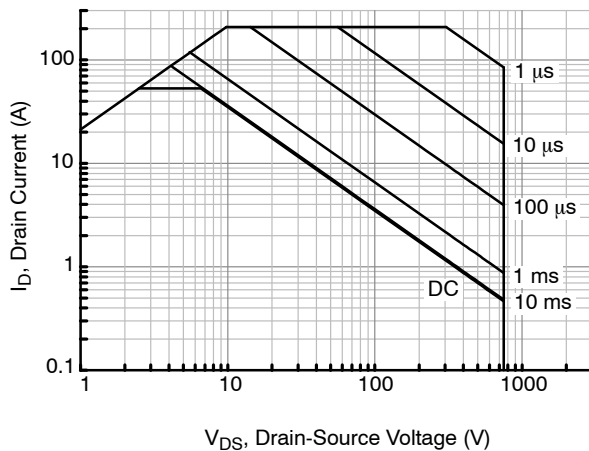


Figure 17. Safe Operation Area at $T_C = 25 \text{ °C}$, $D = 0$, Parameter t_p

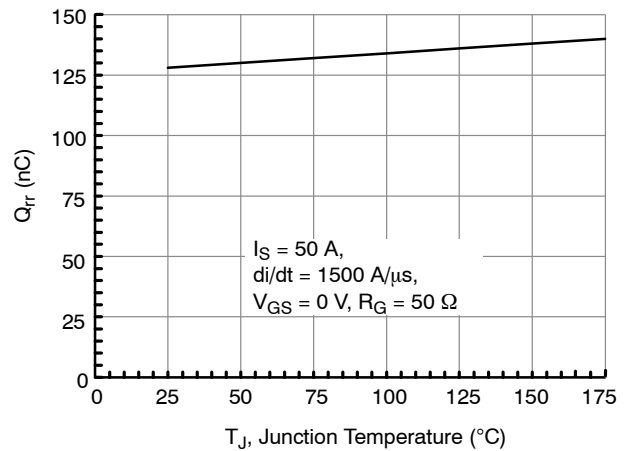


Figure 18. Reverse Recovery Charge Q_{rr} vs. Junction Temperature at $V_{DS} = 400 \text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

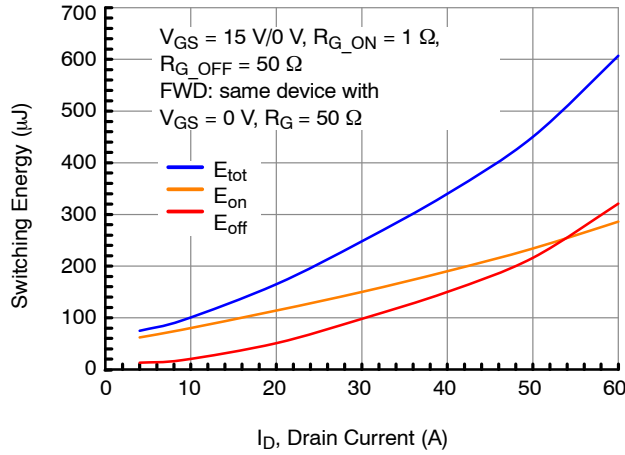


Figure 19. Clamped Inductive Switching Energy vs. Drain Current at $V_{DS} = 400$ V and $T_J = 25$ °C

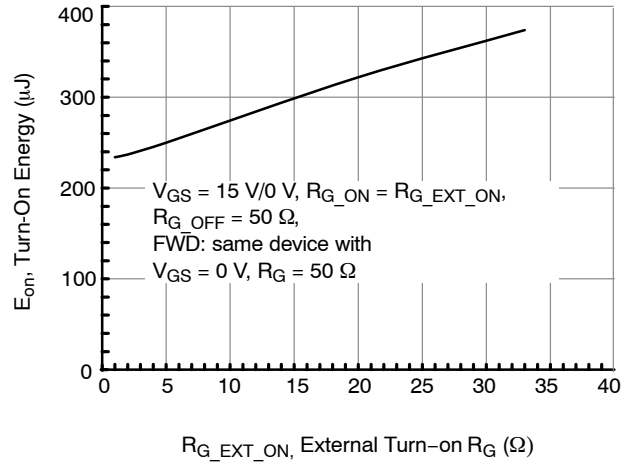


Figure 20. Clamped Inductive Switching Turn-on Energy vs. $R_{G_EXT_ON}$ at $V_{DS} = 400$ V and $I_D = 50$ A

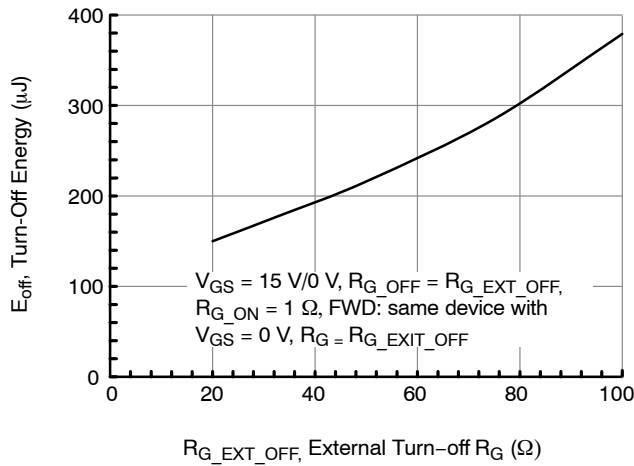


Figure 21. Clamped Inductive Switching Turn-off Energy vs. $R_{G_EXT_OFF}$ at $V_{DS} = 400$ V, and $I_D = 50$ A

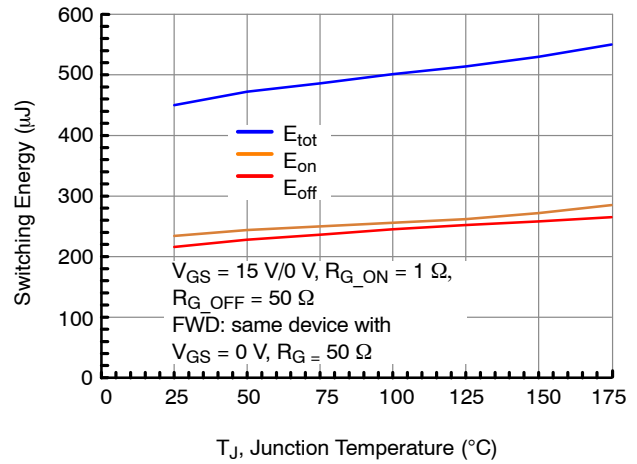


Figure 22. Clamped Inductive Switching Energy vs. Junction Temperature at $V_{DS} = 400$ V and $I_D = 50$ A

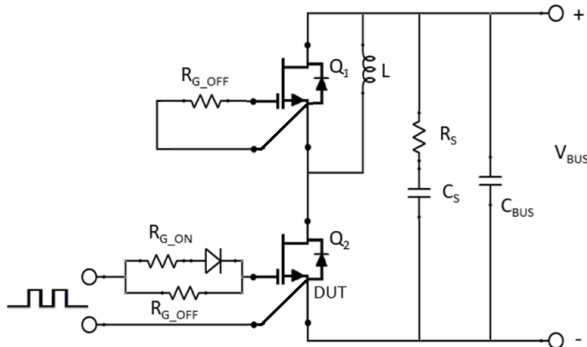


Figure 23. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, a Bus RC Snubber ($R_S = 2.5$ Ω, $C_S = 100$ nF) is Used to Reduce the Power Loop High Frequency Oscillations.

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is

working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com

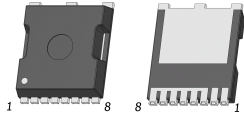
ORDERING INFORMATION

Part Number	Marking	Package	Shipping†
UJ4SC075018L8S	UJ4SC075018	H-PDSO-F8 (Pb-Free, Halogen Free)	2,000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](http://www.onsemi.com).

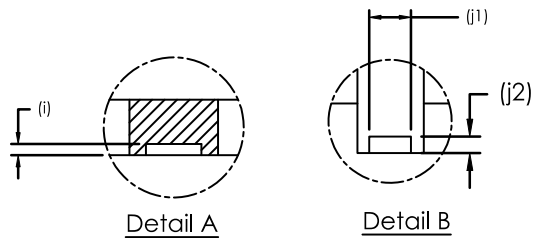
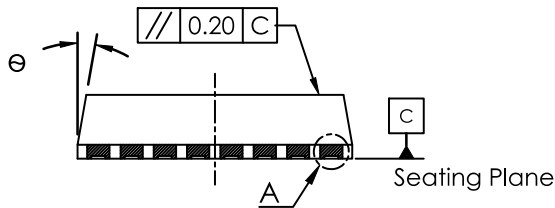
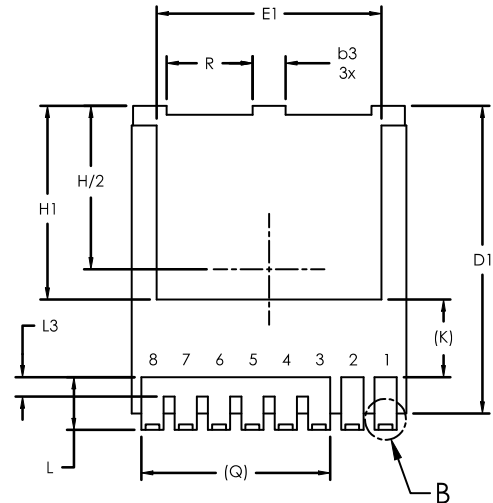
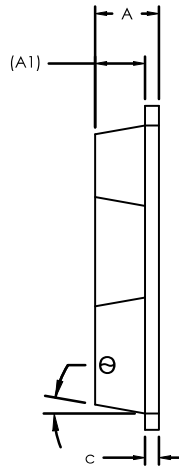
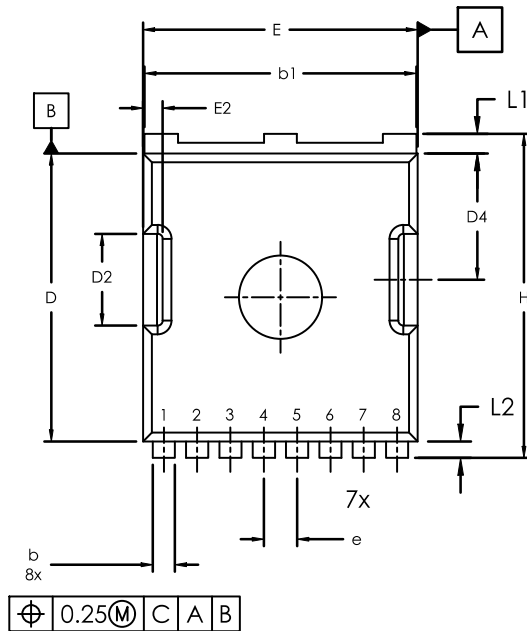
REVISION HISTORY

Revision	Description of Changes	Date
B	Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with onsemi standards for SiC products.	1/15/2025
2	Converted the Data Sheet to onsemi format.	4/28/2025



H-PDSO-F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025



Note:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimensions does not include Burrs and Mold Flashes

TO-LL			
SYMBOL	Value		
	Min	Nom	Max
A	2.15	2.30	2.45
A1	1.80 REF		
b	0.65	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.88	11.08	11.28
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e	1.20 BSC		
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i	0.10 REF		
j1	0.46 REF		
j2	0.20 REF		
K	2.80 REF		
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q	6.80 REF		
R	3.00	3.10	3.20
theta	10°		

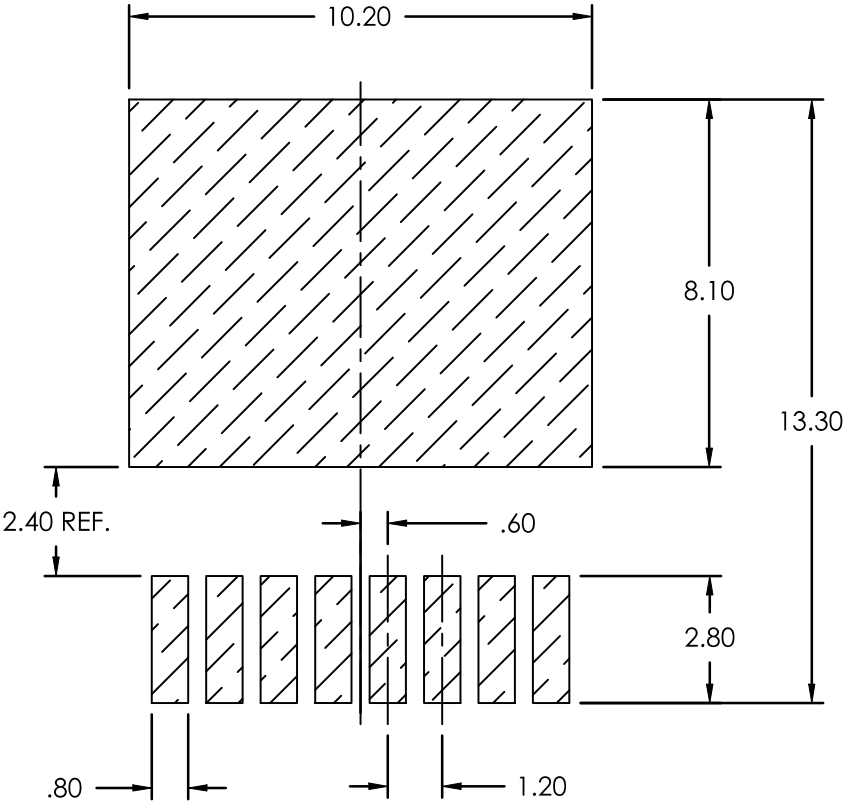
DOCUMENT NUMBER:	98AON26704H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	H-PDSO-F8 9.90x10.38x2.30, 1.20P	PAGE 1 OF 2

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H-PDSO-F8 9.90x10.38x2.30, 1.20P
CASE 740AA
ISSUE B

DATE 24 JUN 2025

RECOMMENDED PCB LAND PATTERN



NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

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