



BRT40N100P2

N-channel Enhancement Mode Power MOSFET

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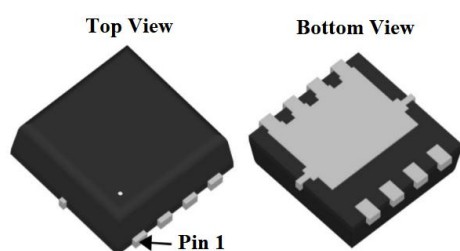
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FEATURES

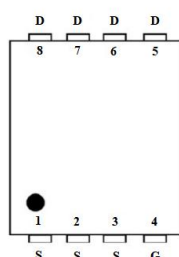
- ◆ 40V, 100A
- $R_{DS(ON)} < 2.9m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 4.5m\Omega @ V_{GS} = 4.5V$
- ◆ Advanced Trench Technology
- ◆ Excellent $R_{DS(ON)}$ and Low Gate Charge
- ◆ Lead Free

APPLICATIONS

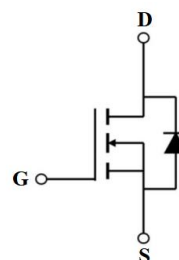
- ◆ Load Switch
- ◆ PWM Application
- ◆ Power Management



PDFN5*6-8L



Pin Assignment



Schematic Diagram

PACKAGE MARKING AND ORDERING INFORMATION

OPN	Package	Quantity
BRT40N100P2	PDFN5*6-8L	5000pcs/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Ratings	Unit
V_{DS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	100	A
		$T_C = 100^\circ C$	63	A
I_{DM}	Pulsed Drain Current ⁽¹⁾		400	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾		306	mJ
P_D	Power Dissipation, $T_C = 25^\circ C$		125	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.0	$^\circ C/W$
T_J, T_{STG}	Junction & Storage Temperature Range		-55 ~ +150	$^\circ C$

ELECTRICAL CHARACTERISTICS (All test condition is $T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40V, V _{GS} = 0V	-	-	1	uA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250uA	1.0	1.5	2.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽³⁾	V _{GS} = 10V, I _D = 30A		2.4	2.9	mΩ
		V _{GS} = 4.5V, I _D = 20A		3.0	4.5	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz	4376	6152	8270	pF
C _{oss}	Output Capacitance		358	487	677	pF
C _{rss}	Reverse Transfer Capacitance		249	313	470	pF
R _g	Gate Resistance	f = 1MHz	-	1.4	-	Ω
Q _g	Total Gate Charge	V _{GS} = 0 to 10V V _{DS} = 20V, I _D = 30A	79	111	150	nC
Q _{gs}	Gate Source Charge		14	20	27	nC
Q _{gd}	Gate Drain("Miller") Charge		15	23	28	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{GS} = 10V, V _{DD} = 19.5V I _D = 30A, R _{GEN} = 3Ω	-	14	-	ns
t _r	Turn-On Rise Time		-	28	-	ns
t _{d(off)}	Turn-Off Delay Time		-	77	-	ns
t _f	Turn-Off Fall Time		-	23	-	ns
Drain-Source Diode Characteristics						
I _S	Continuous Source Current		-	-	100	A
V _{SD}	Forward on voltage	V _{GS} = 0V, I _S = 30A	-	-	1.2	V
T _{rr}	Reverse Recovery Time	I _F = 30A, di/dt = 100A/us	18	25	33	ns
Q _{rr}	Reverse Recovery Charge		-	16	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J=25^{\circ}\text{C}$, $V_{DD}=15\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=35.56\text{A}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1: Power De-rating

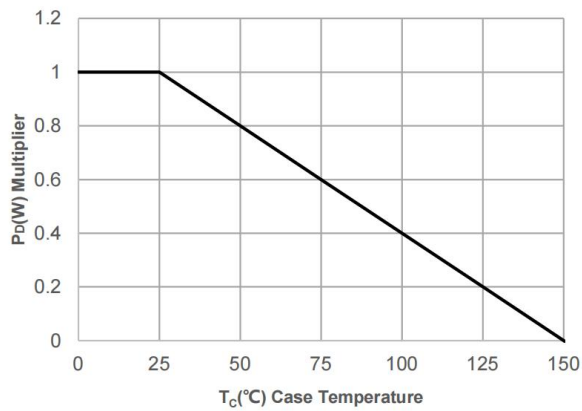


Figure 2: Current De-rating

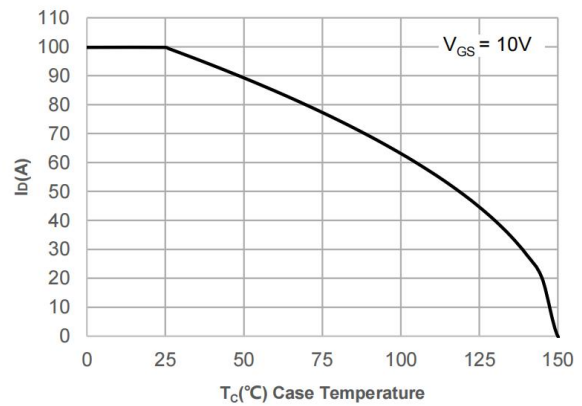


Figure 3: Normalized Maximum Transient Thermal Impedance

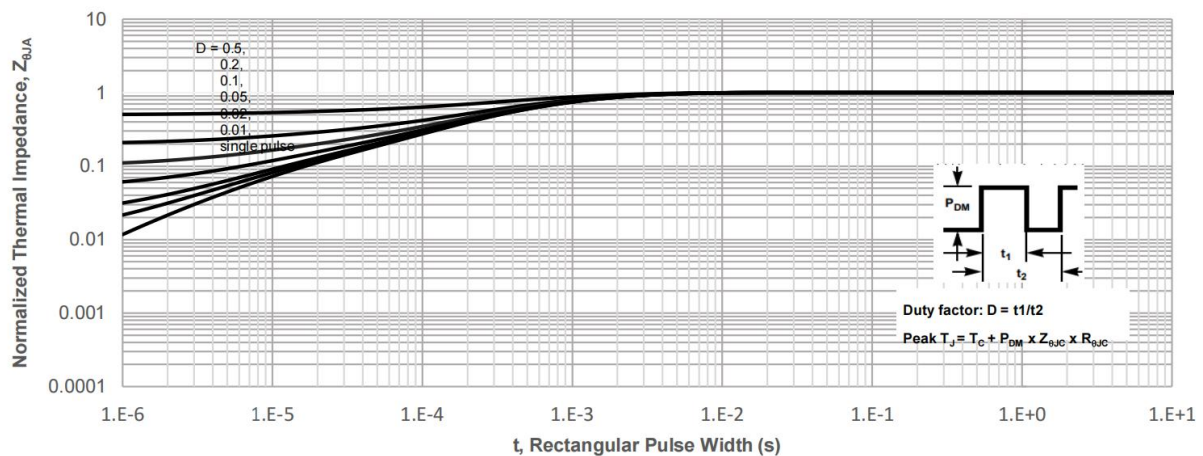
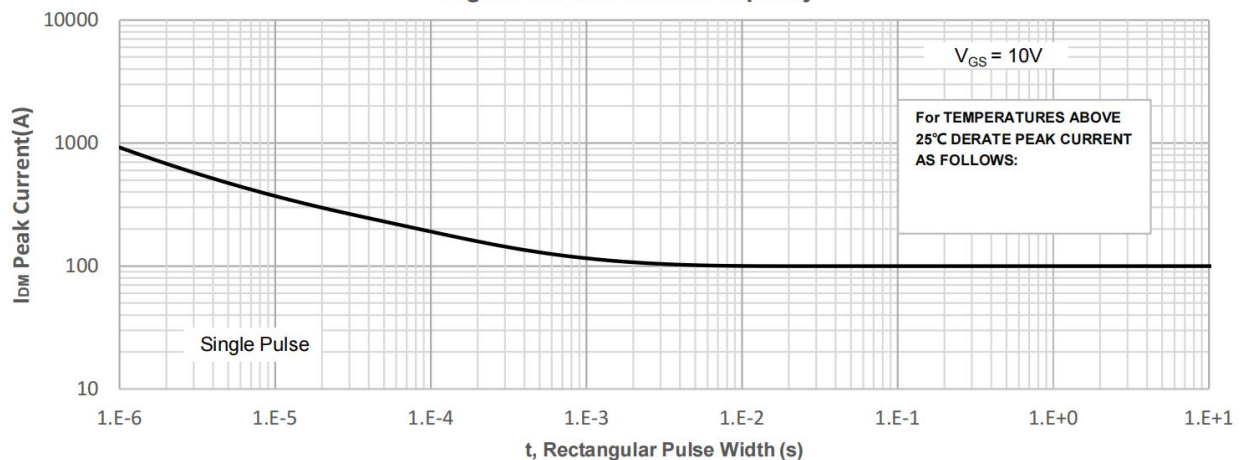


Figure 4: Peak Current Capacity



TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5: Output Characteristics

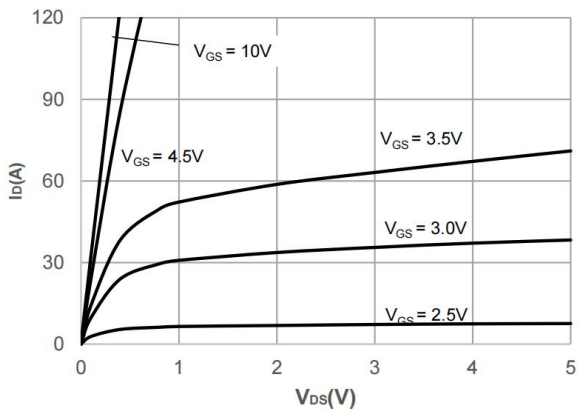


Figure 6: Typical Transfer Characteristics

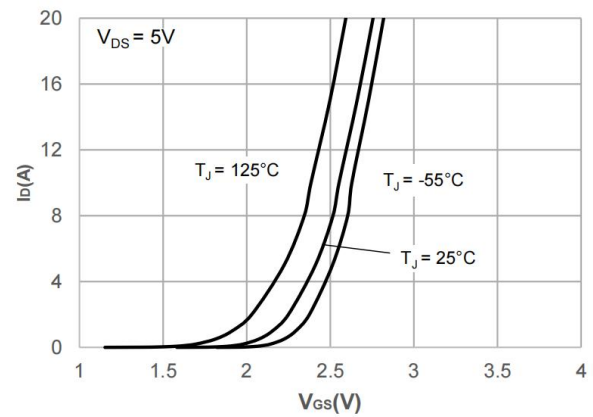


Figure 7: On-resistance vs. Drain Current

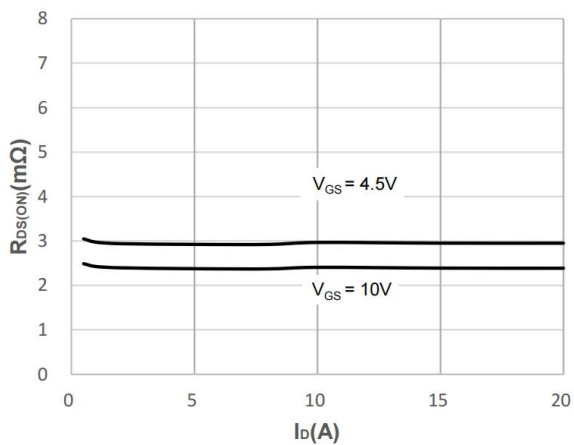


Figure 8: Body Diode Characteristics

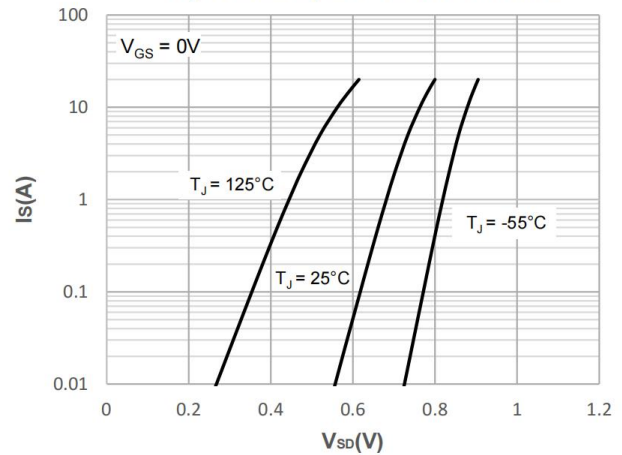


Figure 9: Gate Charge Characteristics

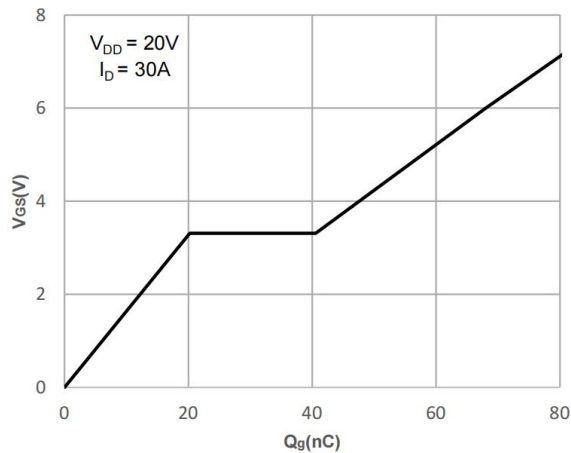
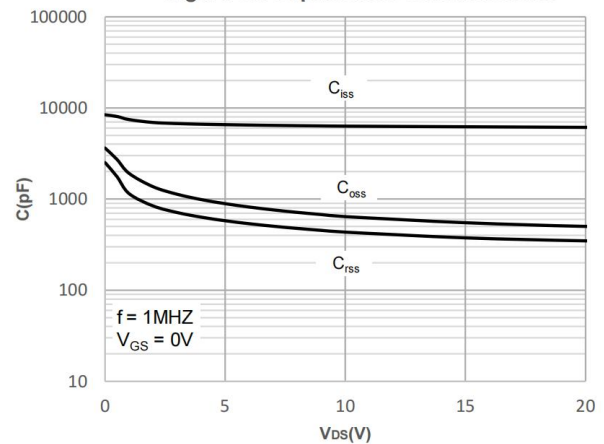


Figure 10: Capacitance Characteristics



TYPICAL PERFORMANCE CHARACTERISTICS

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

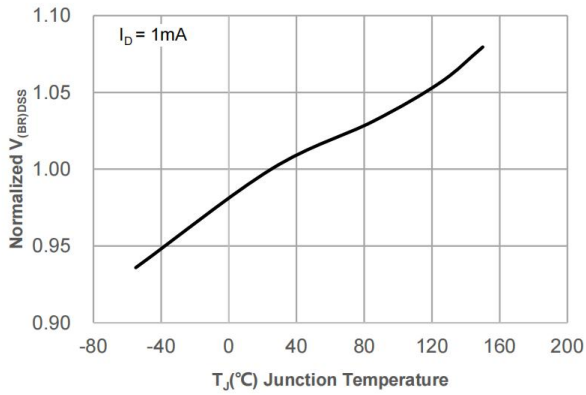


Figure 12: Normalized on Resistance vs. Junction Temperature

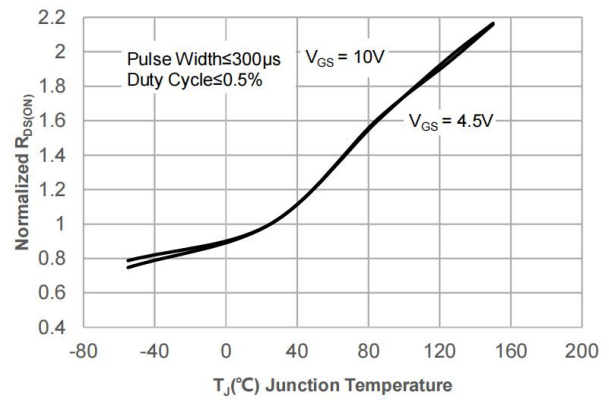


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

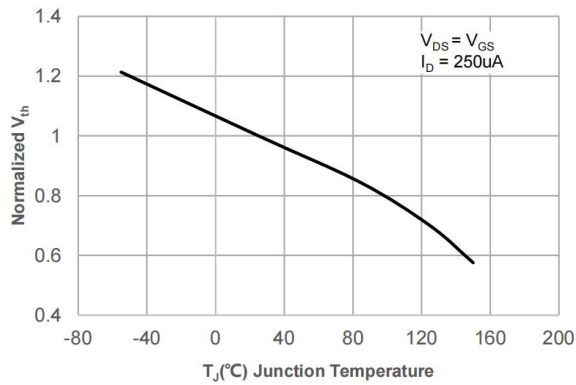


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

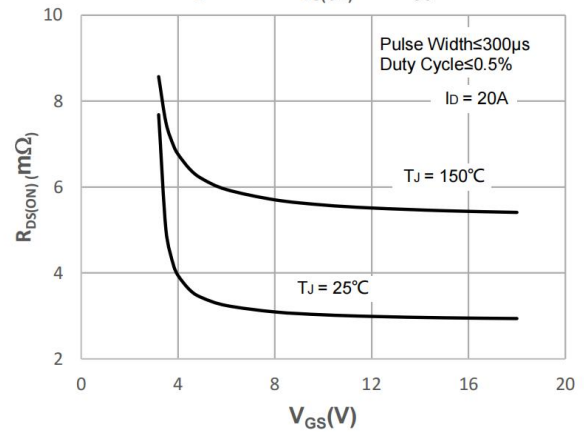
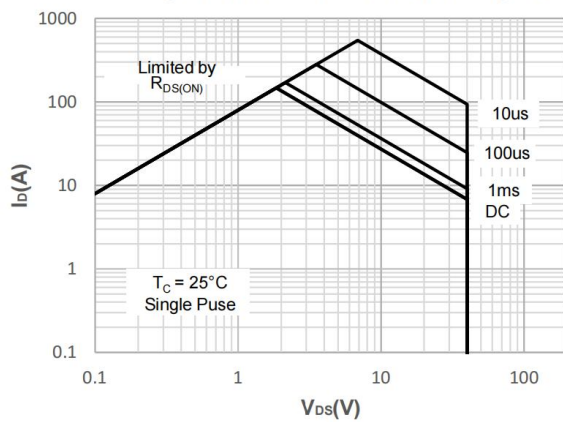


Figure 15: Maximum Safe Operating Area



TEST CIRCUIT

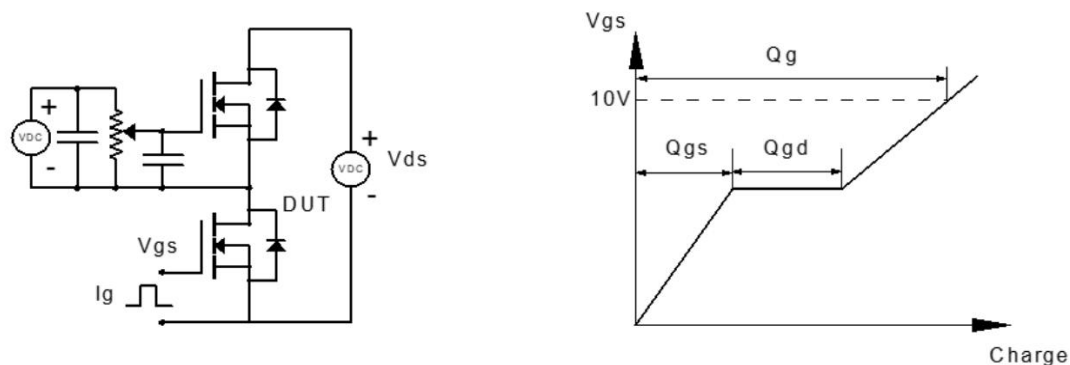


Figure 16: Gate Charge Test Circuit & Waveform

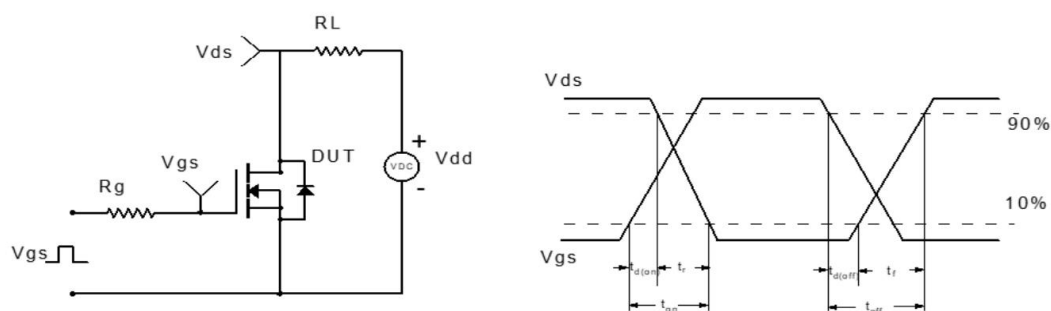


Figure 17: Resistive Switching Test Circuit & Waveform

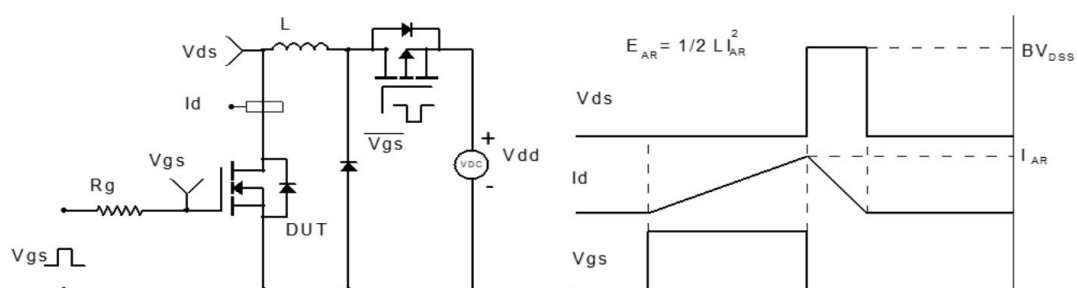


Figure 18: Unclamped Inductive Switching Test Circuit & Waveform

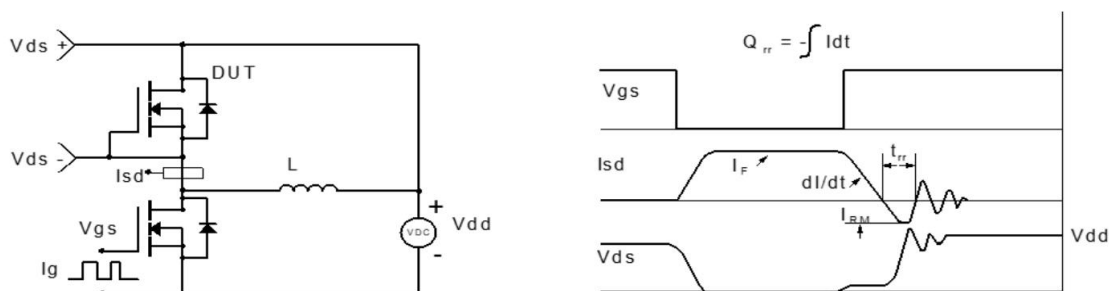
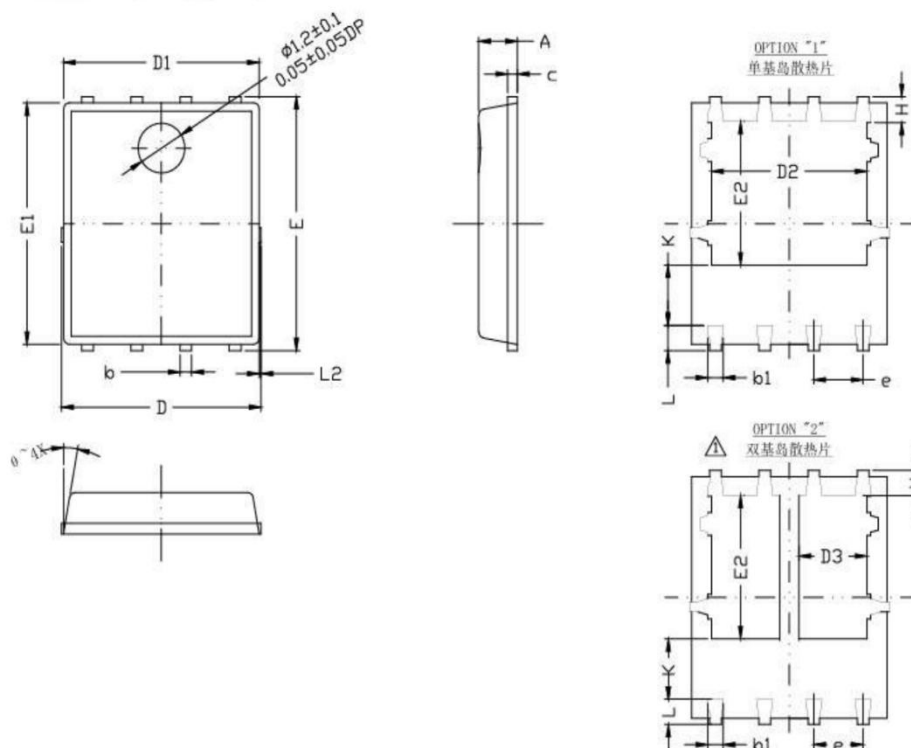


Figure 19: Diode Recovery Test Circuit & Waveform

DETAIL PACKAGE OUTLINE DRAWING (PDFN5*6-8L)



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.25	0.30	0.35
b1	0.30	0.40	0.45
c	0.22	0.25	0.28
D	-	-	5.30
D1	4.90	5.05	5.20
D2	4.01 REF.		
D3	1.75 REF.		
E	6.00	6.15	6.30
E1	5.70	5.85	6.00
E2	3.48 REF.		
e	1.10	1.27	1.40
H	0.61	0.71	0.81
K	1.10	-	-
L	0.51	0.61	0.71
L2	-	-	0.10
θ	8°	-	12°

REVISION HISTORY

Number	Description
Rev 1.0	BRT40N100P2 datasheet release