SUL60512 Sink and Source DDR Termination Regulator

General Description

The SUL60512 is a linear regulator designed to meet the JEDEC SSTL (Series Stub Termination Logic) specifications in DDRI/II/III/IIIL/IV –SDRAM systems.

It is designed for the system which has low input voltage, low cost, low noise, and space consideration.

The SUL60512 provides accurate and fast response with amperage source/sink ability in load transient to track reference voltage with typically 20μF output capacitor. The terminated voltage can be generated by two external resistors or programmed by forcing REFIN pin at a desired voltage.

Also the SUL60512 provides an open-drain PGOOD flag which monitors the output regulation and an EN signal to discharge VTT during STR (S3) mode.

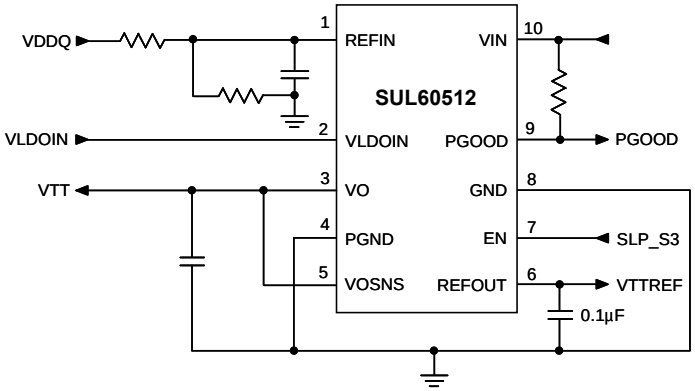
Features

- VIN Input Voltage Range: 2.5V to 5.5V
- VLDOIN Voltage Range: 1.0V to 3.5V
- Support DDR I (1.25 VTT), DDR II (0.9 VTT), DDR III (0.75 VTT), DDR IIIL (0.675VTT) and DDR IV (0.6 VTT) Requirements
- Stable with Output Ceramic Capacitor
- PGOOD to Monitor Output Regulation
- EN Input for Shutdown Function (S3 Mode)
- Remote Sensing (VOSNS)
- ± 25mV Accuracy for VTT Refers to VTTREF
- ± 10mA Buffered Reference (VTTREF)
- Built-In Soft-Start and UVLO
- Over Current Protection
- Thermal Shutdown Protection
- TDFN3X3-10L (Thermal Pad) Package
- Lead free and halogen free

Applications

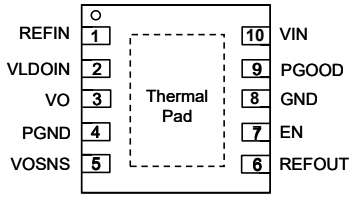
- Memory Termination Regulator for DDR I/II/ III/IIIL, Low-Power DDR III/IV
- Notebooks, Desktops and Servers
- Telecom/Datacom, Base Stations, LCD-TVs/PDP-TVs, Copiers/Printers, Set-Top Boxes

Typical Application Circuit



Pin Configuration

TOP VIEW



TDFN3X3-10L

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Pin Description

PIN	NAME	DESCRIPTIONS
1	REFIN	Terminator reference input voltage, 1.25V for DDR I, 0.9V for DDR II, 0.75V for DDR III, 0.675V for DDR IIIL, 0.6V for DDR IV.
2	VLDOIN	Terminator power pin.
3	VO	Terminator output pin.
4	PGND	Terminator power ground.
5	VOSNS	Voltage sense input pin, connect to remote termination.
6	REFOUT	Terminator reference output pin.
7	EN	ON/OFF function for SLP_S3 mode.
8	GND	Ground.
9	PGOOD	PGOOD open-drain output.
10	VIN	Internal circuit power pin, at least 2.5V.
Thermal Pad	/	Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Ordering Information

PART NO	PACKAGE	TEMPERATURE	QTY/REEL
SUL60512	TDFN3X3-10L	-40°C~+85°C	3000 PCS

SUL60512 devices are Pb-free and RoHS compliant.

Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	VIN,VLDOIN,VOSNS,REFIN,EN	-0.3~+6.5	V
	PGND,GND	-0.3~0.3	V
	VO	-0.3~VLDOIN+0.3	V
	REFOUT,PGOOD	-0.3~+6.5	V
Thermal Resistance of Junction to Ambient	θJA	69	°C/W
Continuous Power Dissipation (TA = +25°C)	PD	1.8	W
Thermal Resistance Junction to Case	θJC	16.5	°C/W
Maximum Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55~150	°C
Reflow Temperature (soldering)		260	°C

Recommend Operating Conditions[Note1]

PARAMETER	VALUE	UNIT
VIN	2.5~5.5	V
VLDOIN	1V~ min(3.5,VIN-1)	V
VOSNS,VO	-0.1V~ min(3.5,VIN-1)	V
EN	-0.1~3.5	V
REFIN	0.5~1.8	V
PGOOD	-0.1~5.5	V
REFOUT	-0.1~1.8	V
PGND,GND	-0.1~0.1	V
TA, Operating Ambient Temperature Range	-40~+85	°C

Note1: All voltage values are with respect to the network ground terminal unless otherwise noted.

Electrical Characteristics

T_A=-40°C~+85°C, V_{VIN}=5V, V_{VLDOIN}=1.5V, V_{REFIN}=0.75V, and V_{EN}=V_{VIN}, Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	I_{VIN}	V_{VIN}=5V, no load, V_{EN}=5V	---	0.7	1	mA
VIN standby current	I_{VINSTB}	V_{VIN}=5V, no load, V_{EN}=0V, V_{REFIN}>0.4V	---	200	400	µA
VIN shutdown current	I_{VINSDN}	V_{VIN}=5V, no load, V_{EN}=0V, V_{REFIN}=0V	---	65	150	µA
VLDOIN supply current	I_{VLDOIN}	V_{VIN}=5V, no load	---	1	100	µA
VLDOIN standby current	$I_{VLDOINSTB}$	V_{VIN}=5V, no load, V_{EN}=0V, V_{REFIN}>0.4V	---	0.1	50	µA
VLDOIN shutdown current	$I_{VLDOINSDN}$	V_{VIN}=5V, no load, V_{EN}=0V, V_{REFIN}=0V	---	0.1	50	µA
REFIN input current	I_{REFIN}	V_{EN}=5V	---	---	1	µA
VOSNS input current	I_{VOSNS}	V_{VIN}=5V, no load, V_{EN}=5V	---	---	1	µA
VTT output voltage	V_{VTT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
VTT output voltage tolerance refer to REOUT	V_{VTTOS}	I_{VTT}=0	-20	---	20	mV
VTT output voltage tolerance refer to REFOUT	ΔV_{VTT}	$\|I_{VTT}\|$<2A	-30	---	30	mV
VTT source current limit	$I_{VOCLSRC}$	VTT=REFIN *0.90, PGOOD=Hi	3	4	---	A
VTT sink current limit	$I_{VOCLSNK}$	VTT=REFIN *1.1, PGOOD=Hi	3	4	---	A
VO discharge current	$I_{DISCHARGE}$	V_{REFIN}=0V, V_{VTT}=0.3V, V_{EN}=0V	---	18	25	Ω
PGOOD threshold	V_{PGTH}	PGOOD lower threshold refer to REFOUT	---	-20	---	%
		PGOOD upper threshold refer to REFOUT	---	20	---	
		PGOOD hysteresis	---	5	---	
PGOOD startup delay	$T_{PGSTUPDLY}$	VOSNS is within 15% of REFOUT	---	2	---	ms
PGOOD bad delay	$T_{PGBADDLY}$	VOSNS is outside 20% of REFOUT	---	10	---	µs
PGOOD output low voltage	$V_{PGOODLOW}$	I_{SINK}=4mA	---	---	0.6 5	V
PGOOD leakage current	$I_{PGOODLK}$	VOSNS is inside of PGOOD window	---	---	1	µA
REFIN UVLO threshold	$V_{REFINUVLO}$	REFIN rising	0.36	0.39	0.42	V
		Hysteresis	---	20	---	mV
REFOUT output voltage	V_{REFOUT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
REFOUT output voltage tolerance refer to REFIN	ΔV_{REFOUT}	-10mA < I_{REFOUT}< 10mA	-25	---	25	mV
REFOUT source current limit	$I_{REFOUTSRCL}$	V_{REFOUT}=0V	10	40	---	mA
REFOUT sink current limit	$I_{REFOUTSNCL}$	V_{REFOUT}=VIN	10	40	---	mA
VIN UVLO threshold	$V_{VINUVLO}$	VIN rising	2.1	2.3	2.4	V
		Hysteresis	---	50	---	mV
EN input voltage threshold	V_{ENTH}	Enable rising	1.7	---	---	V
		Enable falling	---	---	0.3	
		Hysteresis	---	0.5	---	
Logic input leakage current	I_{ENLEAK}		-1	---	1	µA
Thermal Shutdown	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		---	25	---	°C

Electrical Characteristics (Continued)

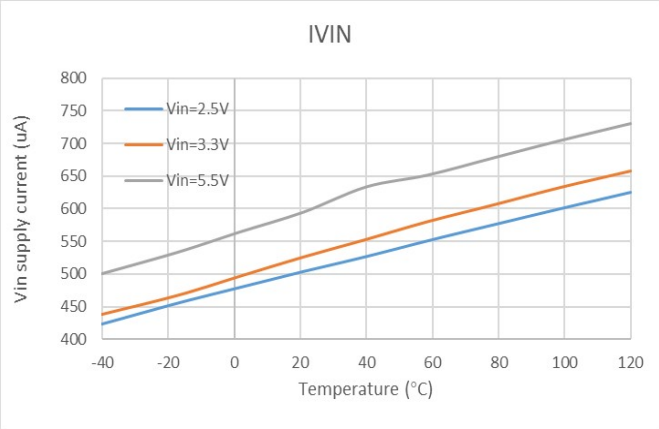
T_A=-40°C~+85°C, V_{VIN}=3.3V, V_{VLDOIN}=1.5V, V_{REFIN}=0.75V, and V_{EN}=V_{VIN}, Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	I_{VIN}	V_{VIN}=3.3V, no load, V_{EN}=3.3V	---	0.7	1	mA
VIN standby current	I_{VINSTB}	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}>0.4V	---	200	400	µA
VIN shutdown current	I_{VINSDN}	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}=0V	---	65	150	µA
VLDOIN supply current	I_{VLDOIN}	V_{VIN}=3.3V, no load	---	1	50	µA
VLDOIN standby current	$I_{VLDOINSTB}$	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}>0.4V	---	0.1	50	µA
VLDOIN shutdown current	$I_{VLDOINSDN}$	V_{VIN}=3.3V, no load, V_{EN}=0V, V_{REFIN}=0V		0.1	50	µA
REFIN input current	I_{REFIN}	V_{EN}=3.3V	---	---	1	µA
VOSNS input current	I_{VOSNS}	V_{VIN}=3.3V, no load, V_{EN}=3.3V	---	---	1	µA
VTT output voltage	V_{VTT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
VTT output voltage tolerance refer to REOUT	V_{VTTOS}	I_{VTT}=0	-20	---	20	mV
VTT output voltage tolerance refer to REFOUT	ΔV_{VTT}	$\|I_{VTT}\|$<2A	-30	---	30	mV
VTT source current limit	$I_{VOCLSRC}$	VTT=REFIN *0.90, PGOOD=Hi	3	4	---	A
VTT sink current limit	$I_{VOCLSNK}$	VTT=REFIN *1.1, PGOOD=Hi	3	4	---	A
VO discharge current	$I_{DISCHARGE}$	V_{REFIN}=0V, V_{VTT}=0.3 V, V_{EN}=0V	---	18	25	Ω
PGOOD threshold	V_{PGTH}	PGOOD lower threshold refer to REFOUT	---	-20	---	%
		PGOOD upper threshold refer to REFOUT	---	20	---	
		PGOOD hysteresis	---	5	---	
PGOOD startup delay	$T_{PGSTUPDLY}$	VOSNS is within 15% of REFOUT	---	2	---	ms
PGOOD bad delay	$T_{PGBADDLY}$	VOSNS is outside 20% of REFOUT	---	10	---	µs
PGOOD output low voltage	$V_{PGOODLOW}$	I_{SINK} =4mA	---	---	0.65	V
PGOOD leakage current	$I_{PGOODLK}$	VOSNS is inside of PGOOD window	---	---	1	µA
REFIN UVLO threshold	$V_{REFINUVLO}$	REFIN rising	0.36	0.39	0.42	V
		Hysteresis	---	20	---	mV
REFOUT output voltage	V_{REFOUT}	DDR I	---	1.25	---	V
		DDR II	---	0.9	---	
		DDR III	---	0.75	---	
		DDR IIIL	---	0.675	---	
		DDR IV	---	0.6	---	
REFOUT output voltage tolerance refer to REFIN	ΔV_{REFOUT}	-10mA < I_{REFOUT}< 10mA	-25	---	25	mV
REFOUT source current limit	$I_{REFOUTSRCL}$	V_{REFOUT}=0V	10	40	---	mA
REFOUT sink current limit	$I_{REFOUTSNCL}$	V_{REFOUT}=VIN	10	40	---	mA
VIN UVLO threshold	$V_{VINUVLO}$	VIN rising	2.1	2.3	2.4	V
		Hysteresis	---	50	---	mV
EN input voltage threshold	V_{ENTH}	Enable rising	1.7	---	---	V
		Enable falling	---	---	0.3	
		Hysteresis	---	0.5	---	
Logic input leakage current	I_{ENLEAK}		-1	---	1	µA
Thermal Shutdown	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		---	25	---	°C

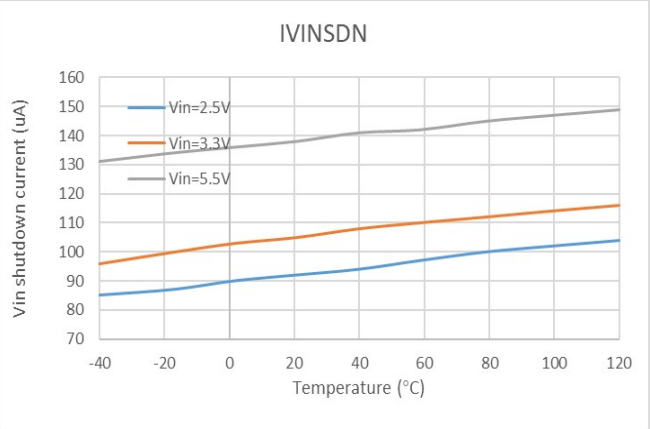
Electrical Characteristics

C_{VLDOIN}=20μF/MLCC/X5R, C_{VIN}=4.7μF/MLCC/X7R, C_{REFOUT}=0.1μF/MLCC/X7R, C_{OUT}=20μF/MLCC/X5R, T_A=25°C, VDDQ=1.5V, VLDOIN=1.5V, unless otherwise noted.

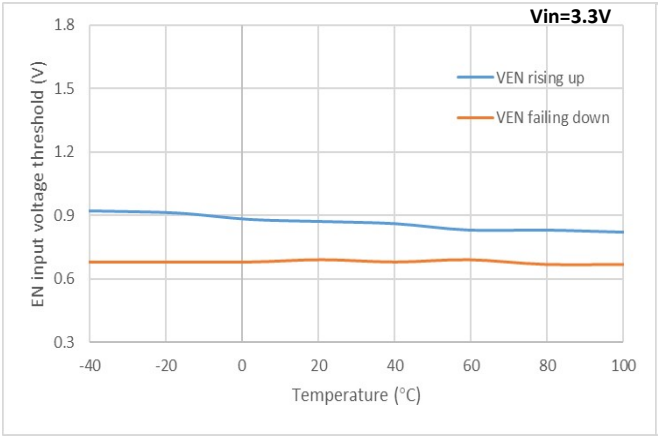
Vin supply current vs Ambient Temperature: (Iout=0A)



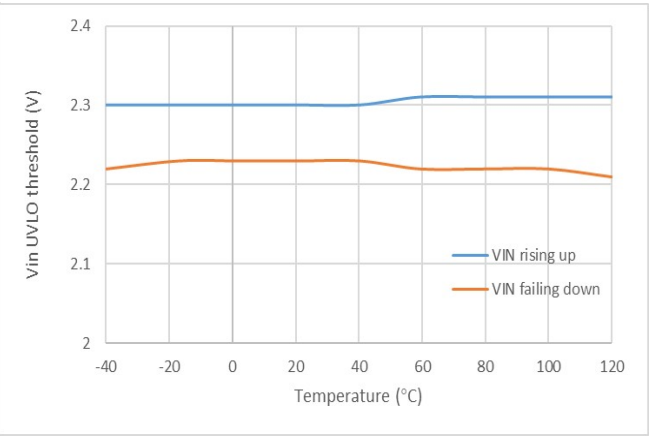
Vin shutdown current vs Ambient Temperature: (Iout=0A)



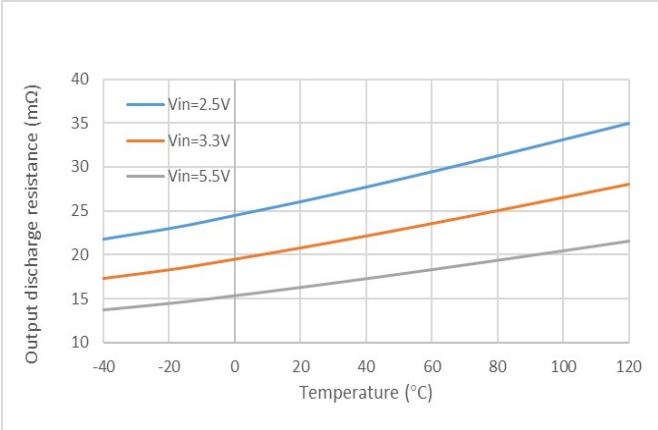
Enable input voltage threshold vs Ambient Temperature



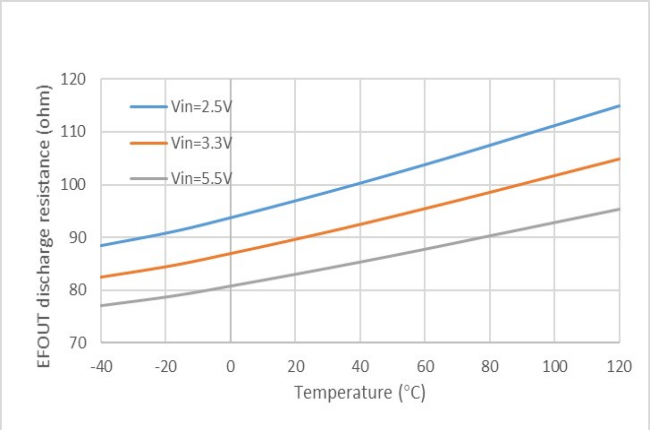
Vin UVLO threshold



Output discharge resistance



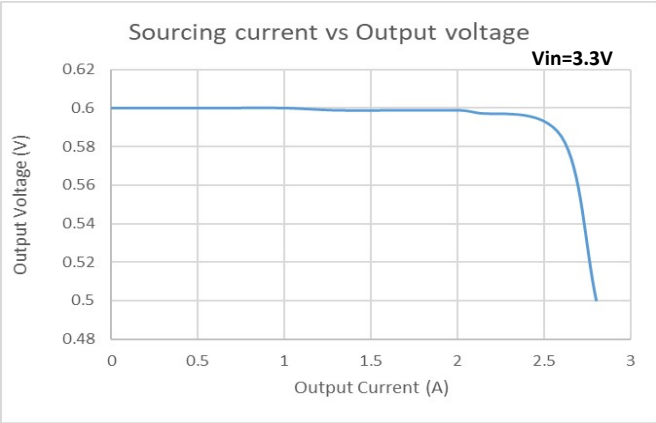
REFOUT discharge resistance



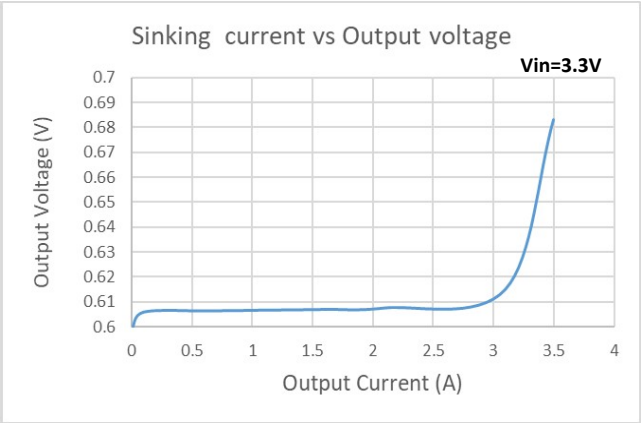
Electrical Characteristics (Continued)

C_{VLDOIN}=20µF/MLCC/X5R, C_{VIN}=4.7µF/MLCC/X7R, C_{REFOUT}=0.1µF/MLCC/X7R, C_{OUT}=20µF/MLCC/X5R, T_A=25°C, VDDQ=1.2V, VLDOIN=1.2V, unless otherwise noted.

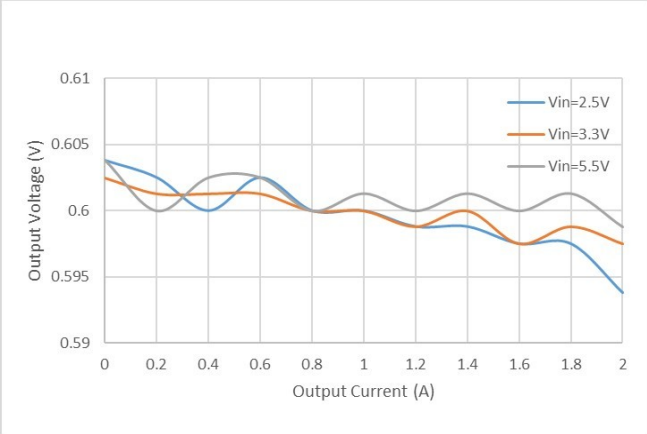
Output voltage vs Output current:Sourcing current



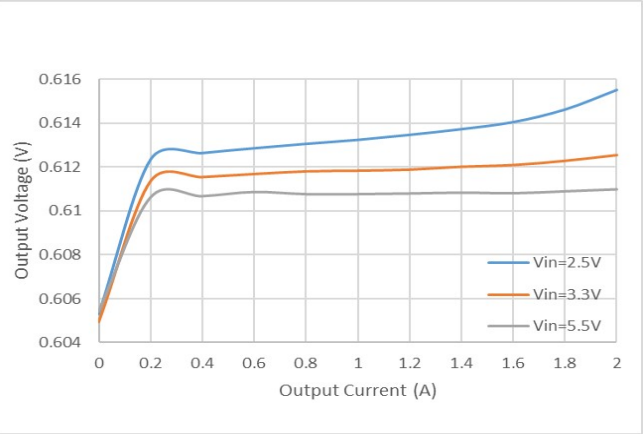
Output voltage vs Output current:Sinking current



Output voltage load regulation Iout from 0A to 2A. sourcing current



Output voltage load regulation Iout from 0A to 2A. sinking current

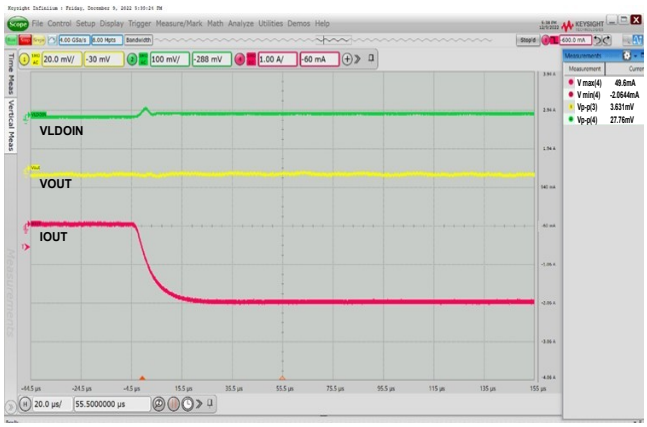


Electrical Characteristics (Continued)

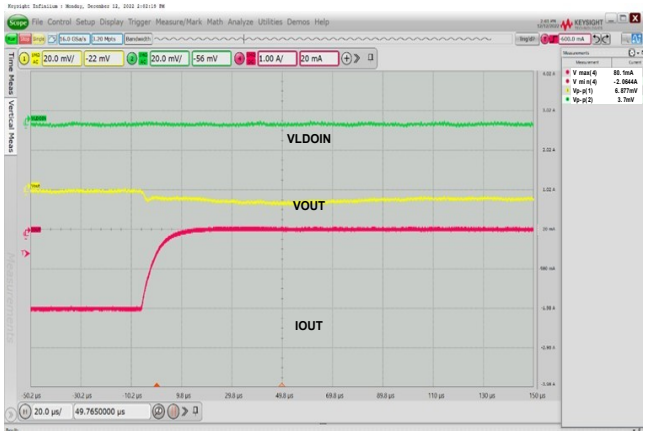
C_{VLDOIN}=20μF/MLCC/X5R, C_{VIN}=4.7μF/MLCC/X7R, C_{REFOUT}=0.1μF/MLCC/X7R, C_{OUT}=20μF/MLCC/X5R, T_A=25°C, VIN=3.3V, VDDQ=1.2V, VLDOIN=1.2V, unless otherwise noted.

Vout Load transient test : Sourcing current Iout from 0A to 2A &2A to 0A

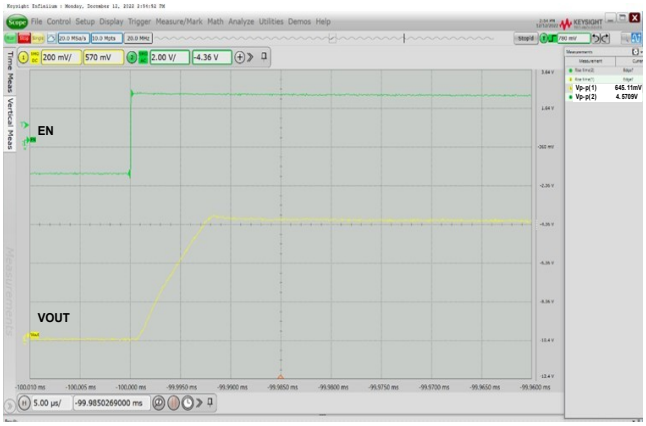
Vout Load transient test : Sinking current Iout from 0A to 2A



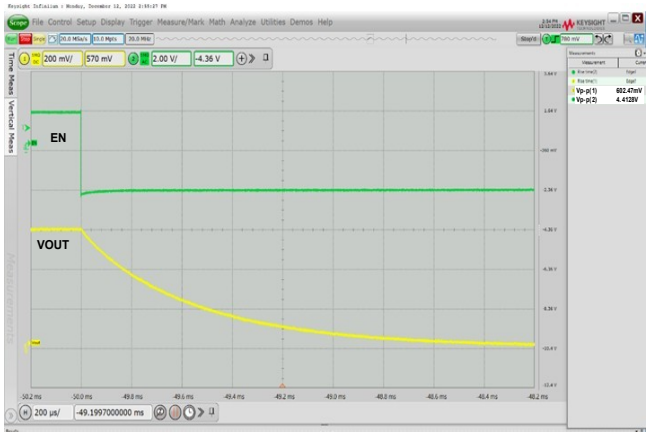
Vout Load transient test : Sinking current Iout from 2A to 0A



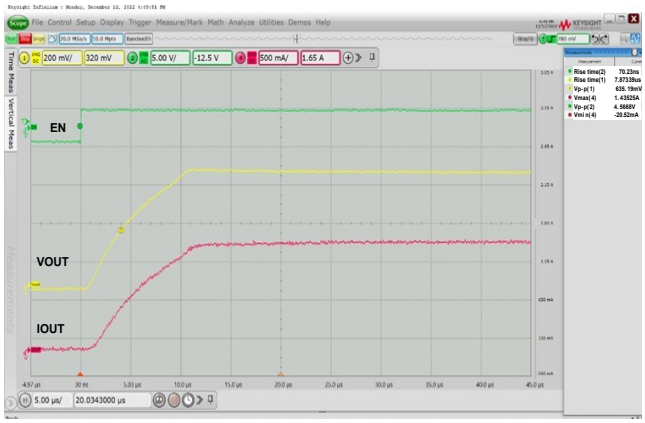
Enable power on: Iout=0A



Enable power off: Iout=0A



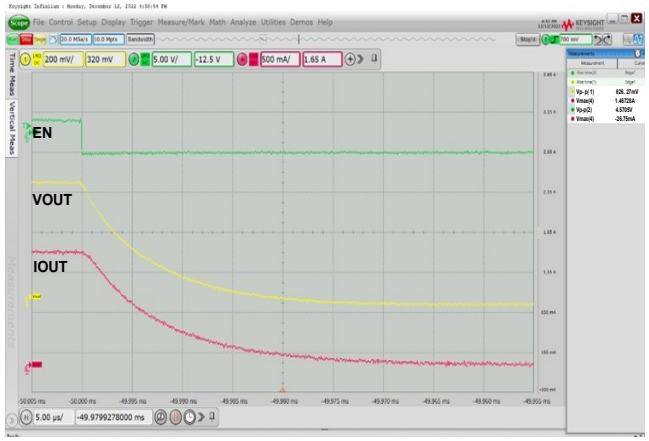
Enable power on: Iout=1.5A



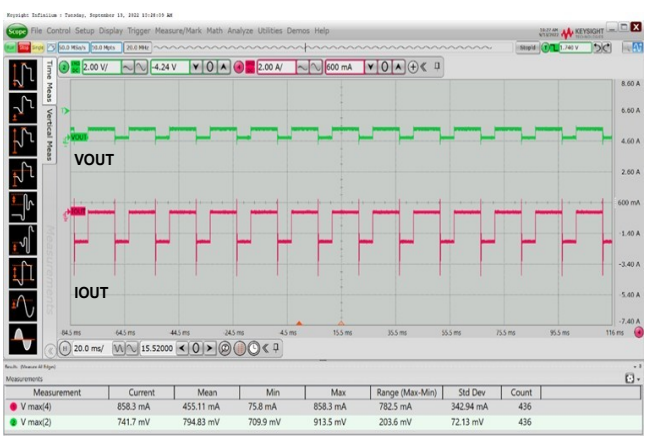
Electrical Characteristics (Continued)

C_{VLDOIN}=20μF/MLCC/X5R, C_{VIN}=4.7μF/MLCC/X7R, C_{REFOUT}=0.1μF/MLCC/X7R, C_{OUT}=20μF/MLCC/X5R, T_A=25°C, VIN=3.3V, VDDQ=1.2V, VLDOIN=1.2V, unless otherwise noted.

Enable power off:Vin=3.3V, Iout=1.5A



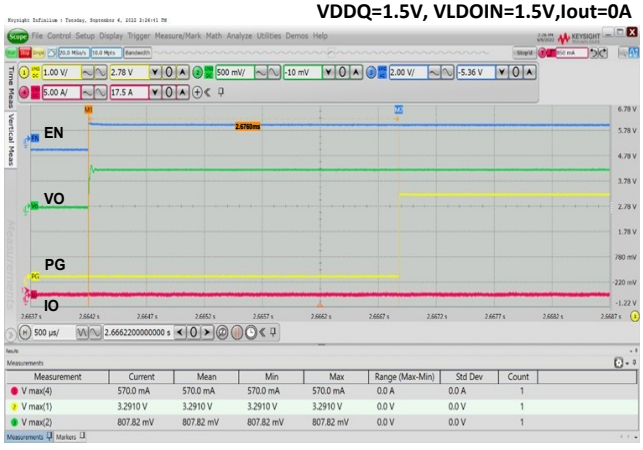
Vout shorts to ground



PGOOD bad delay

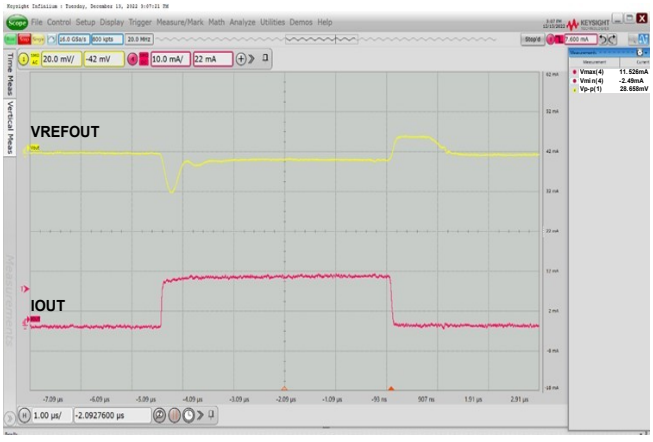
PGOOD start delay

VDDQ=1.5V, VLDOIN=1.5V,Iout=0A

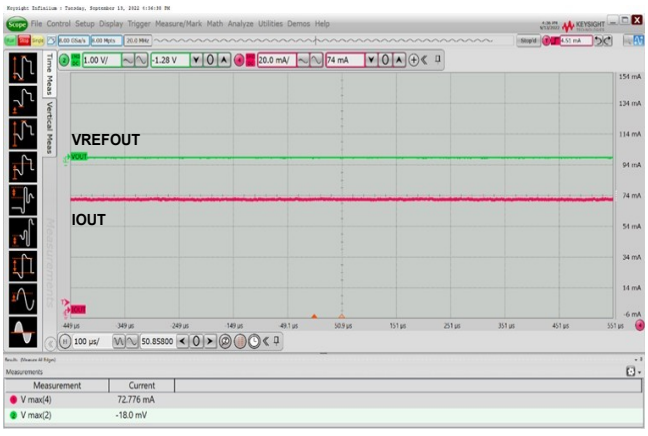


REFOUT Load transient test:Sourcing current

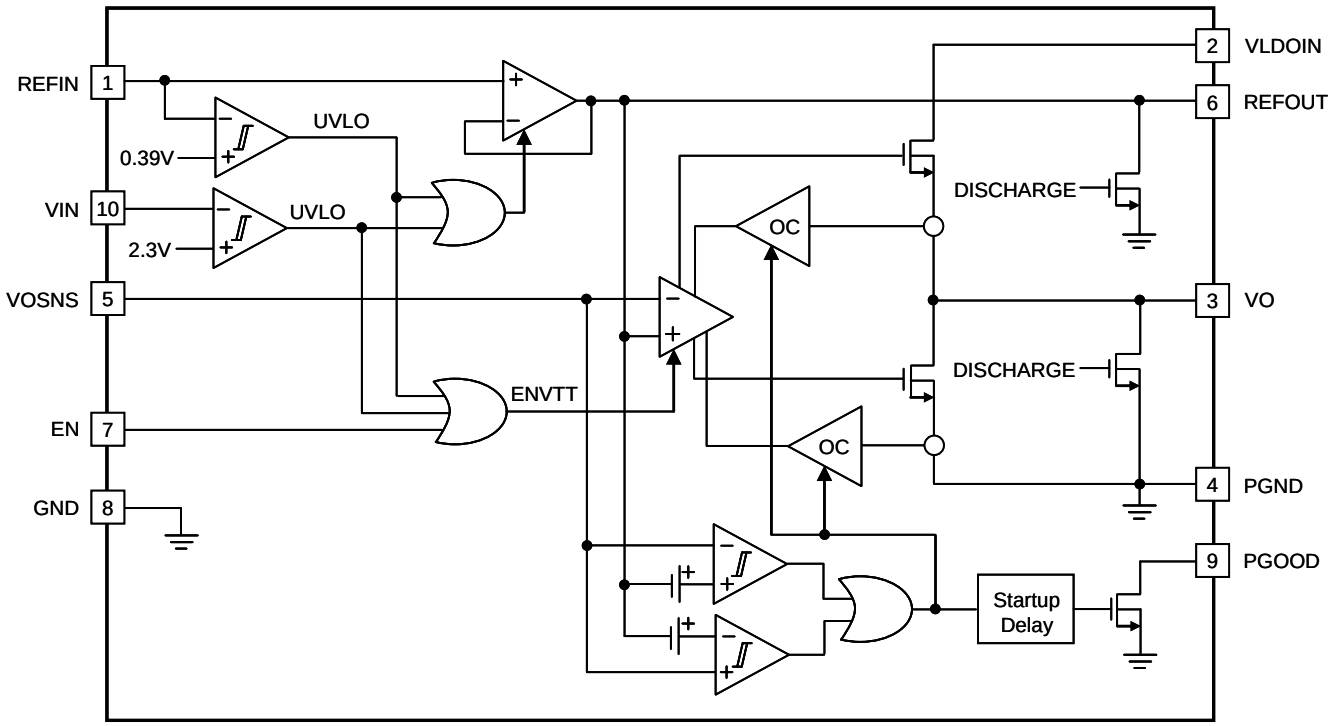
IREFOUT from 0A to 10mA &10mA to 0A



REFOUT short circuit



Block Diagram



Detailed Description

VIN, VLDOIN

VIN and VLDOIN are two independent input supply pins for the SUL60512. VIN is used to supply all the internal analog circuits. VLDOIN is only used to supply the output stage to create the regulated V_{TT}. To keep the regulation successfully, VIN should be equal to or larger than VLDOIN+1V. Using a higher VLDOIN voltage will produce a larger sourcing capability from $V_{TT.}$ But the internal power loss will also increase and then the heat increases. If the junction temperature exceeds the thermal shutdown threshold than the SUL60512 will enter the shutdown state that is the same as manual shutdown, where V_{TT} is tri-state and V_{REF} remains active.

REFIN

When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). Then, the SUL60512 generates REFOUT voltage by reference to REFIN. The REFIN voltage is supported from 0.5V to 2.5V for many types of DDR application.

REFOUT

REFOUT generates the V_{TT} reference voltage. It has 10mA source and sink ability. REFOUT becomes active when REFIN voltage rises to 0.390 V and VIN is above the UVLO threshold. In contrast, it becomes deactivated and discharges to GND through an inter-nal 10kΩ MOSFET when REFIN is less than 0.375V. REFOUT are independent of the EN pin state. For better performance, using an output bypass capacitor close this pin is more helpful for the noise. A ceramic capacitor in the range of 0.1μF to 0.01μF is recommended.

VOSNS

The VOSNS pin is the feedback sensing pin of the operation amplifier which regulates the VTT voltage. In most motherboard applications, the termination resistors will connect VTT in a long plane. If using the remote sensing pin-VOSNS to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the VOSNS pin must still be connected to VTT for correct regulation. Care should be taken when a long VOSNS trace is implemented in close proximity to the memory. Noise pickup in the VOSNS trace can cause problems with precise regulation of VTT. A small 0.1μF ceramic capacitor placed next to the VOSNS pin can help to filter any high frequency signals and preventing errors.

VO

VO is the regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the REFOUT voltage with large sinking and sourcing current capability. The maximum continuous current sourcing from VO is a function of VLDOIN. Using a higher VLDOIN will increase the source current, but it also increase the internal power dissipation and reduce the efficiency. Although the SUL60512 can deliver the larger current, care should be taken for the thermal dissipation when larger current is required. Thus, an over current function is embedded for preventing overloading and short is occurred. Also, when the temperature exceeds the junction temperature, the thermal shutdown protection is activated. That will drive the VO output into tri-state until the temperature returns below the hysteretic trigger point.

Capacitors

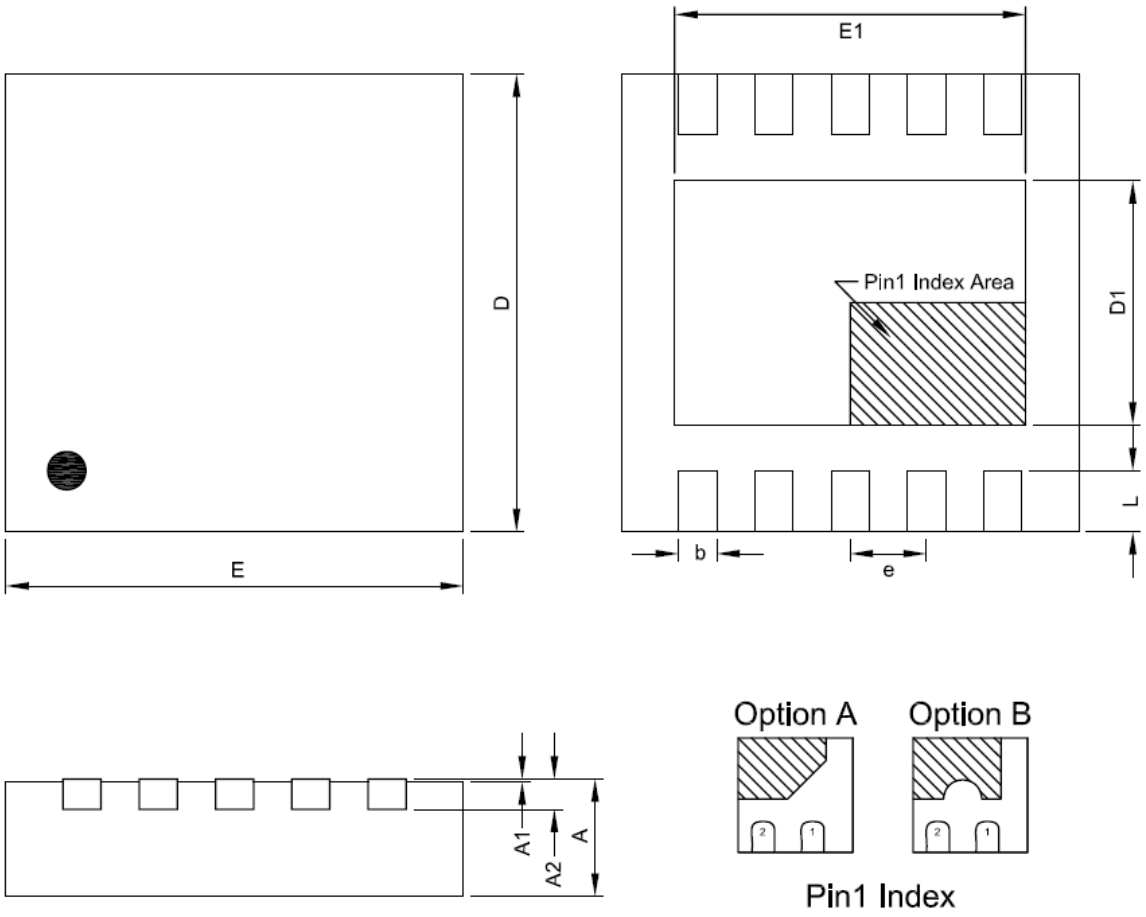
The SUL60512 does not require the capacitors for input stability, but it is recommended for improving the per-formance during large load transition to prevent the input power rail from dropping, especially for VLDOIN. The input capacitor for VLDOIN should be as close as possible. The typical recommended value is 50μF for AL electrolytic capacitors, 10μF with X5R for the ceramic capacitors. To prevent the excessive noise coupling into this device, an additional 0.1μF ceramic capacitor can be placed on the VIN power rail for the better performance.

The output capacitor of the SUL60512 is suggested to use the capacitors with low ESR. Using the capacitors with low ESR (as ceramic, OS-CON, tantalum) will have the better transition performance which is with smaller voltage drop when the peak current occurring at the transition. As a general recommendation the output capacitor should be above 20μF with the low ESR for SSTL applications with DDR-SDRAM.

S3 and Pseudo-S5 Support

The SUL60512 provides S3 and pseudo-S5 support by EN and REFIN voltage level. Both REFOUT and VO are on when EN = high. While REFIN is above 0.390V but EN = low, REFOUT is maintained but VO is turned off and discharged via an internal discharge MOSFET. When REFIN voltage is less than 0.375V and EN=low, SUL60512 enters pseudo-S5 state. Both VO and REFOUT are turned off and discharged to GND through internal MOSFETs.

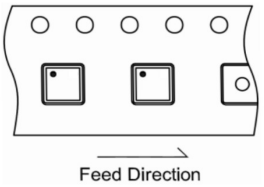
Package Dimensions: TDFN3x3-10L



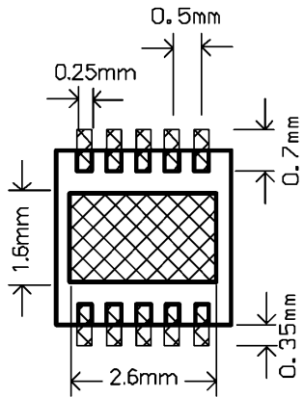
TDFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.50	1.60	1.75	0.0591	0.0630	0.0689
E1	2.20	2.60	2.70	0.0866	0.1024	0.1063
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

Taping Specification



Minimum Footprint PCB Layout Section



TDFN3X3-10L