# UMW PCF8574

8-Bit I/O Expander for I²C Bus

## 1.Description

The PCF8574 is mainly used to expand general-purpose input and output (GPIO) ports. Port data is transmitted via the standard two-line I²C protocol. The PCF8574 features 8-bit quasi-bidirectional GPIO ports (P0~P7), which can directly drive LEDs. Each quasi-bidirectional GPIO port can be used as an input or output without the use of a data-direction control signal. After power on, all GPIO ports are high.

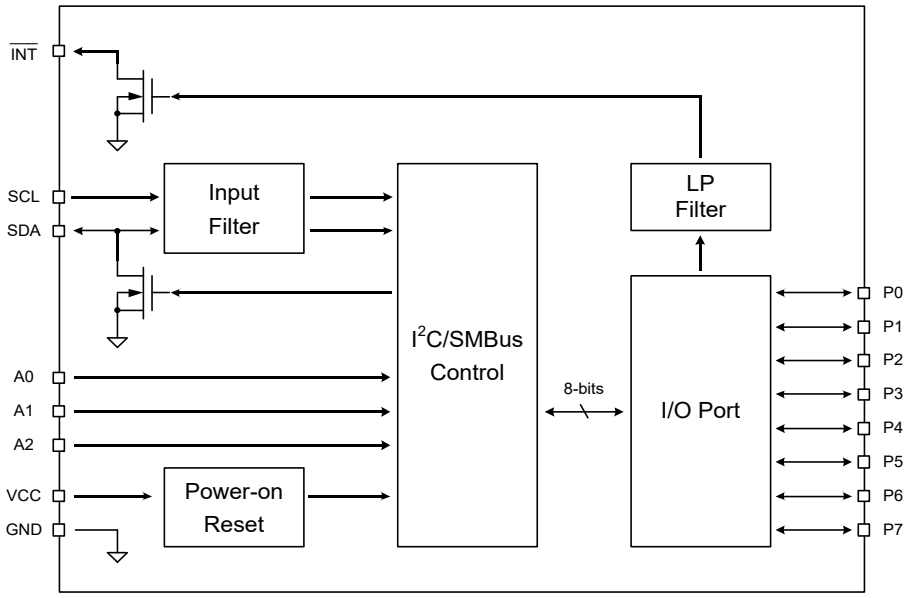
## 2.Features

- I/O interface expander controlled by I²C
- Power supply voltage: 1.6V ~ 5.5V
- Operating temperature: - 40°C ~ +85°C
- Standby power consumption: <1μA
- Can drive LED directly
- Open-drain interrupt output

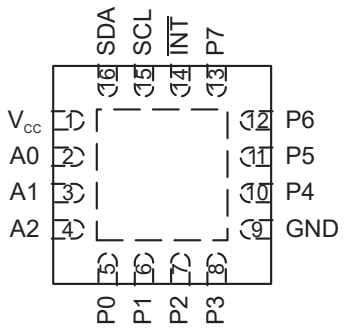
## 3.Applications

- Communication cabinet
- Servers
- Industrial automation
- Products with GPIO-Limited Processors

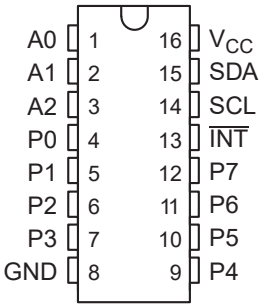
## 4.Test Circuit



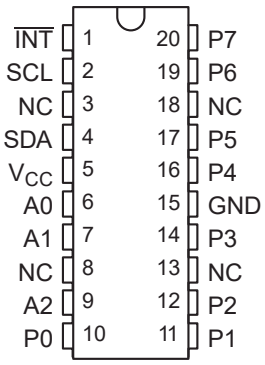
## 5.Pinning Information




QFN16




SOP16




TSSOP20

Pin Functions

| Pin | | | | Description |
|---|---|---|---|---|
| Name | QFN-16 | SOP16 | TSSOP-20 | |
| A[0:2] | 2,3,4 | 1,2,3 | 6,7,9 | Address selects. Connect to $V_{CC}$ or GND pin |
| GND | 9 | 8 | 15 | Ground |
| INT | 14 | 13 | 1 | Interrupt output. Open-drain output, requires a pull-up resistor |
| NC | - | - | 3,8,13,18 | Do not connect. |
| P[0:7] | 5,6,7,8<br>10,11,12,13 | 4,5,6,7<br>9,10,11,12 | 10,11,13,18<br>16,17,19,20 | Quasi-bidirectional GPIO port |
| SCL | 15 | 14 | 2 | Serial clock pin. Open drain output, requires a pull-up resistor |
| SDA | 16 | 15 | 4 | Serial data pin. Open drain output, requires a pull-up resistor |
| $V_{CC}$ | 1 | 16 | 5 | Supply voltage pin. It is recommended to add a 10uF decoupling capacitor |

## 6.Absolute Maximum Ratings

| Parameter | Max | Max | Units |
|---|---|---|---|
| Power Supply Voltage V+ | | 6 | V |
| Pin Voltage | -0.5 | 6 | V |
| Operating Temperature | -40 | 85 | °C |
| Junction Temperature | | 150 | °C |
| Storage Temperature | -60 | 150 | °C |

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range. Stresses beyond the range may cause permanent damage to the device.

## 7.Electrostatic Protection

| Parameter | | Symbol | Value | Units |
|---|---|---|---|---|
| Electrostatic Discharge | Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001 | $V_{ESD}$ | ±5000 | V |
| | Machine Mode (MM), per JEDEC-STD Classification | | 300 | V |

## 8.Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | V+ | 1.6 | 3.3 | 5.5 | V |
| Operating Temperature | $T_A$ | -40 | | 85 | °C |

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range.

## 9.Electrical Characteristics

Unless otherwise noted, the following data apply within the operating temperature range. (Typical operating conditions are +25°C and 3.3V)

| Parameter | Symbol | Conditions | VCC | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| I²C communication frequency | $f_{scl}$ | | 2.5~5.5 | | | 400 | KHZ |
| I²C communication frequency (high speed mode) | $f_{scl,hs}$ | | 2.5~5.5 | | | 2000 | KHZ |
| Power-on reset voltage | $V_{POR}$ | | 5 | | 1 | 1.2 | V |
| GPIO pull-up current | $I_{OH}$ | $V_O$=GND | 2.5~5.5 | 30 | 50 | 300 | μA |
| GPIO pull-up current (fully driven state) | $I_{OHT}$ | High during acknowledge $V_{OH}$=GND | 2.5 | | 1 | | mA |
| GPIO sink current | $I_{OL}$ | $V_O$=1V | 5 | 10 | 25 | | mA |
| SDA sink current | $I_{OL,SDA}$ | $V_O$=0.4V | 2.5~5.5 | 3 | | | mA |
| INT sink current | $I_{OL,INT}$ | $V_O$=0.4V | 2.5~5.5 | 3 | | | mA |
| Source current (operating mode) | $I_{work}$ | I²C communication frequency 100kHz | 5 | | 40 | 100 | μA |
| Source current (standby mode) | $I_{idle}$ | I²C does not communicate | 5 | | 1 | 10 | μA |

## 10.Static Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input SCL; input/output SDA** | | | | | | |
| LOW-level input voltage | $V_{IL}$ | | -0.5 | | $0.3V_{DD}$ | V |
| HIGH-level input voltage | $V_{IH}$ | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | V |
| **I/Os; P0 to P7** | | | | | | |
| LOW-level input voltage | $V_{IL}$ | | -0.5 | | $0.3V_{DD}$ | V |
| HIGH-level input voltage | $V_{IH}$ | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | V |
| **Interrupt INT** | | | | | | |
| LOW-level output current | $I_{OL}$ | $V_{OL}$=0.4V | 1.6 | | | mA |
| leakage current | $I_L$ | $V_I$=$V_{DD}$ or $V_{SS}$ | -1 | | 1 | μA |
| **Select inputs A0, A1, A2** | | | | | | |
| LOW-level input voltage | $V_{IL}$ | | -0.5 | | $0.3V_{DD}$ | V |
| HIGH-level input voltage | $V_{IH}$ | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | V |
| input leakage current | $I_{LI}$ | pin at $V_{DD}$ or $V_{SS}$ | -250 | | 250 | nA |

## 11.Switching Sequence

Unless otherwise specified, the following data apply within the operating temperature range with the GPIO port load capacitance <100pF. (Typical operating conditions are + 25°C and 3.3V)

| Parameter | Symbol | From | TO | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Output data valid | $t_{pv}$ | SCL | GPIO | | | 4 | μs |
| Input data setup time | $t_{su}$ | GPIO | SCL | | 0 | | μs |
| Input data hold time | $t_h$ | GPIO | SCL | | 4 | | μs |
| Interrupt valid time | $t_{iv}$ | GPIO | INT | | | 4 | μs |
| Interrupt reset delay time | $t_{ir}$ | SCL | INT | | | 4 | μs |

## 12.Detailed Description

### 12.1 Port Structure

The simplified circuit of the general purpose input/output (GPIO) is shown in Figure 1, which consists of a weak pull current path (100uA) and a strong sink current path (25mA). This structure can be used as an input or output port without any direction control signal. If used as an input, the port must be written with data 1.

When writing data 0 to the I/O port through the I²C interface, transistor Q2 is turned on, while Q1 and Q3 are turned off. At this time, the pull-down path is turned on and provides sufficient sink current to drive LED. When writing data1 to the I/O port through the I2C interface, transistor Q2 is turned off while Q1 and Q3 are turned on. Q3 is an additional auxiliary for strong current path (1mA) to provide a fast-rising edge when driving heavy loads. Transistor Q3 is turned on only during the Ack period of I2C writing sequence.

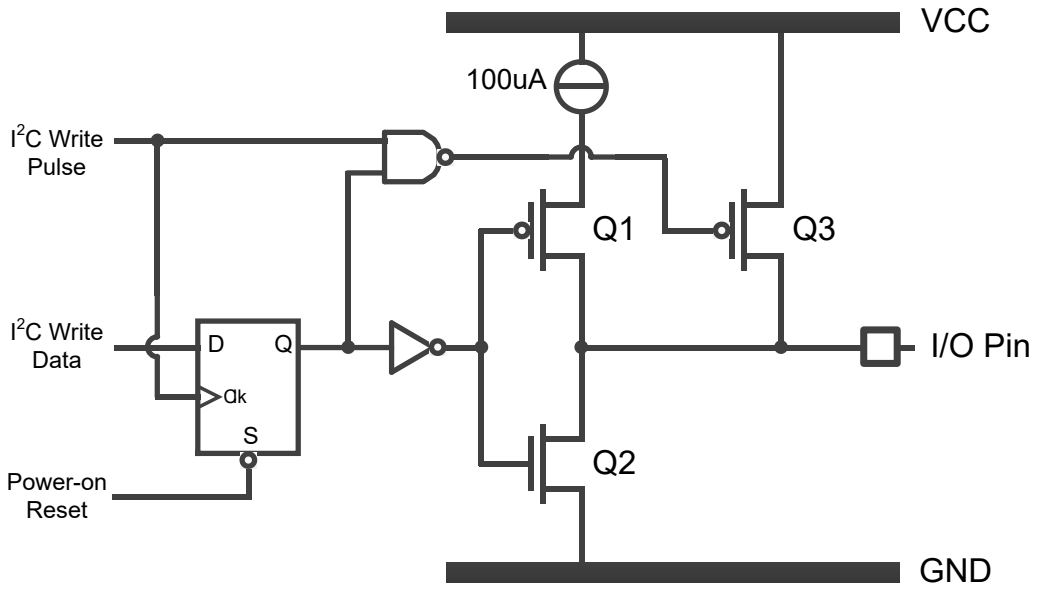



Figure 1. Simplified Circuit Diagram of General Purpose Input/Output (GPIO)

## 12.2 Serial Interface

### 12.2.1 Bus Overview

I2C/SMBus is a two-wire serial communication interface supporting multi-master and multi-slave. The device that initiates the communication is called the master, and the device controlled by the master is called the slave. The master is responsible for generating the serial clock (SCL) and controlling the bus access.

Data transfer is sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA while SCL is high is interpreted as a START or STOP conditions. Parameters for Figure 2 are defined in Table 1.

Table 1. Timing Diagram Requirements

| Symbol | Parameter | Fast Mode | | High-speed Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL operating frequency | 1 | 400 | 1 | 2000 | kHz |
| $t_{SU:STA}$ | Repeated START condition setup time | 0.6 | - | 0.26 | - | us |
| $t_{HD:STA}$ | Repeated START condition hold time | 0.6 | - | 0.26 | - | us |
| $t_{SU:STO}$ | STOP condition setup time | 0.6 | - | 0.26 | - | us |
| $t_{BUF}$ | Bus free time between STOP and START | 1.3 | - | 0.5 | - | us |
| $t_{SU:DAT}$ | Data setup time | 0.1 | - | 0.05 | - | us |
| $t_{HD:DAT}$ | Data hold time | 0 | - | 0 | - | us |
| $t_{HIG}$ | SCL clock high period | 0.6 | - | 0.26 | - | us |
| $t_{LOW}$ | SCL clock low period | 1.3 | - | 0.5 | - | us |
| $t_R$ | Clock and data rise time | - | 300 | - | 120 | ns |
| $t_F$ | Clock and data fall time | - | 300 | - | 120 | ns |

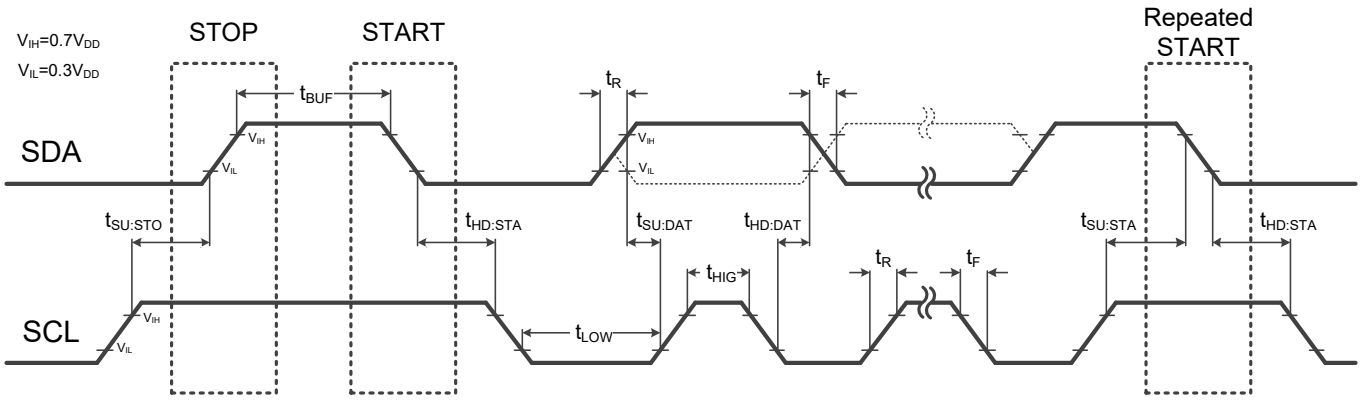



Figure 2. Two-Wire Timing Diagram

### 12.2.2 Slave Address

PCF8574 has 3 hardware address pins (A2/A1/A0), which allow users to select the slave address of the chip. The corresponding reference is shown in Table 2. The logic level of the pin must always remain unchanged during a communication process, otherwise it may cause communication failure. The address pin must be connected to VCC or GND and cannot be in a float state, otherwise it will cause communication failure and the chip will show an abnormal standby current more than 1uA.

The slave address byte consists of 7 address bits and 1 read/write flag bit. The read/write flag bit indicates the data transmission direction. 0b represents write operation; 1b represents read operation. The transmission of communication data starts from the highest bit of the byte.

Table 2. Slave Address Reference

| A2 | A1 | A0 | Slave Address |
|---|---|---|---|
| GND | GND | GND | 0x40 (write), 0x41 (read) |
| GND | GND | VCC | 0x42 (write), 0x43 (read) |
| GND | VCC | GND | 0x44 (write), 0x45 (read) |
| GND | VCC | VCC | 0x46 (write), 0x47 (read) |
| VCC | GND | GND | 0x48 (write), 0x49 (read) |
| VCC | GND | VCC | 0x4A (write), 0x4B (read) |
| VCC | VCC | GND | 0x4C (write), 0x4D (read) |
| VCC | VCC | VCC | 0x4E (write), 0x4F (read) |

### 12.2.3 Read and Write Operations

GPIO output can be achieved by writing data to PCF8574. Starting from the slave address byte with the R/$\overline{W}$ bit low, each subsequent byte represents the data to be output to the GPIO port. PCF8574 refreshes the received data byte to the GPIO port at the rising edge of SCL of the Ack bit of each data byte, and samples the GPIO port at the falling edge of SCL immediately following it to ensure that the write data does not trigger an interrupt signal. Taking the continuous writing of two bytes as an example, the specific timing is shown in Figure 3, and the shaded part represents that the slave is controlling the SDA bus.

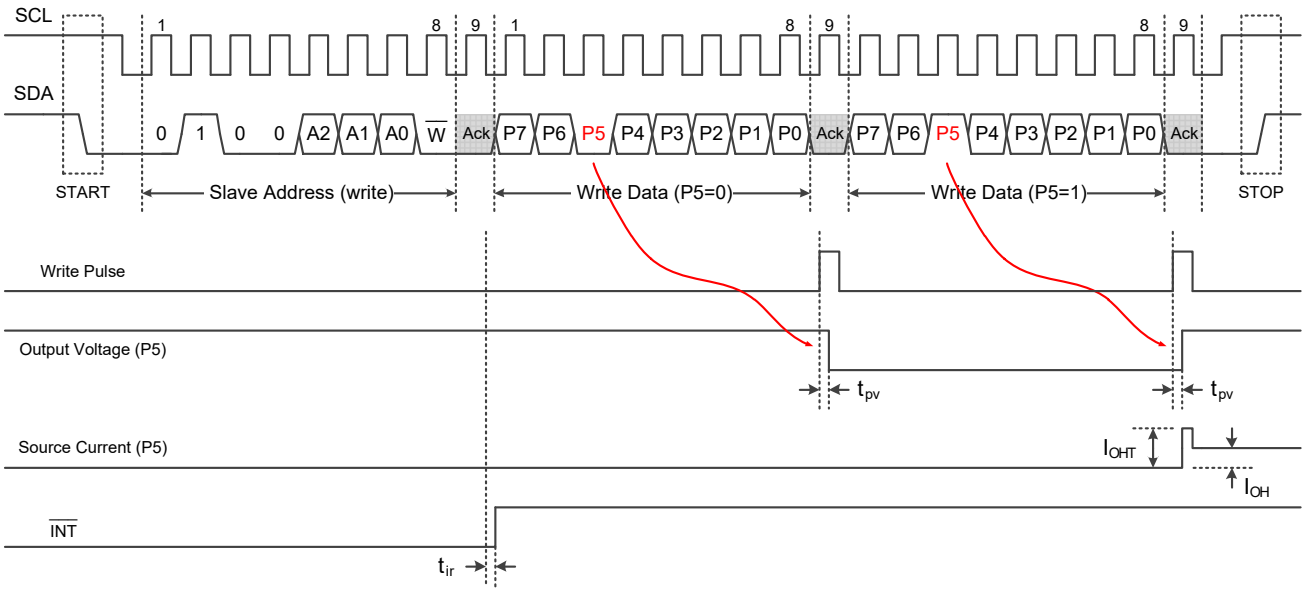



Figure 3. Timing Diagram of Write Sequence

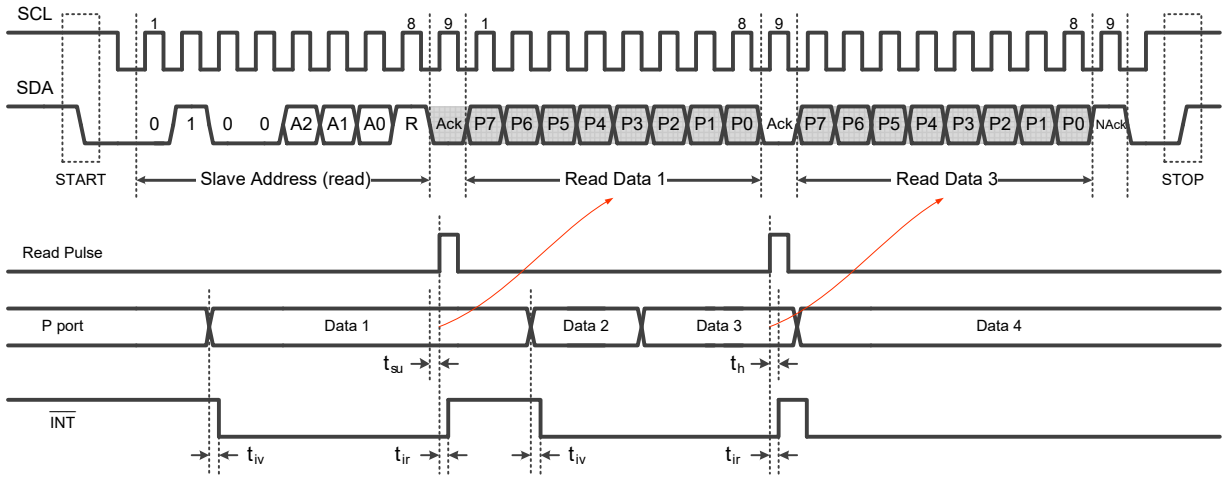



Figure 4. Timing Diagram of Read Sequence

GPIO input can be achieved by reading data from PCF8574. Starting from the slave address byte with the R/W bit high, each subsequent byte represents the data sampled from the GPIO port. PCF8574 samples the GPIO port at the rising edge of SCL of the address byte and the Ack bit of each data byte, thereby clearing the interrupt signal. However, it should be noted that when the host sends the NAck bit, PCF8574 will not sample the GPIO port, so the interrupt signal will not be cleared. Taking the continuous reading of two bytes as an example, the specific timing is shown in Figure 4, and the shaded part represents that the slave is controlling the SDA bus.

Note: When a GPIO port is used as an input port, data 1 must be written to the port first.

#### 12.2.4 High-Speed Mode

If the host sends a high-speed mode code (0000 1xxxb) after the start condition, the chip will not answer the byte, but will switch the input and output filters of the SDA and SCL pins to high-speed mode, allowing the bus to transmit data at a communication frequency of up to 2MHz. The chip will continue to operate in high-speed mode until STOP appears on the bus. Once STOP is received, the chip will switch the input and output filters back to standard mode.

## 12.3 Interrupt Output

PCF8574 provides an open-drain interrupt pin that can be directly connected to the interrupt input of a microprocessor. By sending an interrupt signal, the chip can actively notify the microprocessor if the logic level of the remote I/O pin has changed.

There are three key points to note about setting and clearing interrupt signals:

- Only external changes will cause the interrupt signal to be set, that is, writing data will not cause an interrupt;
- The interrupt signal will not be latched. If the I/O pin logic level returns to the state at the last sampling moment, the interrupt signal will be cleared immediately;
- Interrupt signal assertions that occur close to the Ack bit may be lost.

## 13.Application and Implementation (Note)

The following contents are notes and suggestions for the use of PCF8574, and GXCAS does not warrant its accuracy or completeness. Customers are responsible for determing suitability of components for their purpose, as well as validating and testing their design implementation to confirm system functionality.

## 13.1 Quick Feature Guide

Table 5. Selection Table

| Device | Type | I/O | Address | Built-in Pullup | Reset Input |
|---|---|---|---|---|---|
| GXA574 | Quasi bi-dir. | 8 | 0100 xxxb | | |
| GXA534 | Totem-pole | 8 | 0100 xxxb | | |
| GXA538 | Totem-pole | 8 | 1110 0xxb | | √ |
| GXA554 | Totem-pole | 8 | 0100 xxxb | √ | |
| GXA535 | Totem-pole | 16 | 0100 xxxb | | |
| GXA539 | Totem-pole | 16 | 1110 1xxb | | √ |
| GXA555 | Totem-pole | 16 | 0100 xxxb | √ | |

## 13.2 High Current-Drive Load Application

The I/O pins of the PCF8574 are capable of driving with a minimum perfusion current of 10mA. Additionally, it is possible to connect multiple I/O pins together through short-wiring in order to enhance the current-driven capability. As illustrated in Figure 5, individual current limiting resistors are necessary for each I/O pin and proper synchronization of switches is required to prevent any potential damage to the chip.

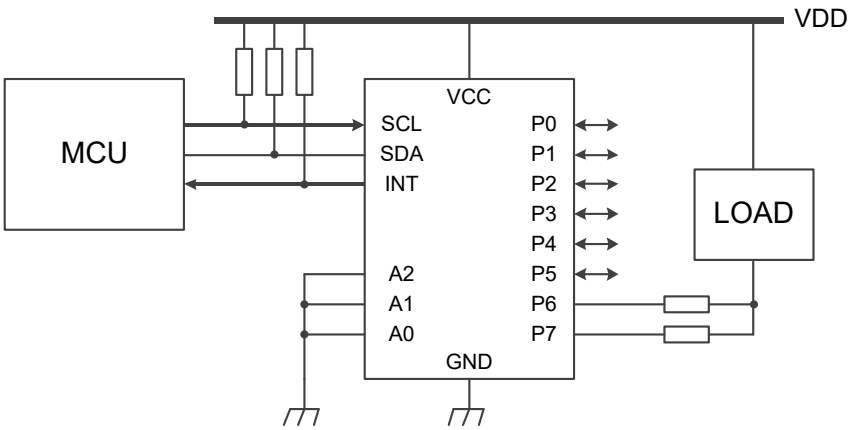
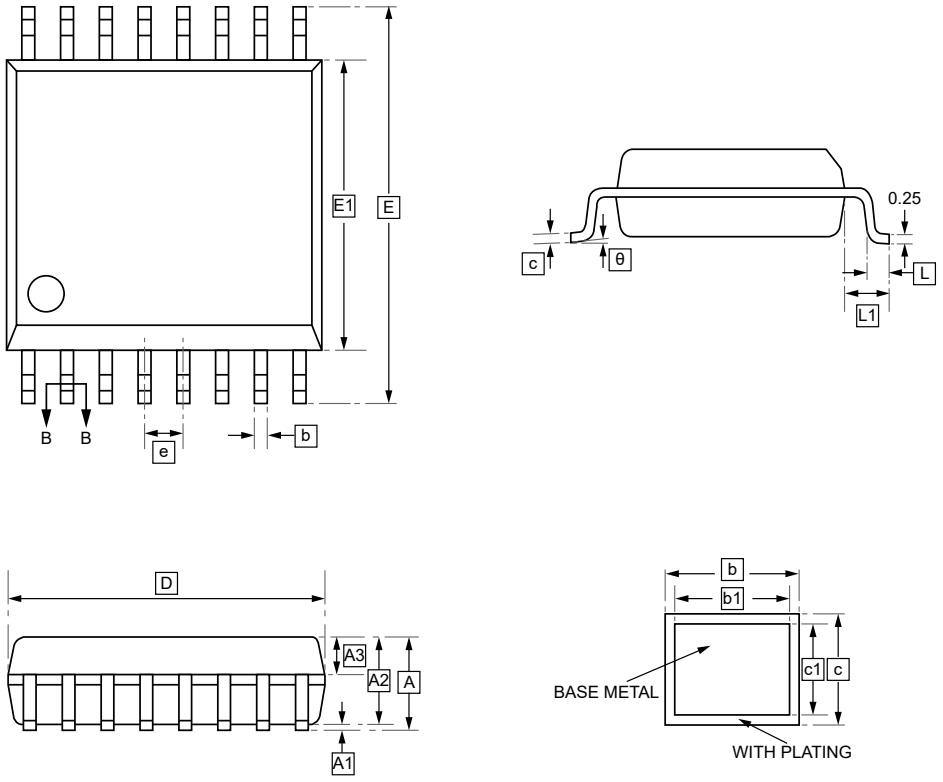



Figure 5. High Current-Drive Load Application

## 14.1 SOIC-16-300mil Package Outline Dimensions

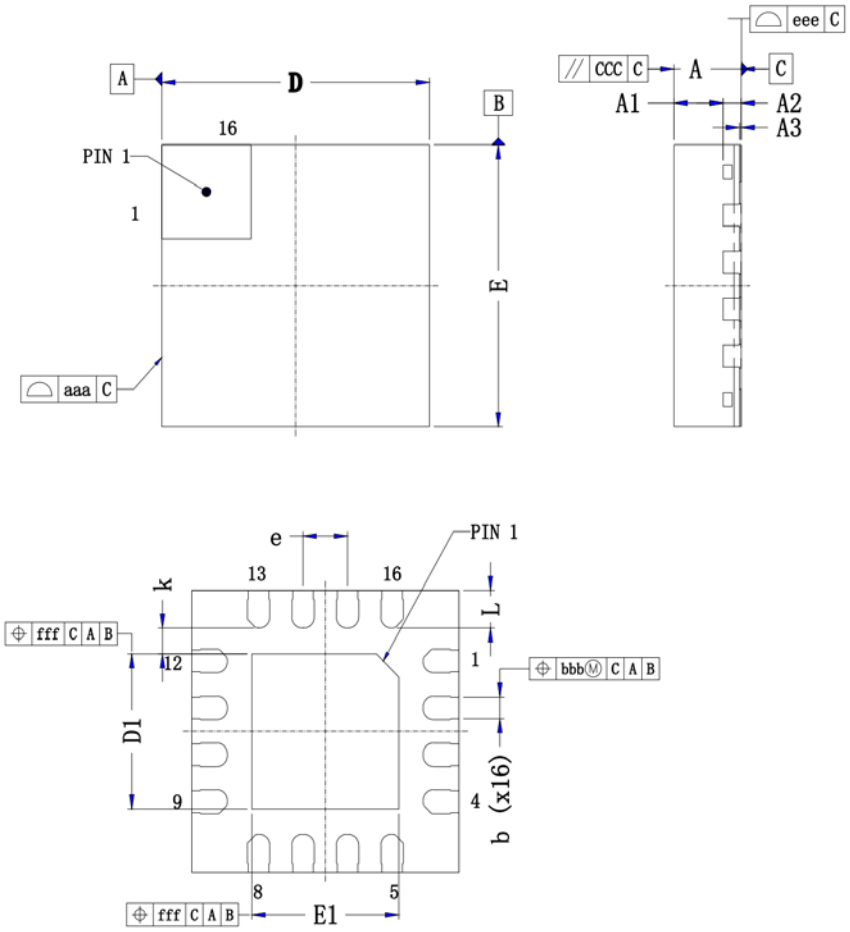



**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | A3 | b | b1 | c | c1 | D | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | - | 0.10 | 2.25 | 0.97 | 0.35 | 0.34 | 0.25 | 0.24 | 10.20 | 10.10 | 7.40 | 1.27 |
| **Max** | 2.65 | 0.30 | 2.35 | 1.07 | 0.43 | 0.40 | 0.29 | 0.26 | 10.40 | 10.50 | 7.60 | BSC |

| Symbol | L | L1 | θ |
|---|---|---|---|
| **Min** | 0.55 | 1.40 | 0° |
| **Max** | 0.85 | REF | 8° |

## 14.2 WQFN-16-EP(3x3) Package Outline Dimensions

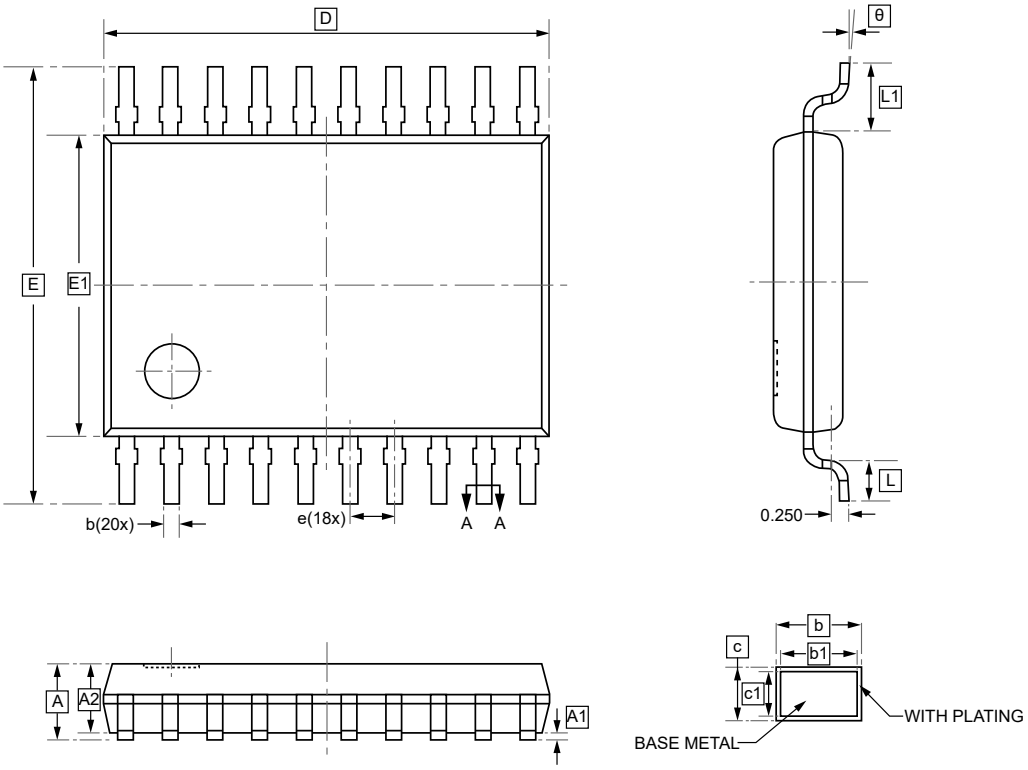



**DIMENSIONS (mm are the original dimensions)**

| Symbol | D | E | D1 | E1 | A | A1 | A2 | A3 | b | L | e | k |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 3.0 | 3.0 | 1.55 | 1.55 | 0.7 | 0.55 | 0.203 | 0 | 0.20 | 0.3 | 0.5 | 0.2 |
| Max | BSC | BSC | 1.75 | 1.75 | 0.8 | | REF | 0.05 | 0.30 | 0.5 | BSC | - |

| Symbol | aaa | bbb | ccc | eee | fff |
|---|---|---|---|---|---|
| Min | 0.1 | 0.07 | 0.1 | 0.08 | 0.1 |
| Max | | | | | |

## 14.3 TSSOP-20 Package Outline Dimensions

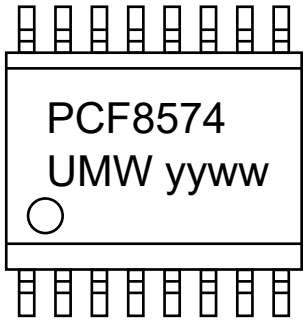



**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | - | 0.05 | 0.90 | 0.20 | 0.19 | 0.13 | 0.120 | 6.40 | 6.20 | 4.30 | 0.65 | 0.85 |
| Max | 1.20 | 0.15 | 1.05 | 0.28 | 0.25 | 0.17 | 0.14 | 6.60 | 6.60 | 4.50 | BSC | 1.15 |

| Symbol | L | θ |
|---|---|---|
| Min | 0.45 | 0° |
| Max | 0.75 | 8° |

## 15.Ordering Information




yy: Year Code
ww: Week Code

| Order Code | Marking | Package | Base QTY | Delivery Mode |
|---|---|---|---|---|
| UMW PCF8574DWR | PCF8574 | SOIC-16-300mil | 2000 | Tape and reel |
| UMW PCF8574RGTR | 8574Q | WQFN-16-EP(3x3) | 3000 | Tape and reel |
| UMW PCF8574PW | PCF8574 | TSSOP-20 | 3000 | Tape and reel |

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