

SUL6113C 5.5V 3A Low Dropout Regulator

GENERAL DESCRIPTION

The SUL6113C device is a CMOS-based very low dropout voltage regulator, offering 3A with NMOS pass transistor and a separate bias supply voltage (VBIAS).

The SUL6113C provides very stable, accurate output voltage with high ripple rejection and excellent full load transient performance.

The SUL6113C device consist of an accurate 0.8V internal voltage-reference, an error amplifier, an under-voltage lock-out (UVLO) block, an output current limit circuit and a thermal-shutdown circuit.

The SUL6113C device can set the output voltage through external resistor divider with FB pin. With the SS pin, user can fulfill the soft-start function through the external capacitor. A Power Good pin (PG) is also available.

The SUL6113C device is available in DFN3x3-10 package.

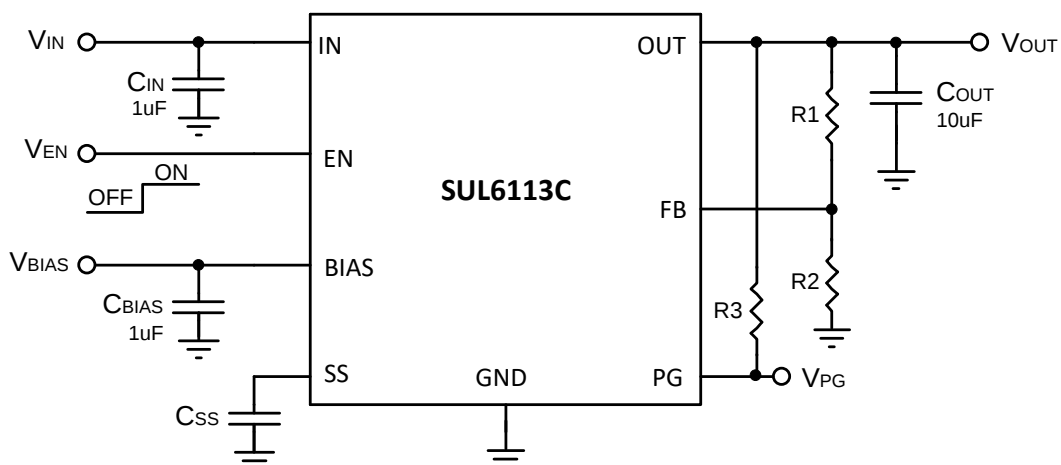
FEATURES

- Wide Input Voltage Range: 0.8V to 5.5V
- Wide BIAS Voltage Range: 2.2V to 5.5V
- Maximum: Output Current:3A
- Adjustable Output Voltage: 0.8V to 3.6V
- Ultra Low Dropout Voltage: 95mV at 3A
- Open Drain Power Good (PG) Output
- Excellent Transient Response
- Built-in Soft-start Function
- Built-in Current Limit and Thermal Shutdown Protection
- Operating Temperature Range: -40 to 85°C

APPLICATIONS

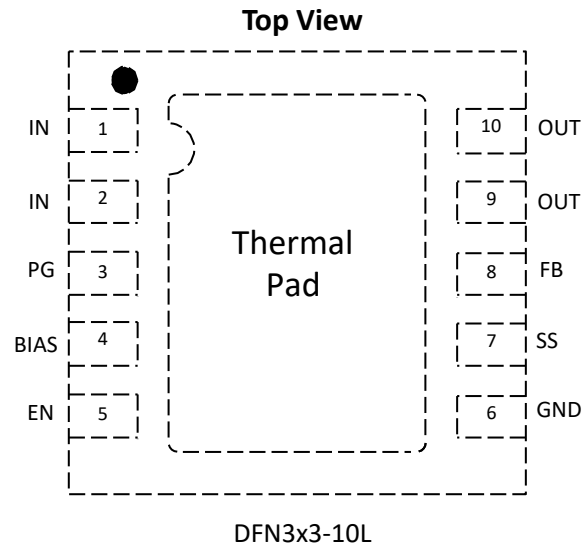
- Notebook PC Applications
- Motherboard Applications

TYPICAL APPLICATION CIRCUIT



Note: $V_{OUT} = 0.8 \times (1 + R1/R2)$, R3 should be from 10KΩ to 1MΩ.

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1, 2	IN	Unregulated input voltage pin.
3	PG	Power-Good pin is an open-drain, active-high output that indicates the status of V_{OUT} . A pull-up resistor from 10k Ω to 1M Ω should be connected to a supply and the PG pin can be left floating alternatively.
4	BIAS	Input voltage for internal control circuits.
5	EN	Enable pin. Active high and this pin must not be left floating.
6	GND	Ground pin.
7	SS	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 200 μ s.
8	FB	Connecting to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
9, 10	OUT	Regulated output voltage.
Thermal Pad		Should be soldered to the ground plane for increasing thermal performance.

ORDERING INFORMATION

Part Number	Package	Temperature Range	Tape&Reel
SUL6113C	DFN3X3-10L	-40 to +85 °C	3000pcs

Note: The SUL6113C devices are Pb-free and RoHS compliant.

ABSOLUTE MAXIMUM RATINGS^(Note 1)

Symbol	Parameter	Rating	Unit
V _{IN}	Input Voltage Range	-0.3 to +6	V
V _{BIAS}	Input Voltage Range	-0.3 to +6	V
V _{EN}	Enable Voltage Range	-0.3 to +6	V
V _{PG}	Power-Good Pin Voltage Range	-0.3 to +6	V
I _{PG}	PG Sink Current	0 to +1.5	mA
V _{SS}	SS Pin Voltage Range	-0.3 to +6	V
V _{FB}	Feedback Pin Voltage Range	-0.3 to +6	V
V _{OUT}	Output Voltage Range	-0.3 to (V _{IN} + 0.3) ≤ 6	V
P _D	Continuous Total Power Dissipation	2.5	W
T _J	Maximum Junction Temperature	+150	°C
T _{STG}	Storage Junction Temperature Range	-65 to +150	°C

Note (1): Exceeding these limits might damage the device. Exposure to absolute maximum rating conditions may affect device reliability.

RECOMMENDED OPERATING RANGE

Symbol	Parameter	Rating	Unit
V _{IN}	Input voltage range	V _{OUT} + V _{DO} to 5.5	V
V _{BIAS}	Bias pin voltage range	2.2 to 5.5	V
T _A	Operating Ambient Temperature	-40 to +85	°C

ELECTRICAL CHARACTERISTICS

$V_{EN}=1.1V$, $V_{IN}=V_{OUT}+0.3V$, $V_{BIAS}=5.0V$, $C_{BIAS}=C_{IN}=1\mu F$, $C_{OUT}=10\mu F$, $I_{OUT}=50mA$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range	$V_{IN}^{(1)}$		$V_{OUT} + V_{DO}$		5.5	V
V_{BIAS} Voltage Range	V_{BIAS}		2.2		5.5	V
Under-voltage Lock-out	V_{UVLO}	V_{BIAS} Rising	1.2	1.6	1.9	V
		Hysteresis		0.2		
Internal Reference	V_{REF}	$T_A=+25^{\circ}C$		0.8		V
Output Voltage Range	V_{OUT}	$V_{IN}=5V, I_{OU}=1.5A, V_{BIAS}=5V$	V_{REF}		3.6	V
Output Accuracy		$2.97V \leq V_{BIAS} \leq 5.25V$, $V_{OUT}+1.62V \leq V_{BIAS}$, $50mA \leq I_{OUT} \leq 3.0A$	-1.0		+1.0	%
Line Regulation	Reg_{LINE}	$V_{OUT(NOM)}+0.3 \leq V_{IN} \leq 5.5V$		0.01		%/V
Load Regulation	Reg_{LOAD}	$0mA \leq I_{OUT} \leq 50mA$		0.005		%/mA
		$50mA \leq I_{OUT} \leq 3.0A$		0.03		%/A
V_{IN} Dropout Voltage	$V_{DROP}^{(2)}$	$I_{OUT}=3.0A$, $V_{BIAS}-V_{OUT(NOM)} \geq 1.62V$		95	160	mV
V_{BIAS} Dropout Voltage		$I_{OUT}=3.0A$, $V_{IN}=V_{OUT}+0.3V$		1.12	1.5	V
Current Limit	I_{LIM}	$V_{OUT}=80\% \times V_{OUT(NOM)}$	3.8	4.6	7	A
V_{BIAS} Current	I_{BIAS}	$0mA \leq I_{OUT} \leq 3.0A$		1.3	2	mA
V_{BIAS} Shutdown Supply Current	I_{SHDN}	$V_{EN}=0V$		0.3	2	μA
V_{IN} to V_{OUT} Ripple rejection	PSRR	1kHz, $I_{OUT}=1.5A$, $V_{IN}=1.5V, V_{OUT}=1.2V$		75		dB
V_{BIAS} to V_{OUT} Ripple rejection		10kHz, $I_{OUT}=1.5A$, $V_{IN}=1.5V, V_{OUT}=1.2V$		78		dB
Output Noise Voltage	$e_N^{(3)}$	100 Hz to 100 kHz, $I_{OUT}=3A, C_{SS}=1.0nF$		$18 \times V_{OUT}$		μV_{rms}
% V_{OUT} Droop During Load Transient	$V_{TRLD}^{(3)}$	$I_{OUT}=50mA$ to $3.0A$ at $1A/\mu s$, $C_{OUT}=10\mu F$, $V_{OUT}=1.2V$		± 2		% V_{OUT}
Minimum Startup Time	t_{ON}	$I_{OUT}=1.5A, C_{SS}=open$		200		μs
Soft-start Charging Current	I_{SS}	$V_{SS}=0.4V$		0.45		μA
Enable Input High Level	V_{ENH}		1.1		5.5	V
Enable Input Low Level	V_{ENL}		0		0.4	V
Enable Pin Hysteresis	$V_{EN,HYS}$			100		mV
Enable Pin Deglitch Time	$t_{EN,DG}$			20		μs

ELECTRICAL CHARACTERISTICS (Continued)

$V_{EN}=1.1V, V_{IN}=V_{OUT}+0.3V, V_{BIAS}=5.0V, C_{BIAS}=C_{IN}=1\mu F, C_{OUT}=10\mu F, I_{OUT}=50mA, T_A=-40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Enable Pin Current	I_{EN}	$V_{EN}=5V$		0.3	1	μA
PG Threshold	V_{TH}	V_{OUT} decreasing	86.5	90	93.5	% V_{OUT}
PG Hysteresis	V_{HYS}			3		% V_{OUT}
PG Output Low Voltage	V_{PGL}	$I_{PG}=1mA$ (sinking), $V_{OUT}<V_{TH}$			0.3	V
PG Leakage Current	$I_{PG,LKG}$	$V_{PG}=5V, V_{OUT}>V_{TH}$		0.03	1	μA
Thermal Shutdown Temperature	T_{TSD}			+155		$^{\circ}C$
Thermal Shutdown Released Temperature	T_{TSR}			+125		$^{\circ}C$

Note (1): The maximum input voltage should take into account the maximum power consumption ($P_{D(MAX)}$). The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 2500mW.

$$V_{IN(MAX)} = 2500mW / I_{OUT} + V_{OUT}$$

For example:

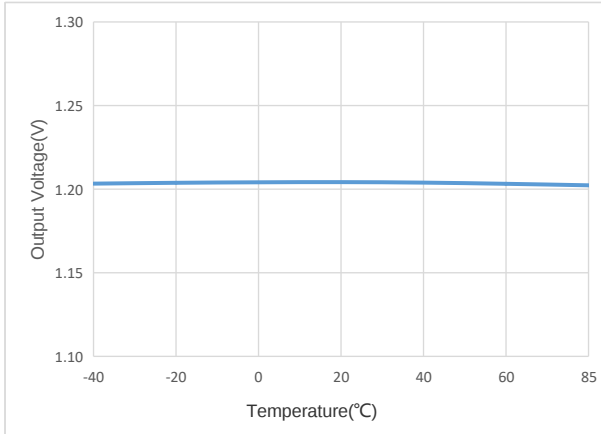
If $V_{OUT}=1.2V$, $I_{OUT}=2500mA$, The maximum input voltage is $V_{IN(MAX)}=2500mW / 2500mA + 1.2=2.2V$

Note (2): V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROPMAX}$ with output current.

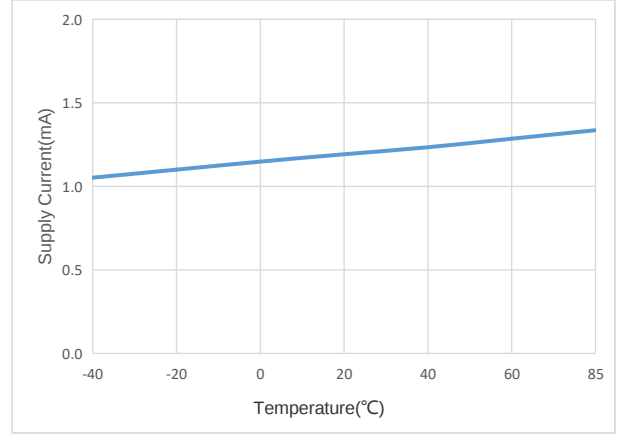
Note (3): Guaranteed by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

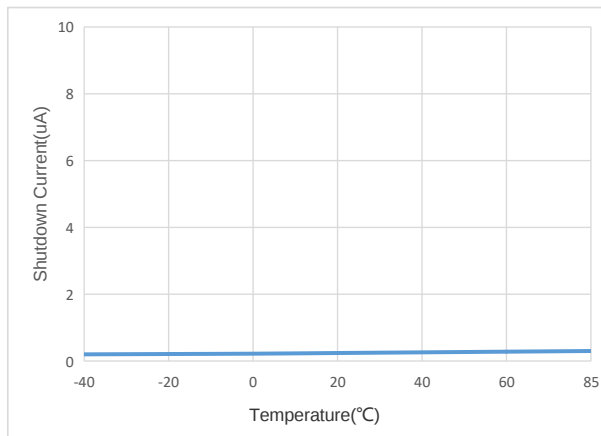
($V_{OUT}=1.2V$, $V_{IN}=1.5V$, $V_{BIAS}=5.0V$, $C_{IN}=C_{BIAS}=1\mu F$, $C_{OUT}=10\mu F$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$)



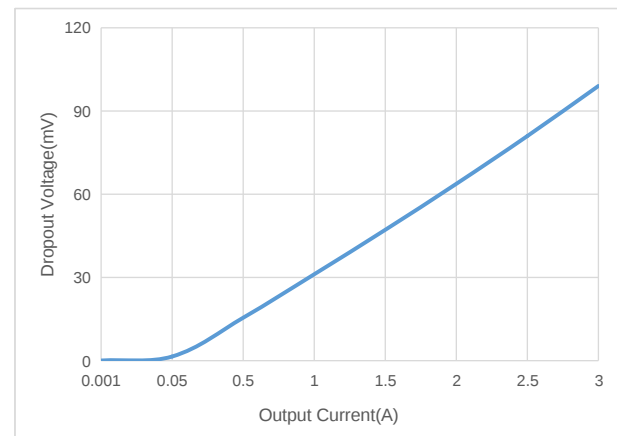
Output Voltage VS Temperature



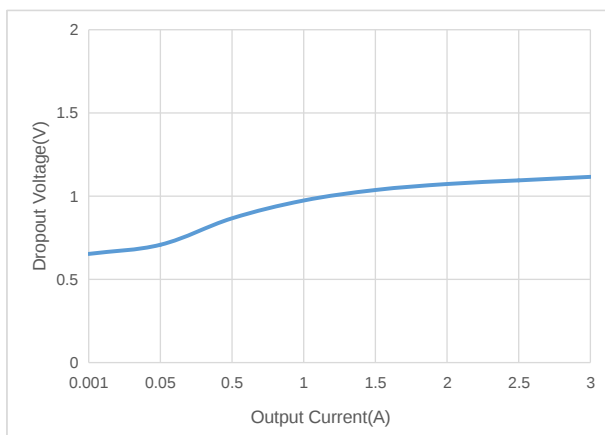
Supply Current VS Temperature



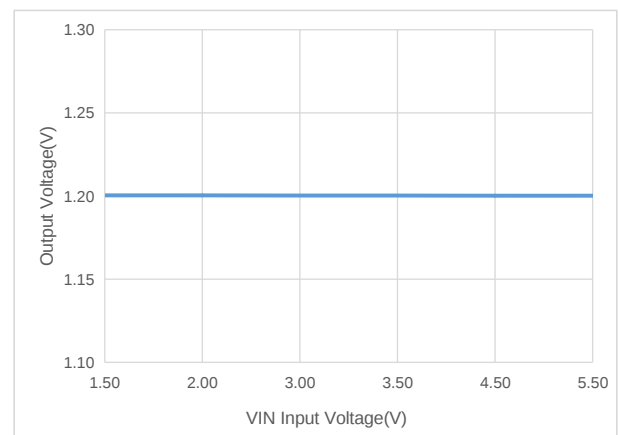
Shutdown Current VS Temperature



VIN Dropout Voltage VS Output Current



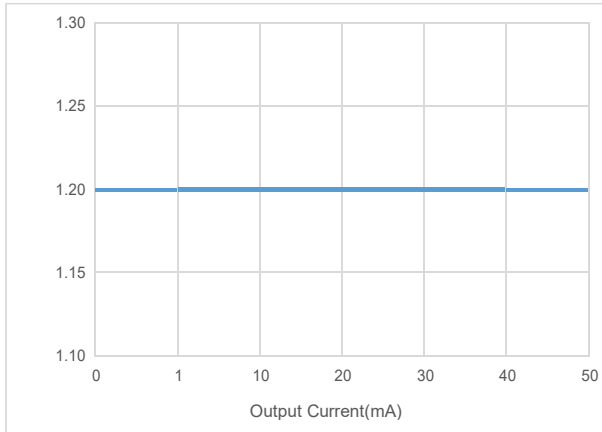
VBIAS Dropout Voltage VS Output Current



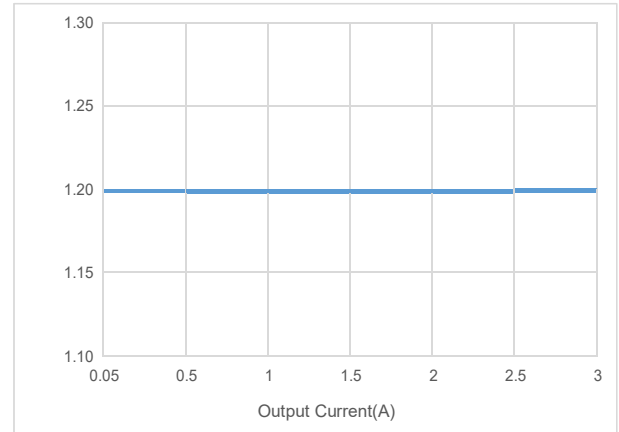
Output Voltage VS VIN Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

($V_{OUT}=1.2V$, $V_{IN}=1.5V$, $V_{BIAS}=5.0V$, $C_{IN}=C_{BIAS}=1\mu F$, $C_{OUT}=10\mu F$, $T_A=-40^{\circ}C$ to $+85^{\circ}C$)



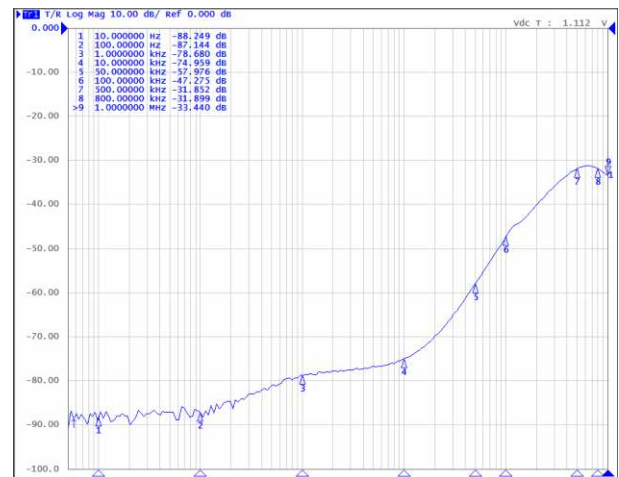
Output Voltage VS Output Current



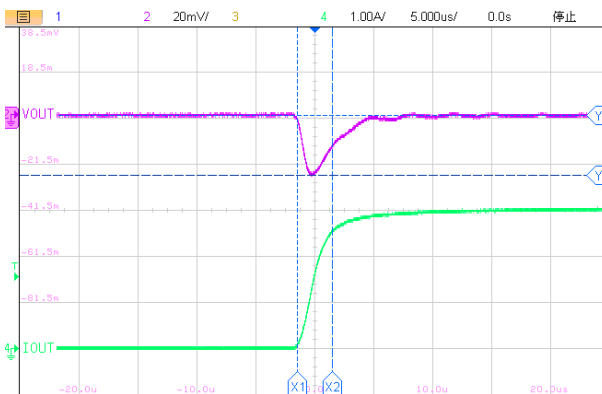
Output Voltage VS Output Current



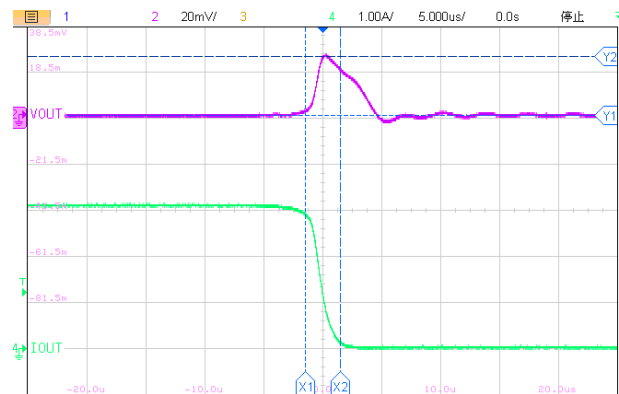
VIN PSRR



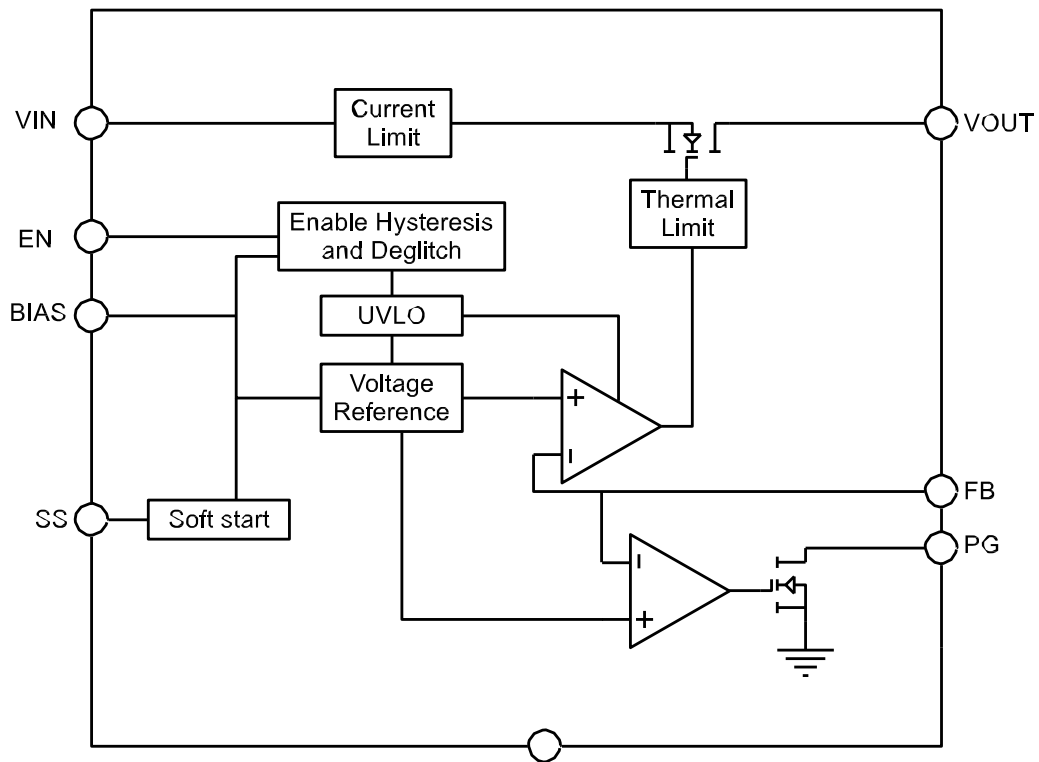
VBIAS PSRR



Load Transient(50mA~3A 1A/us)



Load Transient(3A~50mA 1A/us)

BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The SUL6113C dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the internal control circuit is powered by the BIAS voltage.

The use of an NMOS pass transistor offers several advantages in applications. Comparing to PMOS topology devices, the output capacitor has reduced impact on loop stability. The dropout voltage between V_{IN} and V_{OUT} can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The SUL6113C offers programmable smooth monotonic start-up. The controlled voltage rising limits the inrush current. The soft-start time is programmable by external C_{SS} capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter. An Open Drain Power Good (PG) output is available for V_{OUT} monitoring. When V_{OUT} exceeds the PG threshold, the PG pin goes into high-impedance state. When is below this threshold, the PG pin is set to low-impedance state.

The SUL6113C is an adjustable linear regulator. As shown in application circuit, the required output voltage can be adjusted by two external resistors with FB pin.

Dropout Voltage

There are two Dropout voltages specified.

Firstly, the V_{IN} Dropout voltage is the voltage difference between V_{IN} and V_{OUT} when V_{OUT} starts to decrease by 2%. V_{BIAS} is set to high enough, referring to the specific value in the Electrical Characteristics table.

Secondly, the V_{BIAS} dropout voltage is the voltage difference between V_{BIAS} and V_{OUT} when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease by 2%.

Input and Output Capacitors

The device is designed to be stable for all available types and values of output capacitors $\geq 2.2\mu F$. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supply impedance is available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as an example) the recommended C_{IN} and C_{BIAS} value is $1\mu F$ or greater.

Ceramic or other low ESR capacitors are recommended. For the best performance all capacitors should be connected to the SUL6113C respective pins directly in the device PCB copper layer, not through via having not negligible impedance.

Enable Operation

The SUL6113C is turned on by setting the enable pin to High. The threshold limits are covered in the electrical characteristics table in this datasheet. When the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS} .

Output Noise

When the SUL6113C device reaches the end of the Soft-Start cycle, the Soft Start capacitor will be switched to be a noise filtering capacitor.

Output Voltage Adjust

The output voltage can be adjusted from 0.8 V to 3.6 V using resistors divider between the output and the FB input. The output voltage can be calculated by:

$$V_{OUT}=0.8 \times (1+R1/R2)$$

For example: choose $R_1=2.49k\Omega$, $R_2=4.99k\Omega$, $V_{OUT}=1.2V$.

Programmable Soft-Start

The Soft-Start ramp time depends on the Soft Start charging current I_{SS} , Soft-Start capacitor value C_{SS} and internal reference voltage V_{REF} .

The Soft-Start time can be calculated by:

$$t_{ss} = C_{SS} \times (V_{REF} / I_{SS}) [s,F,V,A]$$

or practically by:

$$t_{ss} = C_{SS} \times 0.8V / 0.45\mu A = C_{SS} \times 1.78$$

Where t_{ss} is Soft-Start time in ms. C_{SS} is Soft-Start capacitor value in nF. For example:

$$t_{ss} \text{ is } 10ms \text{ when } C_{SS} \text{ is } 5.6nF.$$

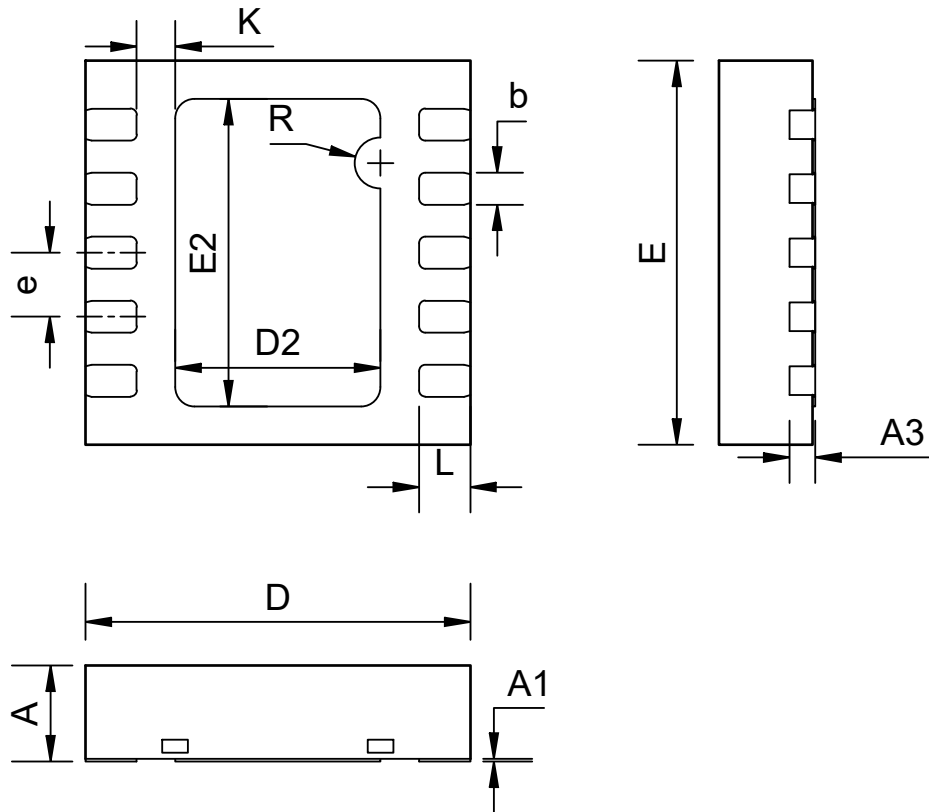
The maximal recommended value of C_{SS} capacitor is 15nF. For higher C_{SS} values the capacitor full discharging before new Soft-Start cycle is not guaranteed.

Current Limitation

When output current of V_{OUT} pin is higher than current limit threshold or the V_{OUT} pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +125°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

PACKAGE DIMENSIONS: DFN3x3-10L


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.55	1.65	1.75
E2	2.30	2.40	2.50
e	0.40	0.50	0.60
K	0.175	0.275	0.375
L	0.35	0.40	0.45
R	0.20REF		