CMOS Programmable Timer High Voltage Types (20V Rating)

The HT4541B programmable timer consists of a 16–stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power–on reset circuit, and output control logic.

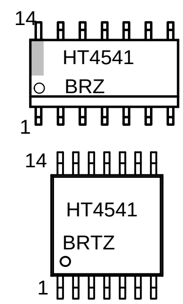
Timing is initialized by turning on power, whereupon the power–on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16–stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Built–in Low Power RC Oscillator (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- $Q/\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V_{DD})
  = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = V_{SS})

SOP14 R SUFFIX HT4541BRZ

TSSOP−14 T SUFFIX HT4541BRTZ

MARKING DIAGRAMS



B = The version number

T_A = -55° to 125° C for all packages

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +20.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient)	±10 (per Pin)	mA
I_{out}	Output Current (DC or Transient)	±45 (per Pin)	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/ C From 65 C To 125 C

PIN ASSIGNMENT

R_{tc}	1 ●	14	V_{DD}
C_{tc}	2	13	B
R_S	3	12	A
NC	4	11	NC
AR	5	10	MODE
MR	6	9	$Q/\overline{Q}$ SEL
V_{SS}	7	8	Q

NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55 C		25 C			125 C		Unit
			Min	Max	Min	Typ [4.]	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 10 15	– 7.96 – 4.19 – 16.3	— — —	– 6.42 – 3.38 – 13.2	– 12.83 – 6.75 – 26.33	— — —	– 4.49 – 2.37 – 9.24	— — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	1.93 4.96 19.3	— — —	1.56 4.0 15.6	3.12 8.0 31.2	— — —	1.09 2.8 10.9	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Auto Reset Quiescent Current (Pin 5 is low)	I_{DDR}	10 15	— —	250 500	— —	30 82	250 500	— —	1500 2000	μAdc
Supply Current [5.] [6.] (Dynamic plus Quiescent)	I_D	5.0 10 15	I_D = (0.4 μA/kHz) f + I_{DD} I_D = (0.8 μA/kHz) f + I_{DD} I_D = (1.2 μA/kHz) f + I_{DD}							μAdc

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25 C.
6. When using the on chip oscillator the total supply current (in μAdc) becomes: $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in μA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power–on with automatic reset enabled is typically 50 μA @ V_{DD} = 10 Vdc.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25 C)

Characteristic	Symbol	V_{DD}	Min	Typ [8.]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Propagation Delay, Clock to Q (2^8 Output) t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns	t_{PLH} t_{PHL}	 5.0 10 15	 — — —	 3.5 1.25 0.9	 10.5 3.8 2.9	µs
Propagation Delay, Clock to Q (2^{16} Output) t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns	t_{PHL} t_{PLH}	 5.0 10 15	 — — —	 6.0 3.5 2.5	 18 10 7.5	µs
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0 10 15	— — —	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	$t_{WH(R)}$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Master Reset Removal Time	t_{rem}	5.0 10 15	420 200 200	210 100 100	— — —	ns

7. The formulas given are for the typical characteristics only at 25 C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

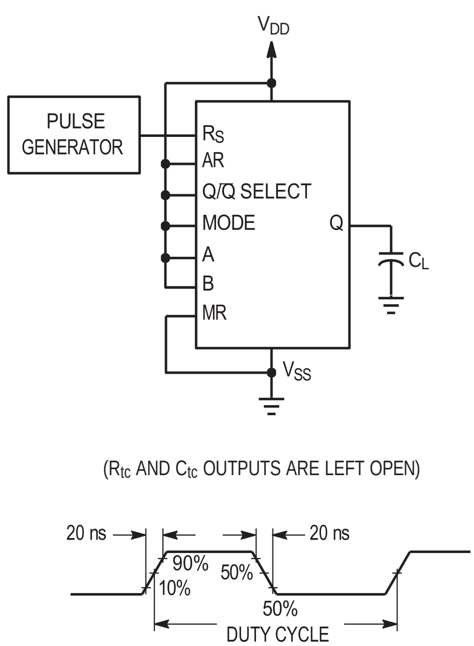


Figure 1. Power Dissipation Test Circuit and Waveform

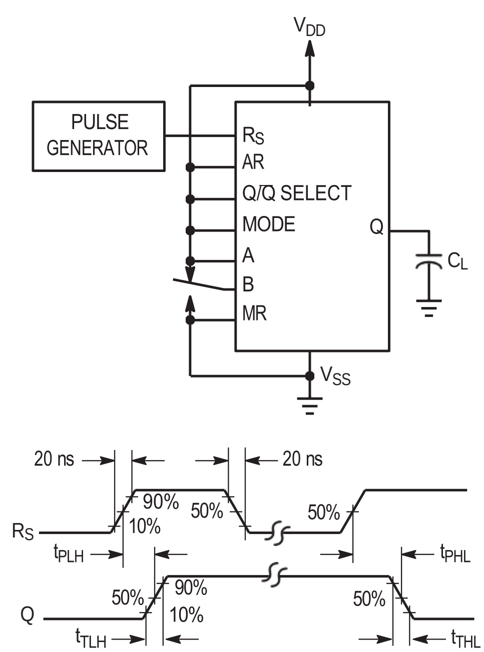
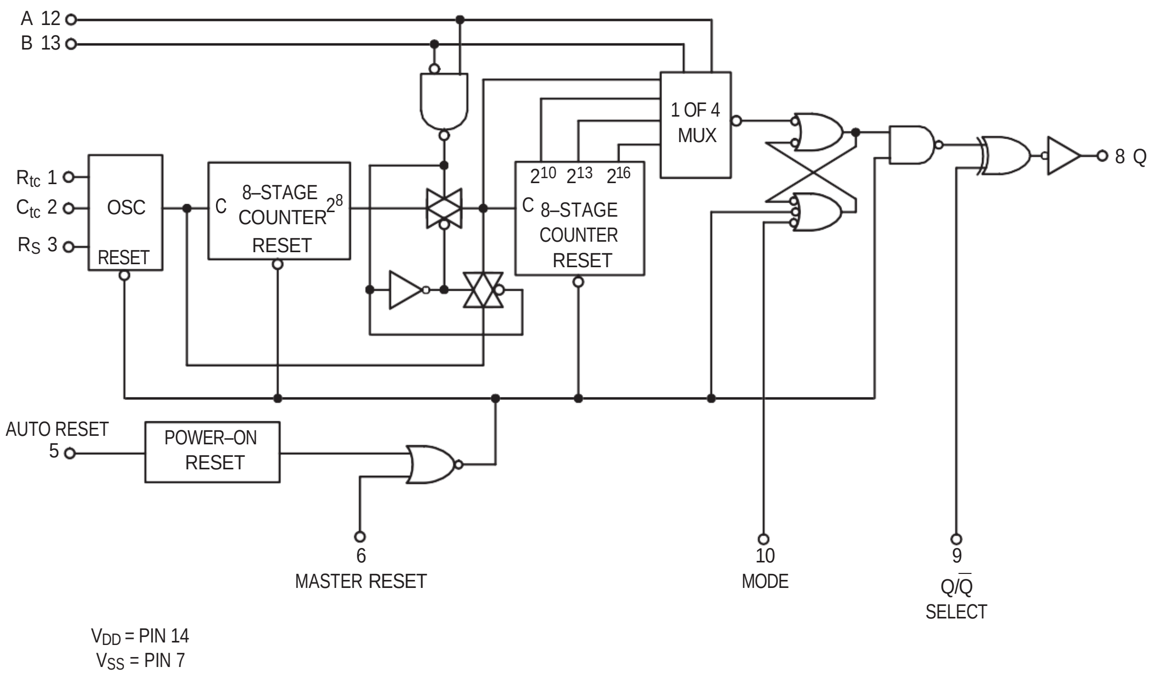


Figure 2. Switching Time Test Circuit and Waveforms

EXPANDED BLOCK DIAGRAM



FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/$\overline{Q}$, 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

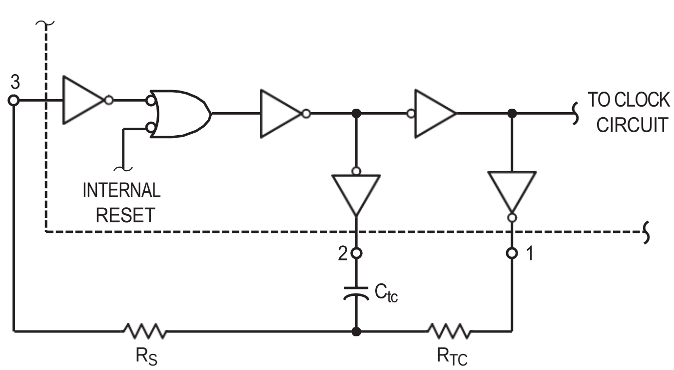


Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

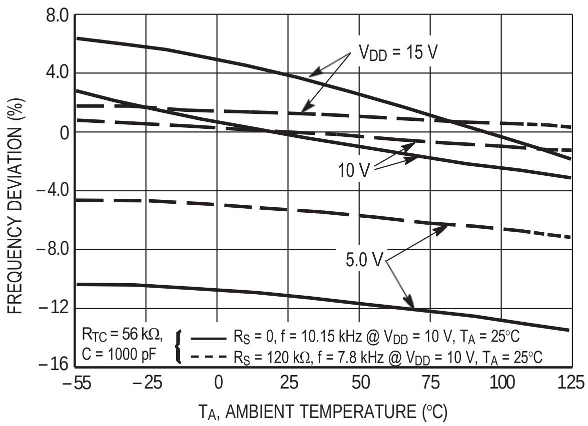


Figure 4. RC Oscillator Stability

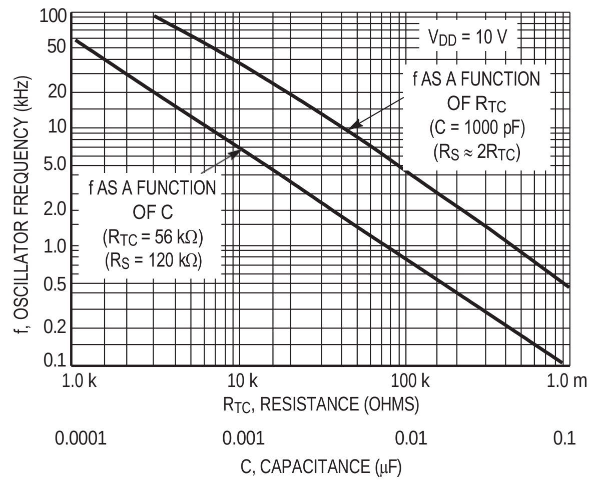


Figure 5. RC Oscillator Frequency as a Function of R_{tc} and C_{tc}

OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a “1” provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\, R_{tc} C_{tc}} \quad \text{if (1 kHz} \quad f \quad \text{100 kHz)}$$

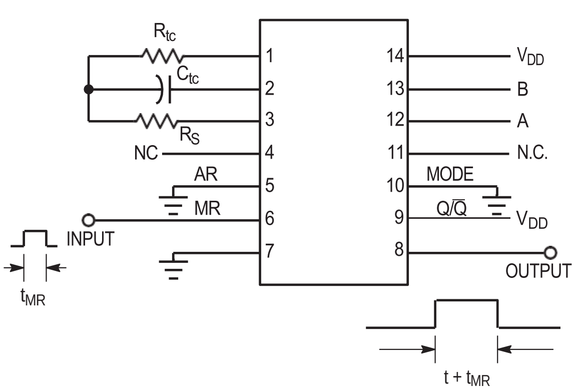
and $R_S \approx 2\, R_{tc}$ where $R_S \geq 10\ k\Omega$

The time select inputs (A and B) provide a two–bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is “1”, 2^{16} is selected for both states of B. However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a “0” the Q output is a “0”, correspondingly when Q/$\overline{Q}$ select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the R_S flip–flop (see Expanded Block Diagram) resets, counting commences, and after 2^{n-1} counts the R_S flip–flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



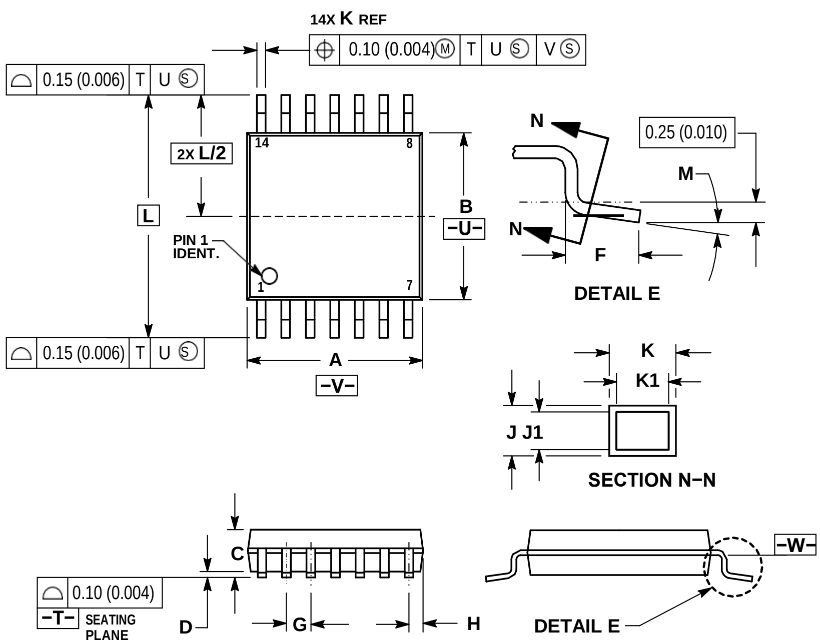
When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

PACKAGE DIMENSIONS

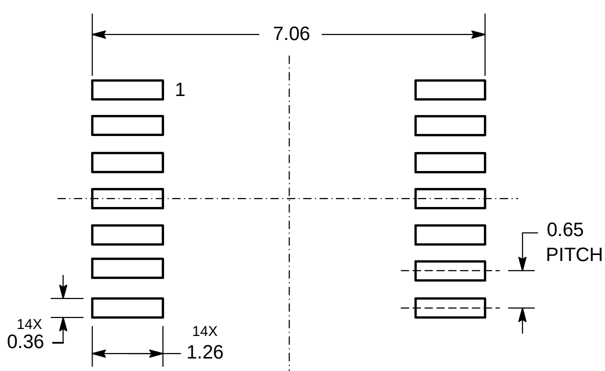
TSSOP−14



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETER		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

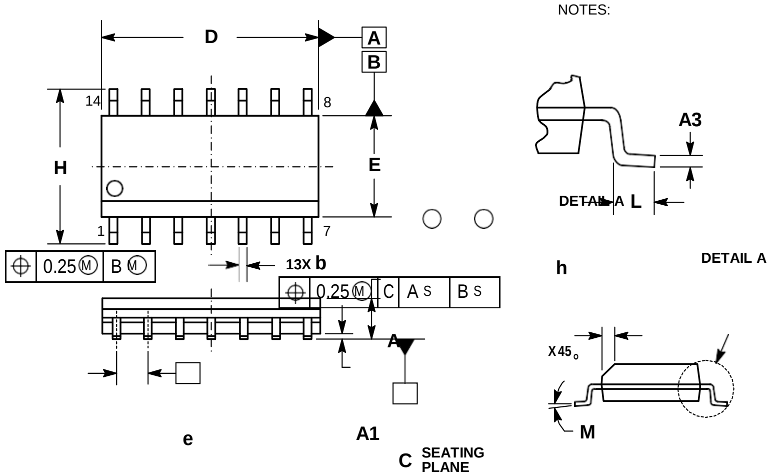


PACKAGE DIMENSIONS

SOP14

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*