YTM32Z1LS0x Data Sheet

Support: YTM32Z1LS06H0MFNR

Document Number: YTM32Z1LS0x DS

Rev.1.2, 2025/4/3

1 Features

- ASIL-B compliant
- QM compliant
- RoHS compliant
- 32-bit ARM Cortex-M0+ core running up to 48 MHz
- Memory
  - 128 KB PFlash with ECC which supports single error correction (SEC) and double error detection (DED)
  - 16 KB SRAM with ECC which supports single error correction (SEC) and double error detection (DED)
- Clocks
  - Fast IRC (FIRC), up to 48 MHz
  - Fast crystal oscillator (FXOSC), range 4~40 MHz
  - Slow IRC (SIRC), up to 2 MHz
  - Slow crystal oscillator (SXOSC), run at 32.768 KHz
  - Low power oscillator (LPO), run at 750 Hz
- 4 DMA channels with up to 41 peripheral hardware trigger sources
- DIVSQRT module with 32-bit integer divide and square root operations
- Mixed-signal analog
  - One Analog-to-Digital Converter (ADC) with 12-bit 1Msps sample rate, it has 12 channels and supports temperature sensor
  - One Analog Comparator (ACMP) with 8-bit DAC
  - Support 12V automotive applications with 5.5V to 28V wide input voltage operating range
  - 5V LDO for analog/IOs and 1.5V LDO for digital
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant
- Enhanced Timer (eTMR), Periodic Timer (pTMR), Low Power Timer (lpTMR) and Real Time Clock (RTC) for a broad range of applications including motor control
- Serial communication interfaces such as UART, SPI, I2C and FlexCAN with FD
- High security and safety with internal Watchdog (WDG), programmable CRC module, ECC Management Unit (EMU) and Clock Monitor Unit (CMU)
- Single power supply with full functional flash program/erase/read operations
- Power management
  - LINPHY
    - support three power modes: Normal, Standby, and Sleep
  - MCU
    - Low-power ARM Cortex-M0+ core with excellent energy efficiency
    - Support four power modes: Active, Sleep, Deepsleep and Standby
    - Support clock gating for unused modules, and specific peripherals remain working in Sleep, Deepsleep and Standby mode
- Up to 39 GPIO pins with interrupt functionality
- Support 48 QFN package
- Temperature parameters:
  - Ambient operation temperature range: -40°C ~ 125°C

Contents

2 Overview

YTM32Z1LS0x series is an automotive ARM® Cortex®-M0+ MCUs that offers the capability to integrate high voltage analog components. This series integrates high-voltage modules, including the high voltage regulator(LDO), Local Interconnect Network(LIN) physical layer and general purpose MCU based on Cortex-M0+. YTM32Z1LS0x series devices are optimized for cost-sensitive applications offering low pin-count option.

The YTM32Z1LS0x series offers a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32Z1LS0x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

3 Block Diagram

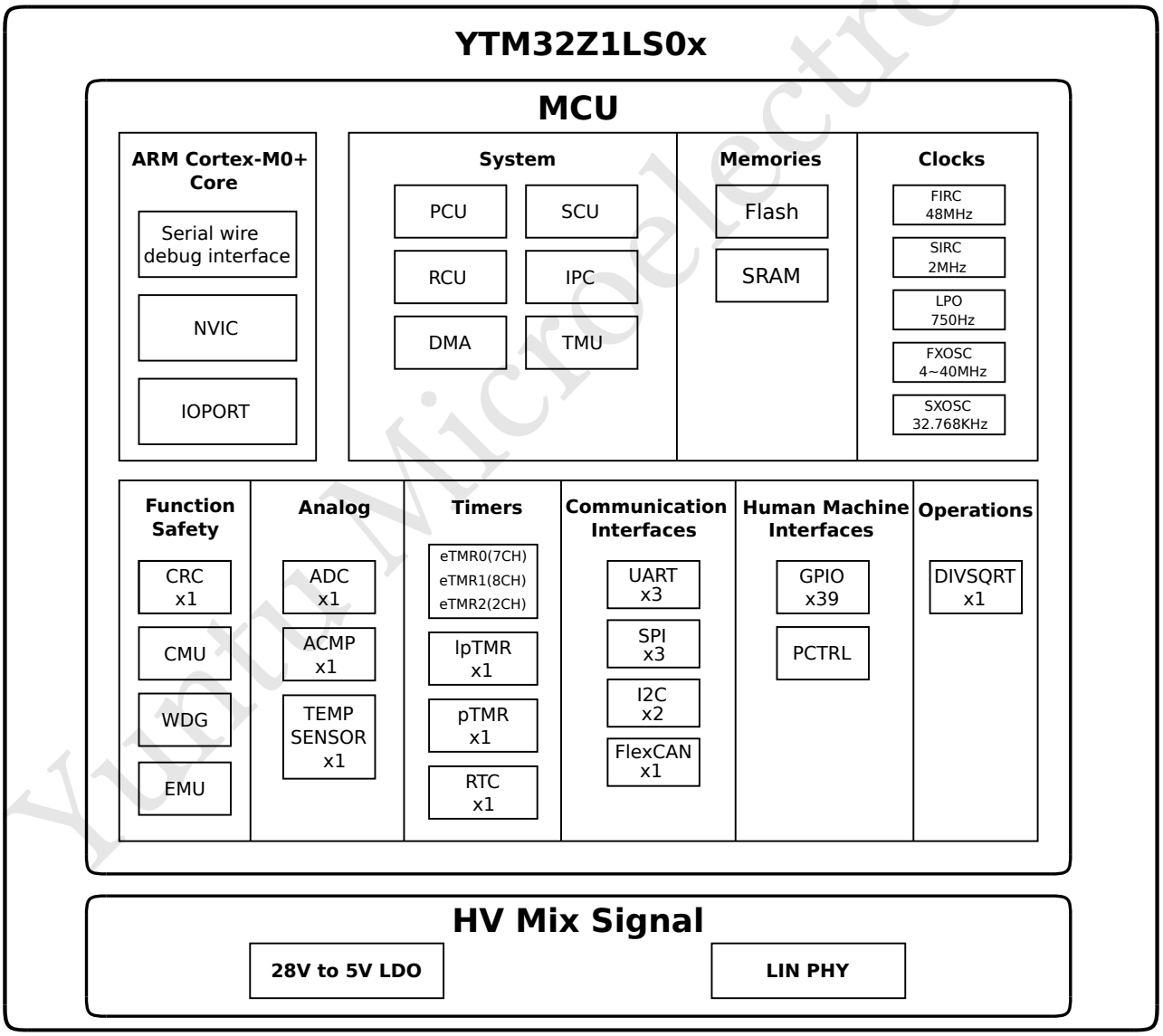


Figure 1: YTM32Z1LS0x Block Diagram

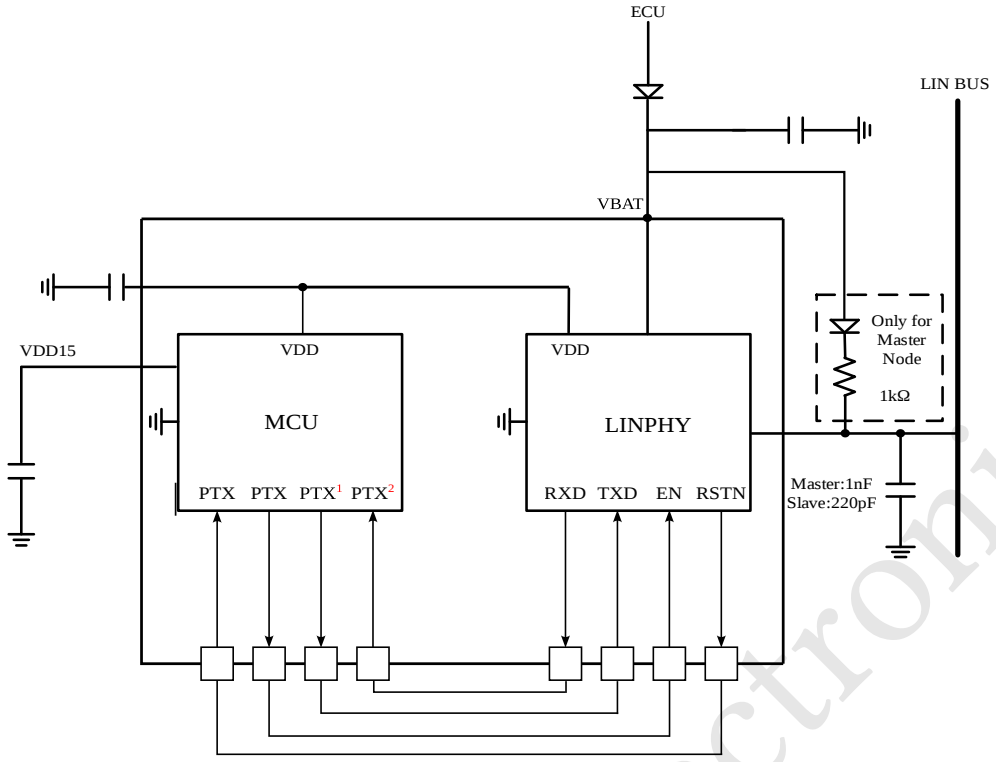


Figure 2: Typical Application Circuit in LIN Bus

4 Features

The following sections describe the high-level module features for YTM32Z1LS0x device.

4.1 Core Modules

4.1.1 ARM Cortex-M0+

- Up to 48 MHz core frequency
- Supports up to 32 interrupt request sources
- 2 stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiplier

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Supports four priority levels for interrupts with two bits in each IPRn registers
- Includes a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast internal RC oscillator (FIRC)
  - Up to 48 MHz
  - Default system boot clock source
  - Support trim for temperature and process
- Slow internal RC oscillator (SIRC)
  - Run at 2 MHz
  - Can be selected as system clock source
  - Always on unless it is forced to be disable in standby mode
  - Support trim for temperature and process
- Fast crystal oscillator (FXOSC)
  - Support 4~40 MHz crystal
  - Can be selected as system clock source
  - Support bypass mode
- Slow crystal oscillator (SXOSC)
  - 32.768 KHz real time oscillator
  - Can't be selected as system clock
  - Provides accurate clock to watchdog(WDG) and real time clock(RTC)
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock
- SCU contains 2 CMU blocks
  - CMU monitors FXOSC and FIRC clock
  - CMU reference clock is SIRC
  - CMU can detect frequency out of range, loss of checked clock and loss of reference clock

4.2.2 Power Control Unit (PCU)

- Combination of power management blocks including POR, Bandgap, LVD, Brownout, full power regulator and low power regulator
- Responsible for sequencing the system enter and exit the Standby mode
- Low Voltage Reset(LVR) for all system relevant power domains
- Designed to support 12V applications with wide operating supply range:
  - 5.5V to 28V supply range (V_{BAT})
- Voltage regulator offering 5 V, 30 mA capability

4.2.3 Reset Controller Unit (RCU)

- Manage the system power up, pin reset, functional reset and fault reset flow
- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work in Active, Sleep, Deepsleep and Standby mode

4.2.4 IP Controller (IPC)

- Peripheral Bus clock enable

- IPC clock source selection as follow
  - FIRC 48 MHz
  - FXOSC 4~40 MHz
  - SIRC 2 MHz
  - SXOSC 32.768 KHz
  - LPO 750 Hz
- IPC clock divide values from 1 to 16

4.2.5 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
  - Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/not change selectable
- Up to 4 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware trigger
- Up to 41 peripheral hardware triggers
- Internal data fifo for data transfer
- Support update DMA transfer information from system memory after transfer complete

4.2.6 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- ADC/ACMP trigger synchronize selection
- Software trigger generate
- eTMR external clock and fault selection
- eTMR channel input/output selection
- Chip and die information

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- 128 KB Program Flash(PFlash) with ECC which supports single error correction (SEC) and double error detection (DED)
- 24 MHz single cycle reads of bytes, aligned halfword (16-bit) and aligned word (32-bit)
- Automated generation of ECC parity while programming and erasing
- Optional interrupt on command completion
- Program and erase operations do not require any special power sources other than the normal VDD supply

4.3.2 On-chip SRAM

- 16 KB SRAM with ECC supports single error correction (SEC) and double error detection (DED)

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 1.0μs for 12-bit resolution conversion time
- Support DMA and conversion result FIFO with watermark
- Support up to 17 input channels
  - 12 channels to measure external analog signals from pad
  - 1 channel to measure internal temperature sensor
- Support multiple conversion modes
  - Single mode: convert one or more channels once a time
  - Continuous mode: convert one or more channels until stopped by software
  - Discontinuous mode: convert one channel once a time
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
- Support work and wake up when the whole chip under low power mode

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-shot mode
    - Loop mode
- Up to 8 channels can be used to execute automatic comparisons
- Digitally filtered, filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in low power mode
- Support independent DAC input channel to the comparator
  - Optional DAC reference source: internal or external reference source
  - 8-bit DAC resolution

- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
    - Generate interrupt when the comparison results don't match expectations
- Interrupt can generate without any clock
- A comparison event can be selected to trigger DMA transfer

4.5 Timer

4.5.1 Periodic Timer (pTMR)

- Timers can generate interrupts
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timers to a longer timer

4.5.2 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wake-up from any low power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler and glitch filter
- Configurable input source for pulse counter
  - Rising-edge
  - Falling-edge
- Support triggering DMA transfer

4.5.3 Enhanced Timer (eTMR)

- There are three eTMRs with below configurations
  - eTMR0: 7 channels
  - eTMR1: 8 channels
  - eTMR2: 2 channels
- Bus clock and external clock can be the source clock of each eTMR
- Each eTMR contains a 7-bits clock prescaler
- Each eTMR contains a 16-bit counter
- Each channel can be configured as three modes
  - Input Capture mode
    - Support rising edges, falling edges or dual edges
    - Support input filter with a prescaler that can be selected for channels, eTMR0: channel 0-3, eTMR1: channel 0-3, eTMR2: channel 0-1
  - Output Compare mode
    - The output signal can be configured to set, clear or toggle on match point
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair channels: Pair channels: channel 0-1, channel 2-3, channel 4-5, channel 6-7
    - Supports independent deadtime insertion for odd and even channel
    - Fault control mechanism: eTMR0 and eTMR1 support 4 fault inputs for global fault control

- Each eTMR can be configured to generate triggers
  - Output triggers on match point
  - Output pulse-out with adjustable pulse width
- PWM outputs can be controlled by software
- Polarity control is available for every channel of each eTMR
- Mask control is available for every channel of each eTMR
- Synchronized loading of write buffered registers is available in each eTMR
- Capture test mode is available in each eTMR
- eTMR1 can be configured as quadrature decoder, which supports relative position counting or external event counting
  - Support phase A and phase B input filters
  - Contains a independent 16-bits counter with a clock prescaler
  - Support 4 up-down counting modes
- Support GTB (Global Time Base) for all eTMRs
- Support several interrupts
  - Channel interrupt (input capture interrupt and output compare interrupt)
  - Counter overflow interrupt
  - Fault interrupt
- Support DMA

4.5.4 Real Time Clock (RTC)

- 32-bit seconds counter with prescaler of 1 Hz
- Support compensation with RTC clock
- Lock support of register access for control and alarm register
- Selectable of 1 Hz to 128 Hz square wave output
- Support two clock sources

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit uses
  - CRC-32 polynomial:
    $X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - CRC-16 polynomial: $X^{16} + X^{12} + X^5 + 1$
  - CRC-4 polynomial: $X^4 + X + 1$
- Programmable initial seed value
- Accept with 8-bit or 16-bit or 32-bit input data size
- Option to transpose input data or output data (the CRC result) bitwise
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

4.6.2 Watchdog (WDG)

- Support regular or window servicing mode
- Support reset request or interrupt for first timeout
- Support fixed key for dog feeding

4.6.3 ECC Management Unit (EMU)

- Error injection
  - Error injection provides a method for diagnostic coverage of SRAM.
  - Error injection uses two-stage enable mechanism.
  - Error injection provides support for inducing single-bit or multi-bit inversions on read data when accessing SRAM
- Error reports
  - Error report provides information and optionally interrupt notification on SRAM error events associated with ECC (Error Correction Code) and parity
  - Error report provides count registers which count all correctable error so far

4.7 Operation Unit

4.7.1 Divide and Square Root (DIVSQRT)

- Support 32-bit integer divide and square root arithmetic operations
  - Divide arithmetic support unsigned and signed 32-bit integer
  - Support selectable action to divide-zero
  - Square arithmetic support unsigned 32-bit integer
- Input data and result are memory-mapped with easy programming model
  - Support data write to start calculation and data read get result
  - Support control and status register for calculation

4.8 Communication Interfaces

4.8.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0 Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32 or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 32 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts

- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8-bit) IDs, with up to 32 ID Filter Table elements

4.8.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN mode
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baud rate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wake-up
- Support transmit/receive line switch, single line mode
- Hardware flow control support

4.8.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support Master and slave mode
- Support Transmit/Receive via DMA

4.8.4 Inter-Integrated Circuit (I2C)

- Support standard, fast and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBUS mode
- Support multi-master arbitration and synchronization
- Support Master and slave clock stretching
- Transmit/Receive FIFO (Master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA
- I2C1 do not support slave mode

4.8.5 Local Interconnect Network Physical Layer (LINPHY)

- Meets LIN2.0, LIN2.1, LIN2.2, LIN2.2A and ISO 17987-4:2016(12V) physical-layer (EPL) standards
- Compliant to SAE J2602-1 and SAE J2602-2 LIN physical-layer specification
- Support up to 20kbps LIN transmission data rate
- Operating mode
  - Normal operation
  - Low-power Standby typ.25μA
  - Low-power Sleep typ.16μA
  - Power-off
- Wake-up from low-power mode
  - Remote wake-up via LIN bus
  - Wake-up via EN pins
- Integrated 30kΩ LIN pull-up resistor
- Power-up/down glitch-free operation on LIN bus and RXD output
- Integrated protection increases robustness
  - $\pm$ 42V fault-tolerant LIN bus
  - 42V load dump protection
  - Enhanced ESD protection
  - Undervoltage protection on V_{BAT}
  - Transmitter dominant timeout prevents lockup
  - VDD output voltage short and LIN bus short circuit protection functions
  - Thermal shutdown
  - System level fail-safe protection for the unpowered node or ground disconnection

4.9 Human Machine Interface

4.9.1 General Purpose Input/Output (GPIO)

- Port Data Input register visible in all digital pin multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Port Input Disable register
- Pin interrupts
  - Interrupt flag and enable registers for each pin, functional in all digital pin multiplexing modes
  - Support for interrupt, DMA request or Peripheral Trigger configured per pin
  - Support for edge sensitive (rising, falling, both) or level sensitive (low, high) configured per pin
  - Asynchronous wake-up in low power modes
  - Each pin can be configured for 1 of interrupt, DMA request or trigger output

4.9.2 Port Controller (PCTRL)

- Individual pull control fields with pull-up, pulldown and pull-disable support
- Individual drive strength field supporting high and low drive strength
- Individual mux control field supporting analog or pin disabled, GPIO and up to 6 chip-specific digital functions
- Individual passive filter field supporting enabling and disabling passive filter for specific input

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering table

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash	SRAM	Pin count	Package	GPIO	ADC	FlexCAN
YTM32Z1LS06H0MFNR	128KB	16KB	48	QFN	39	12	1

5.1 Part Numbers

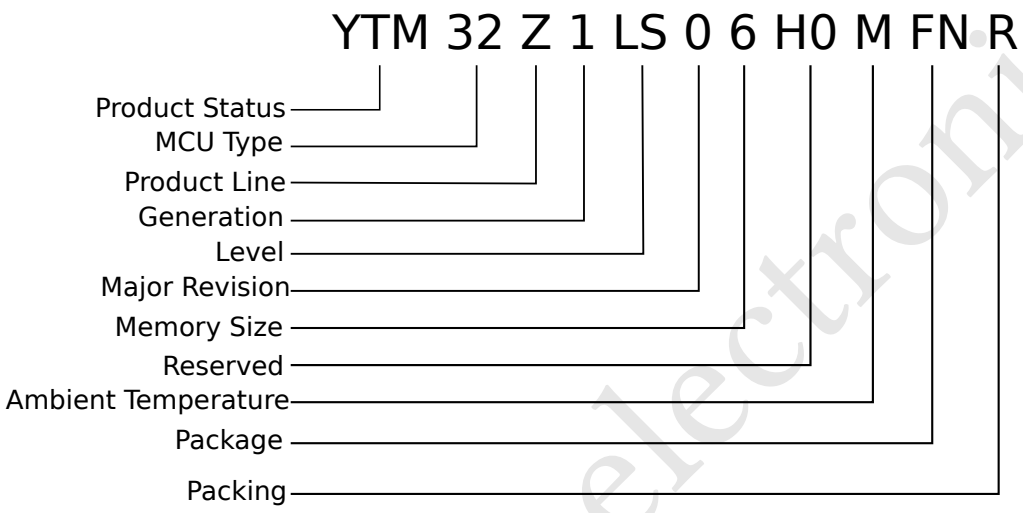


Figure 3: Part Numbers Field

The part numbers field description is shown as below.

Table 2: Part Number Field Description

Field	Description	Values					
YTM	Product Status	YTM: Qualified PTM: Prototype					
32	MCU Type	32: 32-bit					
Z	Product Line	Z: High voltage, integrity					
1	Generation	1st generation production					
Lx	Level	M: Motor+LIN-PHY L: LIN-PHY C: CAN-PHY T: Touch-sensor					
0	Major Revision	1st revision					
6	Memory Size	1	2	3	4	5	6
		8K	16K	32K	48K	64K	128K
H0	Reserved	Reserved					

Field	Description	Values				
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C				
FN	Package	Pins	LQFP	QFN	BGA	-
		24	-	FK	-	-
		32	LE	FM	-	-
		48	LF	FN	-	-
		64	LH	-	-	-
		100	LL	-	MH	-
		144	LQ	-	-	-
		176	LU	-	-	-
		257	-	-	MM	-
		289	-	-	MQ	-
D	Optional Feature	S: Single end mode D: Differential mode				
T[1]	Packing	T: Trays/Tubes R: Tape and Reel				

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	135	°C
T_{STG}	Storage temperature range	-55	–	135	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	3	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (except V_{HBM_LIN})	-2000	2000	V	1
V_{HBM_LIN}	Electrostatic discharge voltage, human body model, only LIN pin to VSS	-6000	6000	V	
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-50	50	mA	3
	Latch-up current at ambient temperature of 25 °C	-100	100	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.1.4 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8[1]	V	
I_{VDD}	Maximum current into V_{DD}	–	70	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	
V_{BAT}	Supply voltage range (To VSS, To LIN)	-0.3	42	V	
V_{DD}	LDO Output Voltage (To VSS)	-0.3	7	V	
TXD	TXD voltage range (To VSS)	-0.3	V_{DD}+0.3	V	
RXD	RXD voltage range (To VSS)	-0.3	V_{DD}+0.3	V	
RSTN	RSTN voltage range (To VSS)	-0.3	V_{DD}+0.3	V	
RSTEN	EN voltage range (To VSS)	-0.3	V_{DD}+0.3	V	
LIN	LIN voltage range (To VSS, To V_{BAT})	-42	42	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.
10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.

- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

6.2.1 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	4.9	5.1	V	
V_{DDA}	Analog supply voltage	4.9	V_{DD}	V	
V_{REFH}	Reference voltage	4.9	V_{DDA}	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-1	1	mA	1
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	–	15	mA	
T_{ramp}	MCU supply ramp rate	5 V/100ms	100 V/ms	–	
V_{BAT}	Battery voltage range	5.5	28	v	
V_{LIN}	LIN bus voltage range	0	28	v	
V_{LOGIC}	Logic voltage range (RSTN, RXD, EN and TXD)	0	5.5	V	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} − 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}-0.3V-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}-(V_{DD}+0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.2 DC Electrical Specifications at 5.0V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4.9	5	5.1	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.1 * V_{DD}	–	0.3 * V_{DD}	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	10	20	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	10	20	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	20	30	–	mA	

Table 8 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	20	30	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	380	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	–	500	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($4.9V \leq V_{DD} \leq 5.1V$, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	V_{DD}	V	
V_{OL}	Output low voltage					
	Normal drive pad ($4.9V \leq V_{DD} \leq 5.1V$, I_{OL} = -2.8mA)	V_{SS}	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Noraml pins	–	0.002	0.5	μA	
	High drive pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	15	–	70	kΩ	
V_{DD}	LDO output supply voltage (V_{DD}=5V, V_{BAT}=12V; I_{VDD}=-30mA to 0mA, V_{DD} power supply current capability,)	4.9	5	5.1	V	
I_{Olim}	Output current limit (V_{DD}=0V to 5.5V)	-500	-360	-150	mA	
V_{uvd}	Under voltage detection voltage ($V_{DD(nom)}$=5V, Ramp Down)	4.3	4.5	4.75	V	
V_{uvr}	Under voltage recovery voltage ($V_{DD(nom)}$=5V, Ramp Up)	4.4	4.62	4.9	V	
$R_{(VBAT-VDD)}$[1]	resistance between pin V_{BAT} and pin V_{DD} ($V_{DD(nom)}$=5V; V_{BAT}=4.5V to 5.5V; I_{VDD}=-70mA to -5mA; LDO regulator in saturation;)					
	T_{VJ}= 85°C	–	5	7	Ω	
	T_{VJ}= 135°C	–	5	7	Ω	
C_O[1]	Output capacitance (equivalent series resistance <5Ω)	1	10		μF	

1. The test data is based on bench test and design simulation.

6.2.3 Power and Ground Pins

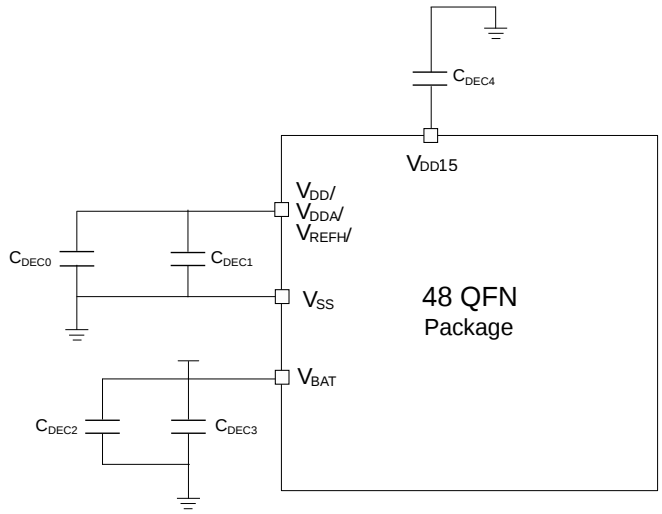


Figure 4: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{DEC0} [1,2,3,4]	Recommended decoupling capacitance	1	–	10	μF
C_{DEC1} [1,2,3,4]	Recommended decoupling capacitance	50	100	200	nF
C_{DEC2} [1,2,3,4]	Recommended decoupling capacitance	1	–	10	μF
C_{DEC3} [1,2,3,4]	Recommended decoupling capacitance	50	100	200	nF
C_{DEC4} [2,3,4]	Recommended decoupling capacitance	1	–	10	μF

1. For improved performance, it is recommended to use 0.1μF and 4.7μF capacitors in parallel.
2. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
3. All decoupling capacitors must be low ESR ceramic capacitors(for example X7R type).
4. The requirement and value of C_{DEC} will be decided by the device application requirement.

6.2.4 Power on Reset (V_{BAT})

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$V_{th(det)pon}$	power-on detection threshold voltage			4.05	5.25	V
$V_{th(det)poff}$	power-off detection threshold voltage		3	3.7	4.2	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		50	350		mV

6.2.5 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	1μs	–
DEEPSLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	5μs	–
STANDBY -> ACTIVE	FIRC	48MHz, 24MHz	–	40μs	–
T_{POR}	FIRC(reset value)	48MHz, 24MHz	–	250μs	–

6.2.6 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	FIRC	Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	$\leq$ 25 °C	–	9.0	14.5	mA
				125 °C	–	9.0	14.5	mA
SLEEP	I_{DD_SLEEP}	FIRC	Sleep mode current, V_{DD}=5V	$\leq$ 25 °C	–	3.9	5.0	mA
				125 °C	–	4.0	5.0	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	FIRC	Deepsleep mode current, V_{DD}=5V SIRC=1, SXOSC=0	$\leq$ 25 °C	–	100	150	μA
				125 °C	–	130	250	μA
STANDBY	$I_{DD\_STANDBY}$	FIRC	Standby mode current, V_{DD}=5V SIRC=1, SXOSC=0	$\leq$ 25 °C	–	4.0	20	μA
				125 °C	–	50	100	μA
POWERDOWN	$I_{DD\_POWERDOWN}$	FIRC	Powerdown mode current, V_{BAT}=12V LIN wakeup, LDO disabled, and MCU power off	$\leq$ 25 °C	–	15.6	–	μA
				125 °C	–	17.9	–	μA

6.2.7 Power Sequence

6.2.7.1 Power Up Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

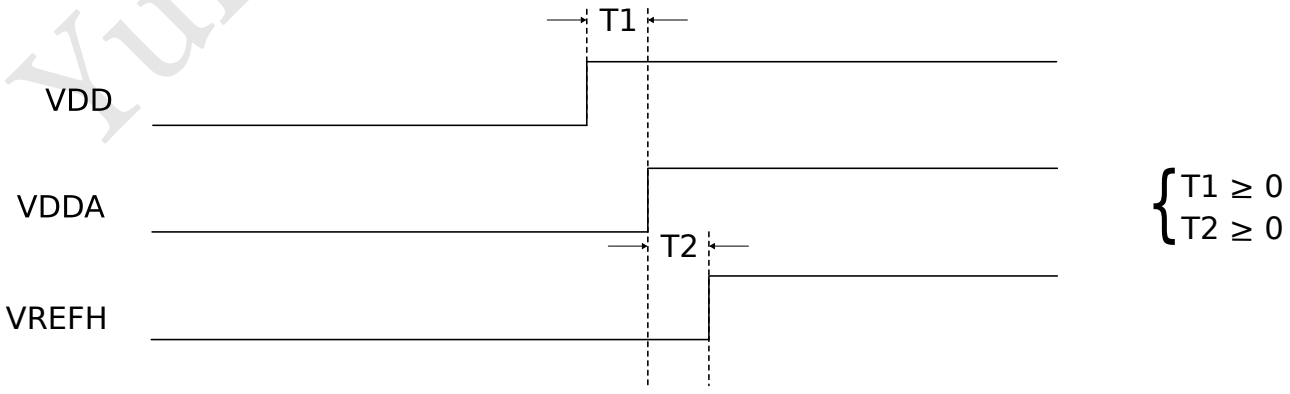
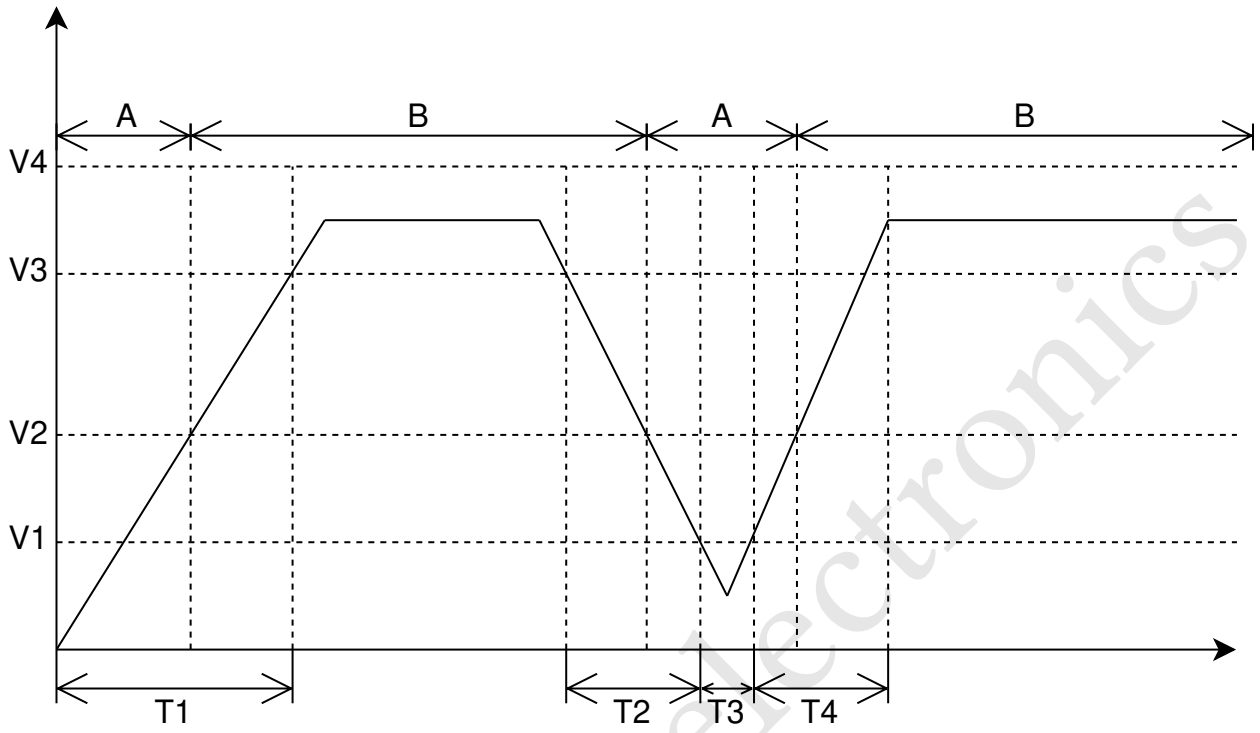


Figure 5: Power Sequence

6.2.7.2 Power Up Requirements

It is necessary to ensure that VDD meets the following timing during the power-up process of YTM32Z1LS0x.



A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 6: Power Up Requirements

Symbol	Name	Description	Unit (V)
V1	Restart threshold voltage	When restarting the MCU, VDD should keep below V1 for a period of T3.	0.2
V2	Minimum MCU operating voltage	The MCU starts working when the power supply reaches V2.	2.5
V3	Lower voltage limit of MCU operating normally	Minimum operating voltage for normal MCU operation and interaction with peripherals.	2.7
V4	Upper voltage limit of MCU operating normally	Maximum operating voltage for normal MCU operation and interaction with peripherals	5.5

Symbol	Name	Description	Requirement
T1	Power up time	Rising time of MCU VDD from 0V to V3	10 μs < T1 < 50ms
T2	Power down time	Drop time of MCU VDD from V3 to V1 during the MCU restart/power down process	10 μs < T2 < 500ms
T3	Restart threshold voltage retain time	Minimum duration of MCU VDD below V1, when restarting MCU	T3 > 100 μs

Table 14 continued from previous page

Symbol	Name	Description	Requirement
T4	Restart power up time	Rising time of MCU VDD normal operation from V1 to V3	10 μs < T4 < 50ms

NOTE: The power-up process needs to be restarted if a VDD voltage drop occurs during the T1~T4 power-up process before the VDD voltage reaches the V2 voltage. Restarting the power-up of MCU needs to ensure that the voltage of VDD continues to drop below V1 and remains there for T3 time.

6.2.8 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Power Supply Fluctuation Requirements

1. The power supply fluctuation must be maintained within ± 10% of the power supply voltage, and the fluctuation frequency should not exceed 100 KHz.
2. The maximum power supply fluctuation should not exceed ± 20% of the power supply voltage, and in this case, the fluctuation frequency should be less than 30 KHz.
3. Power supply fluctuations exceeding the above requirements may cause chip abnormalities and require a power-up process according to the requirements outlined in Power Up Requirements.

6.3.2 Device Clock Specifications

Symbol	Description	Min.	Max.	Unit	Notes
f_{core}	System and core clock	–	48	MHz	
f_{bus}	Bus clock	–	24	MHz	

6.3.3 I/O Electrical Characteristics

6.3.3.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

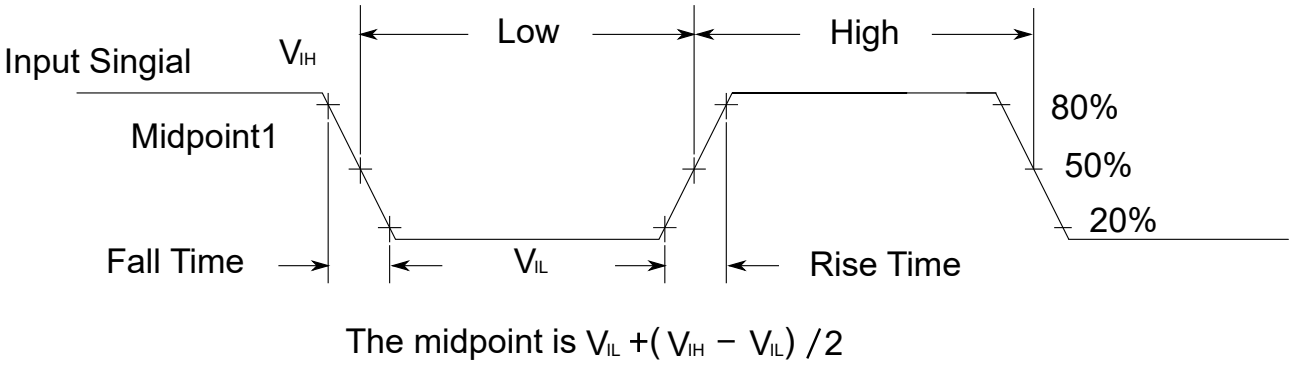


Figure 7: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40MHz) Characteristics

The following diagram is Fast Crystal OSC circuit.

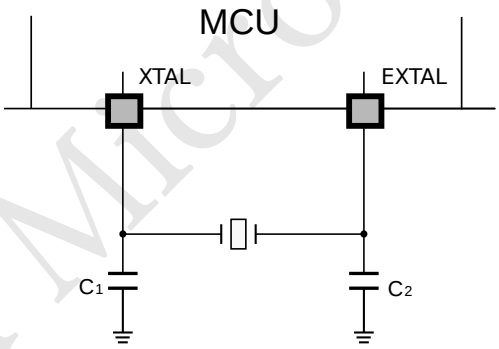


Figure 8: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	4.9	5	5.1	V	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, V_{DD}=5V	0.7*V_{DD}	–	V_{DD}	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, V_{DD}=5V	V_{SS}	–	0.3*V_{DD}	V	
$T_{FXOSCSU}$	FXOSC startup time (40MHz oscillator)	–	0.5	3.5	ms	
D_{FXOSC}	Duty of FXOSC (40MHz oscillator)	40	50	60	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	

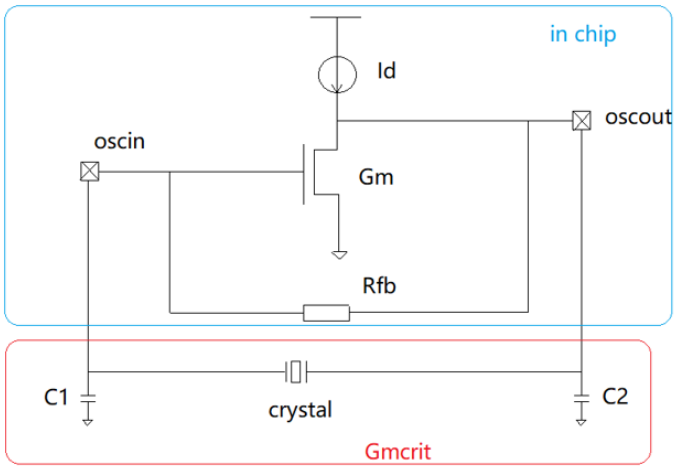
Table 16 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_F	FXOSC internal feedback resistor	400	500	700	kΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (40MHz oscillator)	1.2	2.25	V_{DD}	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as: gm_crit=4 * (ESR + R_S) * $(2\pi F)^2$ * $(C_0 + C_L)^2$

where:

- g_{mXOSC} is the transcondutance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [\ C_1 * C_2 / (C_1 + C_2)\ ]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins.



■ The internal circuitry of the chip utilizes an Id current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (Gm) of the amplifying transistor is greater than the intrinsic gain (Gmcrit) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that Gm>5*Gmcrit.

■ Rfb provides the DC bias point for the input terminal of the amplifying transistor.

Figure 9: Block Diagram of Crystal Oscillator Circuit

Table 17: Startup Time - Gain Selection for Gmxosc of 40MHz Crystal Oscillator Circuits (Simulation)

Gain Setting	Gm (at statup)			Unit
	Min.	Typ.	Max.	
0x0			0	mS
0x1	1.4	2.2	3.6	mS
0x2	2.8	4.5	7.2	mS
0x3	4.2	6.8	10.8	mS

Table 17 continued from previous page

Gain Setting	Gm (at statup)			Unit
	Min.	Typ.	Max.	
0x4	4.9	7.9	12.6	mS
0x5	6.2	10.2	16.2	mS
0x6	7.6	12.5	19.9	mS
0x7	9.1	14.7	23.5	mS

6.4.2 FIRC(48MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	48	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-1.0	–	1.0	%	
	FIRC frequence accuracy, factory trimmed, -40°C – 125°C	-1.5	–	1.5	%	
I_{FIRC}	FIRC operating current	–	250	–	μA	
$T_{Startup}$	Startup time	–	–	20	μs	

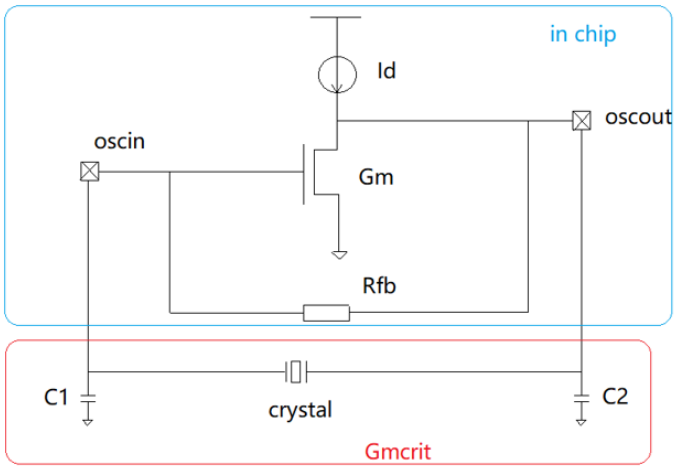
6.4.3 SXOSC(32.768KHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SXOSC}	Slow crystal oscillator frequency	30	32.768	35	KHz	
$T_{startup}$	SXOSC startup time (32.768KHz oscillator)	–	–	1	s	
D_{SXOSC}	Duty of SXOSC (32.768KHz oscillator)	40	50	60	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	SXOSC internal feedback resistor	6	8	11	MΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (32.768KHz oscillator)	0.94	1.2	V_{DD}	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as: gm_crit=4 * (ESR + R_S) * $(2\pi F)^2$ * $(C_0 + C_L)^2$

where:

- g_{mXOSC} is the transcondutance of the internal oscillator circuit. g_{mXOSC} > 10 μS
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [C_1 * C_2 / (C_1 + C_2)]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins



- The internal circuitry of the chip utilizes an Id current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (Gm) of the amplifying transistor is greater than the intrinsic gain (Gmcrit) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that Gm>5*Gmcrit.

- Rfb provides the DC bias point for the input terminal of the amplifying transistor.

Figure 10: Block Diagram of Crystal Oscillator Circuit

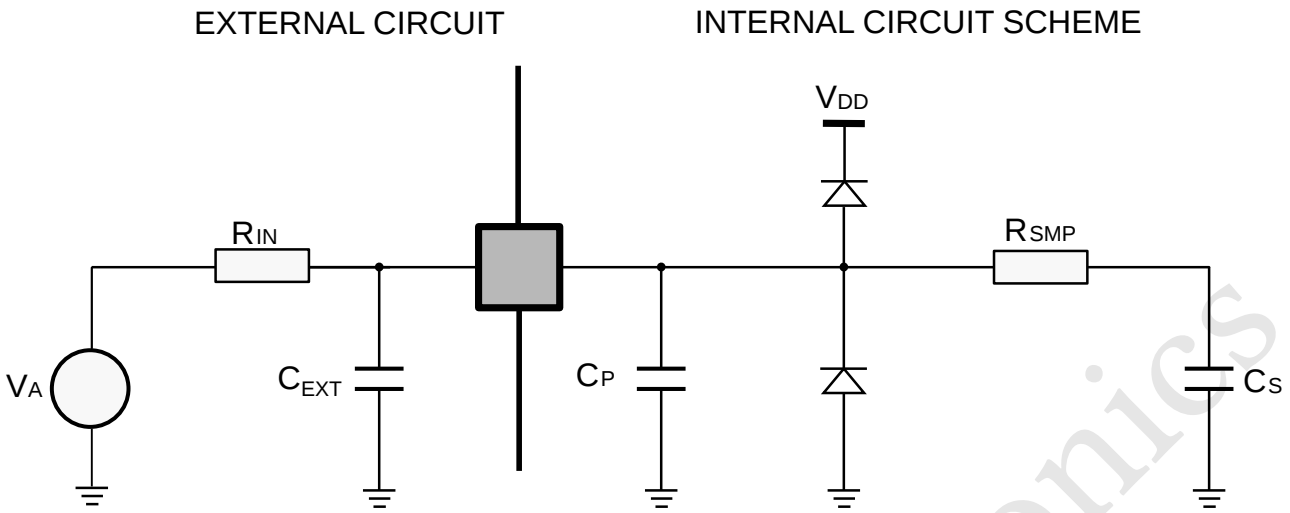
6.4.4 SIRC(2MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	2	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-3.0	–	3.0	%	
	SIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-4.0	–	4.0	%	
	SIRC frequence accuracy, factory trimmed, −40 °C – 125 °C	-5.0	–	5.0	%	
I_{SIRC}	SIRC operating current	–	23	–	μA	
$T_{Startup}$	Startup time	–	10	50	μs	

6.4.5 LPO(750Hz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{LPO}	Low power oscillator frequency	300	750	2000	Hz	

6.4.6 ADC Characteristics



Note: R_{IN} is the internal resistance of signal source.

Figure 11: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		4.9	5.0	5.1	V	
I_{DDA}	Analog supply current		–	2	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		0	–	100	mV	
V_{REFH}	Reference voltage		4.9	–	V_{DDA}	V	
I_{REFH}	Reference current		–	–	800	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		–	–	1.5	kΩ	
C_{EXT}	External capacitance		50	–	–	nF	
C_P	Pin Capacitance		–	6	–	pF	
C_S	Sampling capacitance		–	6	7	pF	

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		5	–	–	μs	
T_{SAMPLE}	Sampling time		200	–	2000	ns	
T_{sample_TS}	Tempsensor sampling time		500	–	2000	ns	

1. Theses parameters of this table can be configured by register, please refer to Reference Manual for details.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
DNL	Differential nonlinear	12-bit resolution	–	±1.0	–	LSB	
INL	Integer nonlinear	12-bit resolution	–	±2.0	–	LSB	
ACC_{TS}	Temperature sensor accuracy		-10		10	°C	
K[1]	Slope of temperature and voltage curve	ADC sampling frequncy @ 500kHz		616.9		°C / V	
F_{ADC}	ADC conversion clock		2		16	MHz	2

1. T = C - K*V, see Reference Manual for details.
2. ADC conversion clock = ADC function clock / [(ipc_divider +1) * (adc_clock_div +1)]

6.4.7 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		4.9	5.0	5.1	V	
I_{ACMP}	Analog supply current		–	20	40	μA	
$V_{INOFFSET}$	Analog input offset voltage		-10	–	10	mV	
V_{IN}	Analog input voltage		V_{SS}	–	V_{DD}	V	
V_{HYST0}	Analog comparator hysteresis 0		12	20	45	mV	
V_{HYST1}	Analog comparator hysteresis 1		24	40	85	mV	
V_{HYST2}	Analog comparator hysteresis 2		36	60	130	mV	
DAC_{DNL}	Differential nonlinear		–	±1	–	LSB	

1. ACMP connects to VDD.

6.4.8 NVM Specifications

6.4.8.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	46	50	53.5	μs	
T_{erase}	Erase execution time	4.0	4.5	5.0	ms	
T_{chip_erase}	Chip erase execution time	30	35	40	ms	

6.4.8.2 Reliability Specifications

Symbol	Description	Min.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention @25°C	20	–	years	
$t_{nvmcycp}$	Cycling endurance	100,000	–	cycles	

6.4.9 Debug Module Electrical

6.4.9.1 SWD Electrical Specifications

Table 28: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

6.4.9.2 SWD Input Clock Timing

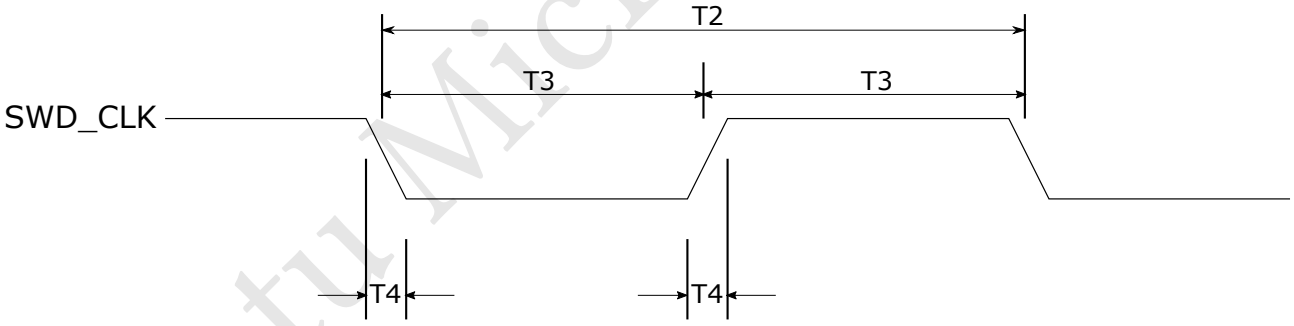


Figure 12: SWD Clock Timing

6.4.9.3 SWD Output Data Timing

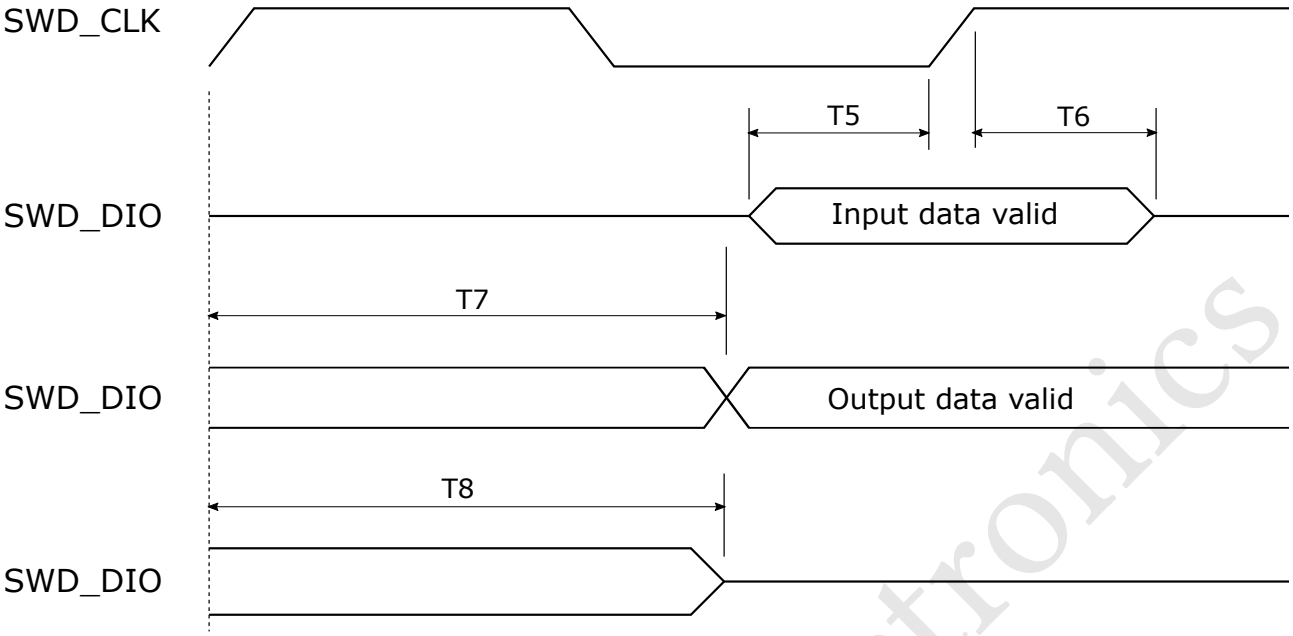


Figure 13: SWD Data Timing

6.4.10 LINPHY Specifications

Over recommended operating conditions, T_A = -40°C to 125°C (unless otherwise noted), V_{BAT}=12V.

6.4.10.1 DC Characteristics (Power Supply V_{BAT})

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{BAT}	V_{BAT} Current	Standby mode: V_{LIN} = V_{BAT}		25	49	μA
		Sleep mode: V_{LIN} = V_{BAT}		16	25	μA
		Normal mode (recessive): V_{LIN}=V_{BAT} V_{RXD}=V_{DD} V_{RSTN}=HIGH		135	1800	μA
		Normal mode (dominant): V_{BAT}=12V V_{RXD}=0 V_{RSTN}=HIGH		1.5	4.5	mA

6.4.10.2 TXD Pin

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage	V_{DD}=2.97V to 5.5V	0.3xV_{DD}		0.7xV_{DD}	V
$V_{hys(i)}$	Hysteresis voltage	V_{DD}=2.97V to 5.5V	200			mV
R_{pu}	TXD pull-up resistor		5	12	25	kΩ

6.4.10.3 RXD Pin

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{OL}	Low-level output current	Normal mode: V_{RXD}= V_{DD} -0.4V;V_{LIN}= V_{BAT}			-0.4	mA
I_{LH}	High-level leakage current	Normal mode: V_{RXD}= 0.4V;V_{LIN}= 0V	0.4			mA

6.4.10.4 EN Pin

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$V_{th(sw)}$	Switching threshold voltage		0.8		2	V
R_{pd}	Pull-down resistance		50	130	400	kΩ

6.4.10.5 RSTN Pin

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
R_{pu}	Pull-up resistance	V_{RSTN}=V_{DD}-0.4V; V_{DD}=2.97V to 5.5V	3	6	12	kΩ
I_{OL}	Low-level output current	V_{RSTN}=0.4V; V_{DD}=2.97V to 5.5V; -40°C<T_{VJ}<195°C	3.2	11	40	mA
V_{OL}	Low-level output voltage	V_{DD}=2.5V to 5.5V; -40°C<T_{VJ}<195°C	0		0.5	V
V_{OH}	High-level output voltage	-40°C<T_{VJ}<195°C	0.8xV_{DD}		V_{DD}+0.3	V

6.4.10.6 LIN Pin

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{BUS_LIM}	Driver output current limitation @dominant	V_{TXD}=0V;V_{LIN}=V_{BAT}=18V			40	mA
$I_{BUS\_PAS\_rec}$	Receiver input leakage current@ recessive	V_{TXD}=V_{DD} ;V_{LIN}= 18V; V_{BAT}=5.5V			20	μA
$I_{BUS\_PAS\_dom}$	Receiver input leakage current@ dominant	Normal mode; V_{TXD}=V_{DD}; V_{LIN}= 0V;V_{BAT}=12V	-600			μA
$V_{SerDiode}$[1]	Voltage drop on the serial diode	in pull-up path with R_{slave}, $I_{SerDiode}$=10μA	0.4		1	V
$I_{BUS\_NO\_VSS}$	Bus current @ loss ground	V_{BAT}=18V; V_{LIN}= 0V	-750		10	μA
$I_{BUS\_NO\_BAT}$	Bus current @ loss battery	V_{BAT}=0V; V_{LIN}= 18V			10	μA

Table 34 continued from previous page

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{BUSdom}	LIN receiver dominant state	V_{BAT}=5.5V to 18V			0.4 V_{BAT}	V
V_{BUSrec}	LIN receiver recessive state	V_{BAT}=5.5V to 18V	0.6 V_{BAT}			V
V_{BUS_CNT}	LIN receiver center threshold	V_{BAT}=5.5V to 18V V_{BUS_CNT}=(V_{BUSdom} + V_{BUSrec})/2	0.45 V_{BAT}	0.5 V_{BAT}	0.55 V_{BAT}	V
V_{HYS}	LIN receiver hysteresis voltage	V_{BAT}=5.5V to 18V V_{HYS}=V_{BUSrec} - V_{BUSdom}			0.175 V_{BAT}	V
R_{slave}		Resistance between LIN and V_{BAT}, LIN=0V;V_{BAT}=12V	20	30	60	kΩ
C_{LIN}[1]	Slave resistance				30	pF
$V_{O(DOM)}$	LIN dominant output	Normal mode;V_{TXD}=0V; V_{BAT}=7V			1.4	V
		Normal mode;V_{TXD}=0V; V_{BAT}=18V			2.0	V

Note
1. The test data is based on bench test and design simulation.

6.4.10.7 Duty Cycle

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$\delta 1^{1,2}$	Duty cycle 1	$V_{th(rec)(max)}$=0.744 x V_{BAT}; $V_{th(dom)(max)}$=0.581 x V_{BAT}; t_{bit}=50μs; V_{BAT}=7V to 18V	0.396			
		$V_{th(rec)(max)}$=0.76 x V_{BAT}; $V_{th(dom)(max)}$=0.593 x V_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V to 7V	0.396			
$\delta 2^{2,3}$	Duty cycle 2	$V_{th(rec)(min)}$=0.422 x V_{BAT}; $V_{th(dom)(min)}$=0.284 x V_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V to 18V			0.581	
		$V_{th(rec)(min)}$=0.41 x V_{BAT}; $V_{th(dom)(min)}$=0.275 x V_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V to 7.6V			0.581	
$\delta 3^{1,2}$	Duty cycle 3	$V_{th(rec)(max)}$=0.778 x V_{BAT}; $V_{th(dom)(max)}$=0.616 x V_{BAT}; t_{bit}=96μs; V_{BAT}=7V to 18V	0.417			
		$V_{th(rec)(max)}$=0.797 x V_{BAT}; $V_{th(dom)(max)}$=0.630 x V_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V to 7V	0.417			

Table 35 continued from previous page

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$\delta 4$[2,3]	Duty cycle 14	$V_{th(rec)(min)}$=0.389 x V_{BAT}; $V_{th(dom)(min)}$=0.251 x V_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V to 18V			0.59	
		$V_{th(rec)(min)}$=0.378 x V_{BAT}; $V_{th(dom)(min)}$=0.242 x V_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V to 7.6V			0.59	

Note

1. $\delta 1$, $\delta 3=\frac{t_{bus(rec)(min)}}{2\times t_{bit}}$
2. LIN bus load condition:
   (1) C_{BUS}=1nF, R_{BUS}=1kΩ;
   (2) C_{BUS}=6.8nF, R_{BUS}=660Ω;
   (3) C_{BUS}=10nF, R_{BUS}=500Ω
3. $\delta 2$, $\delta 4=\frac{t_{bus(rec)(max)}}{2\times t_{bit}}$

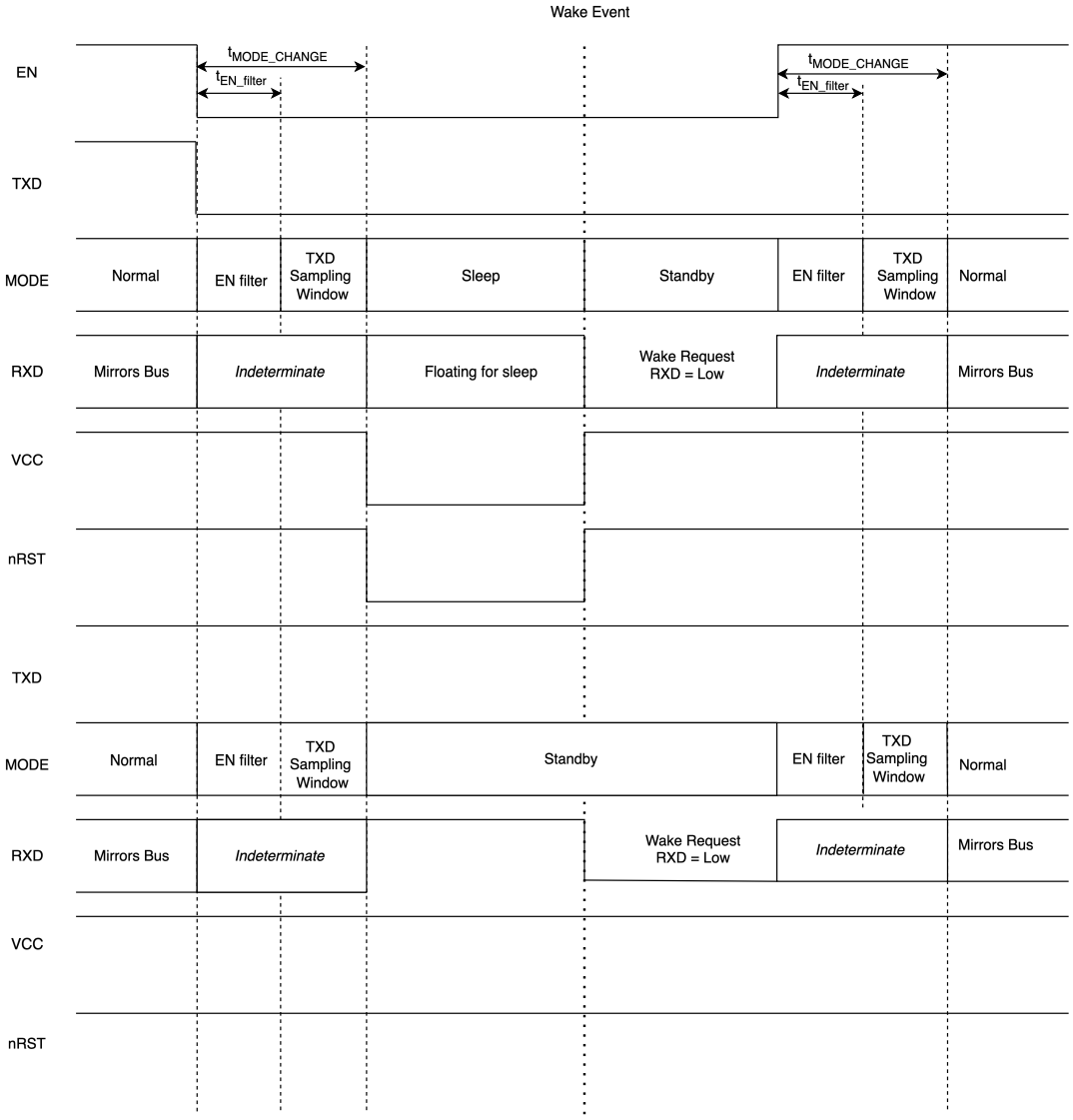
6.4.10.8 Thermal Shutdown

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$T_{th(act)otp}$[1]	Thermal shutdown temperature		165	180	195	°C
$T_{th(rel)otp}$[1]	Thermal shutdown temperature recovery		126	138	150	°C

Note:
1. The test data is based on bench test and design simulation.

6.4.10.9 Switching Characteristics

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$t_{P(RX)}$	receiver propagation delay	Riseand fall, C_{RXD}=20pF			6	μs
$t_{P(RX)sym}$	receiver propagation delay symmetry	C_{RXD}=20pF	-2		2	μs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode	30	80	150	μs
$t_{to(dom)TXD}$	TXD-dominant timeout	V_{TXD}=0V	6	13	20	ms
t_{msel}	mode select time		3	11.5	20	μs
$t_{det(UV)(VDD)}$	undervoltage detection time on pin V_{DD}	C_{RSTN}=20pF	1	8	15	μs
t_{rst}	RSTN reset time		2		8	ms



NOTE:
1. t_{EN_filter}: Enable pin setup time prior to Mode switching
2. t_{MODE_CHANGE}: Mode transition time
3. TXD Sampling Window: TXD Sampling Timing during Mode transition
4. Wake Event: Upon detecting a wake-up signal on the bus, RXD responds to the wake request by pulling low in both Standby and Sleep modes.
5. The requirements for Mode switching: The EN pin must remain stable throughout t_{MODE_CHANGE} ;
   TXD must settle its logic level before the EN pin's setup time has elapsed (within t_{EN_filter} after the EN pin transition)

Figure 14: Mode Transition

6.4.10.10 Parameter Measurement Information

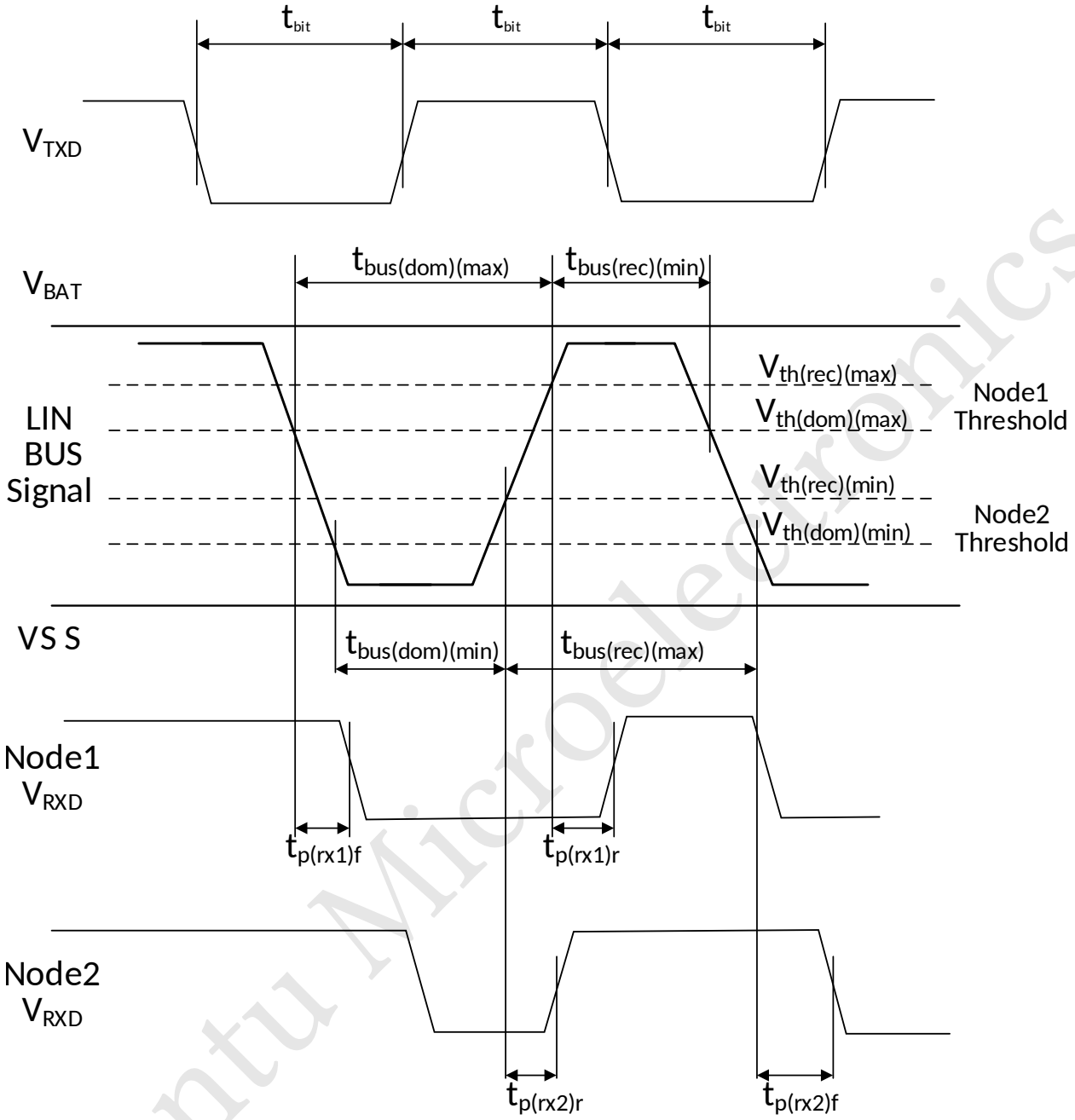
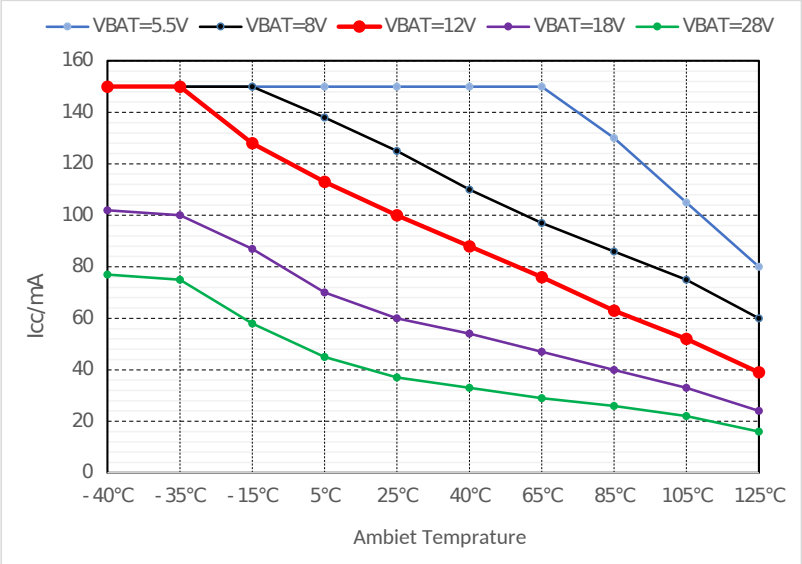


Figure 15: LIN Bus Transmission Timing Diagram



NOTE:
The power supply capability requires external PCB heat dissipation and an additional heat sink mounted on the chip's top surface. The actual current supply capacity must consider the chip's thermal derating coefficient and the practical external thermal dissipation conditions.

Figure 16: VDD Power Supply Current Capability Derating Curve

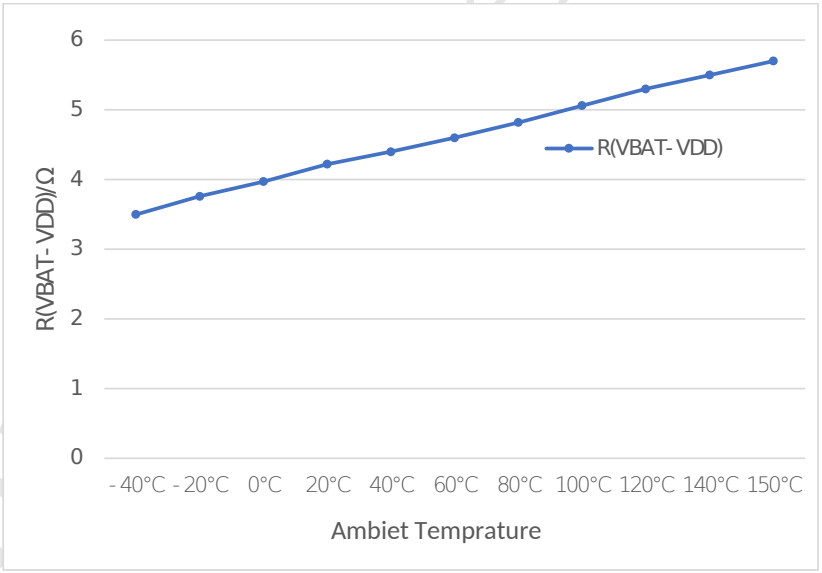


Figure 17: R(VBAT-VDD) Typical values VS. Temperature Changes

6.5 Thermal Attributes

Table 38: Thermal Characteristics

Package Family	Package Type	Thermal Resistance		Unit
		R_{JA}	R_{JC}	
QFN	QFN48L	30	9	°C/W

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 39: Pinmux Table

48QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	PTD_1	-	PTD_1	eTMR0_CH3	SPI1_SIN	-	I2C1_SCL	-	TMU_OUT2
2	PTD_0	-	PTD_0	eTMR0_CH2	SPI1_SCK	-	I2C1_SDA	-	TMU_OUT1
3	PTE_5	-	PTE_5	TCLK_IN2	-	eTMR1_CH1	CAN0_TX	-	-
4	PTE_4	-	PTE_4	CCM_CLKOUT	-	eTMR1_CH0	CAN0_RX	-	-
5	VDD VDDA VREFH	VDD VDDA VREFH	-	-	-	-	-	-	-
6	VBAT	-	-	-	-	-	-	-	-
7	VSS	VSS	-	-	-	-	-	-	-
8	EN	-	-	-	-	-	-	-	-
9	LIN	-	-	-	-	-	-	-	-
10	RSTN	-	-	-	-	-	-	-	-
11	TXD	-	-	-	-	-	-	-	-
12	RXD	-	-	-	-	-	-	-	-
13	PTB_7	EXTAL	PTB_7	I2C0_SCL	-	UART2_TX	-	-	TMU_OUT2
14	PTB_6	XTAL	PTB_6	I2C0_SDA	-	UART2_RX	-	-	TMU_OUT1
15	PTD_16	EXTAL32K	PTD_16	eTMR0_CH1	-	SPI0_SIN	ACMP0_ACTIVE	-	-
16	PTD_15	XTAL32K	PTD_15	eTMR0_CH0	-	SPI0_SCK	-	-	-
17	PTB_5	-	PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	CCM_CLKOUT	TMU_IN0	-
18	PTB_4	-	PTB_4	eTMR0_CH4	SPI0_SOUT	-	-	TMU_IN1	-
19	PTC_1	ADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT	SPI2_SIN	-	eTMR1_CH7	-
20	PTC_16	ADC0_SE14	PTC_16	eTMR1_FLT2	-	SPI2_SCK	-	-	-
21	PTC_15	ADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK	SPI2_SOUT	-	TMU_IN8	-
22	PTC_14	ADC0_SE12	PTC_14	eTMR1_CH2	-	SPI2_PCS0	-	TMU_IN9	-
23	PTB_3	ADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	-	TMU_IN2	-
24	PTB_2	ADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	-	TMU_IN3	-
25	PTB_1	ADC0_SE5	PTB_1	UART0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	-	-
26	PTB_0	ADC0_SE4	PTB_0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	-	-
27	PTC_9	-	PTC_9	UART1_TX	eTMR1_FLT1	-	-	UART0_RTS	-
28	PTC_8	-	PTC_8	UART1_RX	eTMR1_FLT0	-	-	UART0_CTS	-
29	PTA_7	ADC0_SE3	PTA_7	eTMR0_FLT2	-	RTC_CLKIN	-	UART1_RTS	-
30	PTA_6	ADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1	-	-	UART1_CTS	-
31	PTE_7	-	PTE_7	eTMR0_CH7	SPI1_PCS2	-	-	-	-
32	PTB_13	-	PTB_13	eTMR0_CH1	-	-	-	-	-
33	PTD_3	-	PTD_3	-	SPI1_PCS0	I2C1_SCL	eTMR2_CH0	TMU_IN4	CORE_NMI_b
34	PTD_2	-	PTD_2	-	SPI1_SOUT	I2C1_SDA	eTMR2_CH1	TMU_IN5	-
35	PTA_3	-	PTA_3	eTMR2_CH0	I2C0_SCL	SPI2_SCK	-	UART0_TX	-
36	PTA_2	-	PTA_2	eTMR2_CH1	I2C0_SDA	SPI2_SIN	-	UART0_RX	-
37	PTA_1	ADC0_SE1 ACMP0_IN1	PTA_1	eTMR1_CH1	-	SPI2_SOUT	eTMR1_QD_PHA	UART0_RTS	TMU_OUT0
38	PTA_0	ADC0_SE0 ACMP0_IN0	PTA_0	eTMR1_CH0	-	SPI2_PCS0	-	UART0_CTS	TMU_OUT3
39	PTC_7	-	PTC_7	UART1_TX	-	SPI2_PCS1	CAN0_TX	eTMR1_QD_PHA	-
40	PTC_6	-	PTC_6	UART1_RX	-	-	CAN0_RX	eTMR1_QD_PHB	-
41	PTA_13	-	PTA_13	eTMR1_CH7	-	-	UART2_TX	-	-
42	PTA_12	-	PTA_12	eTMR1_CH6	-	-	UART2_RX	-	-

Table 39 continued from previous page

48QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
43	PTA_11	-	PTA_11	eTMR1_CH5	-	I2C1_SCL	ACMP0_ACTIVE	-	-
44	PTA_10	-	PTA_10	eTMR1_CH4	-	I2C1_SDA	-	-	-
45	VDD15	-	VDD15	-	-	-	-	-	-
46	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT	-	-	eTMR1_QD_PHB	SWD_CLK
47	PTA_5	-	PTA_5	-	TCLK_IN1	-	-	-	RCU_RESET_b
48	PTA_4	-	PTA_4	-	-	ACMP0_OUT	-	-	SWD_IO

7.2 Packages

The information of package pinouts is as follows:

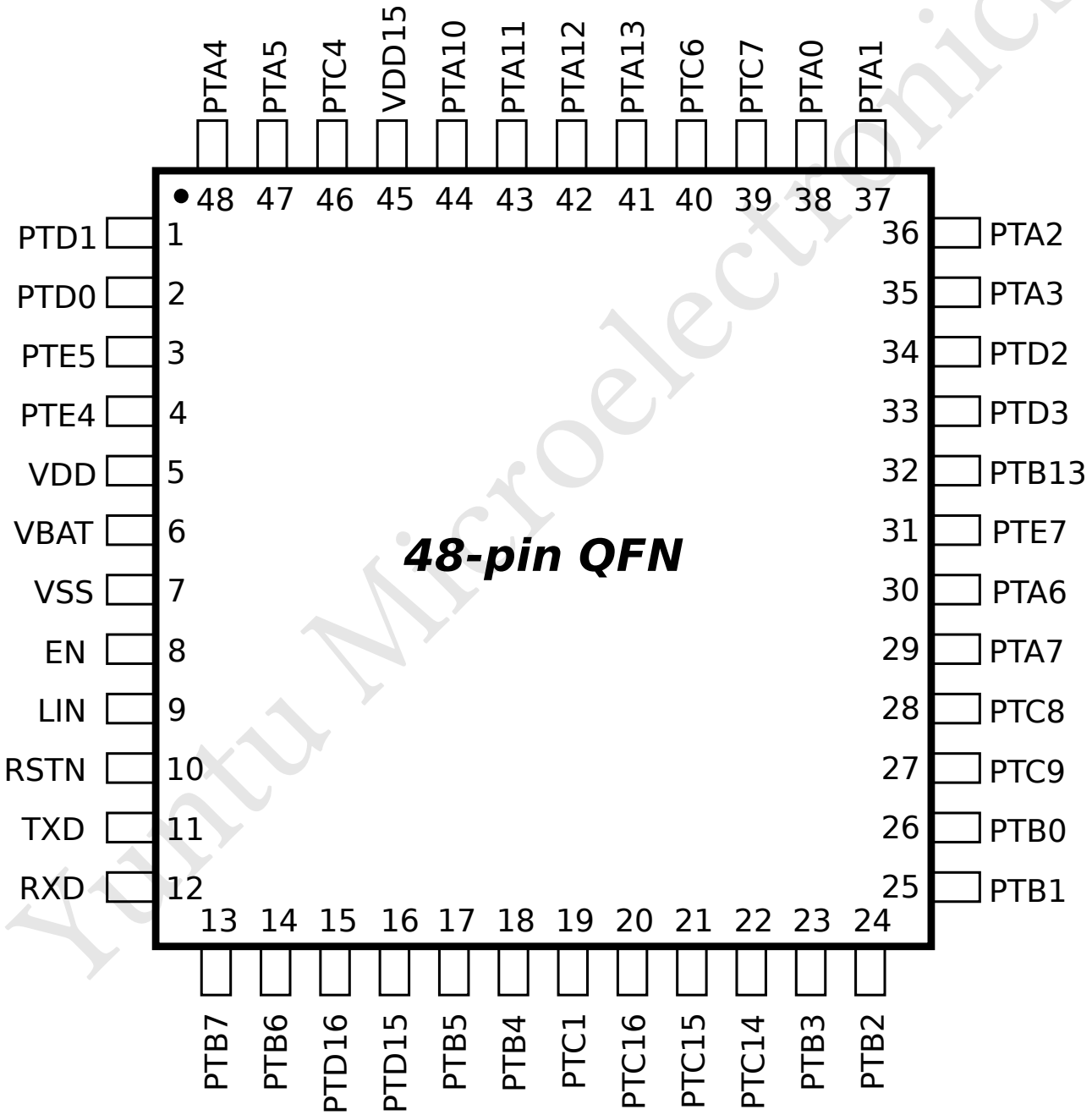
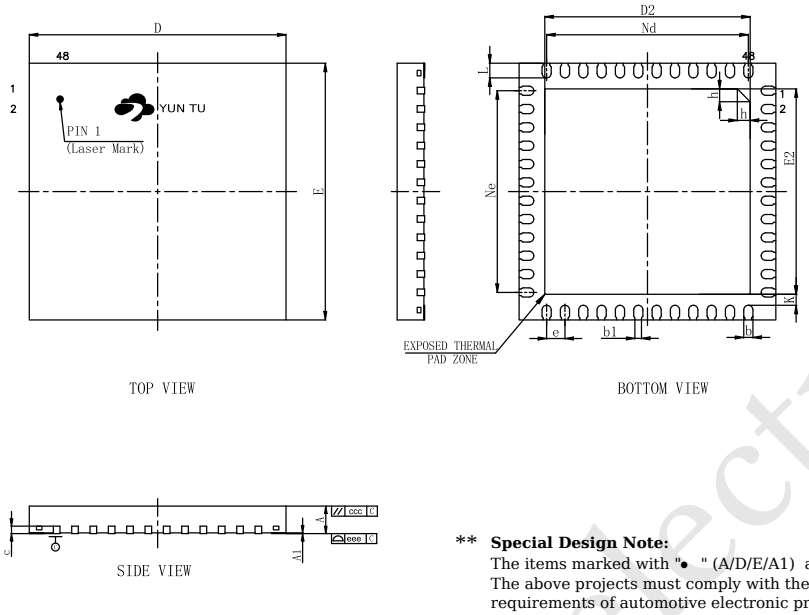


Figure 18: 48-pin QFN Package

Note: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
• A	0.80	0.85	0.90
• A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
• D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e	0.50BSC		
Ne	5.50BSC		
Nd	5.50BSC		
• E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.30REF		
ccc	0.10		
eee	0.08		

** **Special Design Note:**
The items marked with "• " (A/D/E/A1) are key characteristics.
The above projects must comply with the management and control requirements of automotive electronic projects.

Figure 19: 48pin QFN

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2024/4/22	Initial version
1.1	2024/5/16	Changed the value of I_{LAT} from "±100" to "±50" @125 °C, from "±200" to "±100" @25 °C in "ESD Handling Ratings" Changed the Max value of I_{BUS_LIM} from "125" to "40" and removed the Min value of this symbol in "LIN Pin" Updated the Figure of 48pin QFN in "Dimensions"
1.2	2025/4/3	Corrected "AEC-Q100 qualified" to "QM compliant" in chapter of 'Features' Added Min and Max value in subsection of 'Moisture Handling Ratings' Updated Min and Max value in subsection of 'ESD Handling Ratings' Updated Max value of I_{VDD} in subsection of 'Absolute Maximum Ratings' Updated Min and Max value in subsection of 'Voltage and Current Operating Requirements' Updated Min and Max value in subsection of 'DC Electrical Specifications at 3.3V' Updated Min and Max value in subsection of 'DC Electrical Specifications at 5.0V' Added Min and Max value in subsection of 'Power and Ground Pins' Removed the subsection of 'POR,LVR and LVD Operating Requirements(V_{DD})' Updated the table in subsection of 'Power Mode Transition Operating Behaviors' Added Min and Max value in subsection of 'Power Consumption' Added the whole subsection of 'Power Supply Fluctuation Requirements' Added Min and Max value in subsection of 'FXOSC(4-40MHz) Characteristics' Updated the value of table in subsection of 'FIRC(48MHz) Characteristics' Added Min and Max value in subsection of 'SXOSC(32.768KHz) Characteristics' Updated the value of table in subsection of 'SIRC(2MHz) Characteristics' Added Min and Max value in subsection of 'LPO(750Hz) Characteristics' Added Min and Max value in subsection of 'ADC Characteristics' Added Min and Max value in subsection of 'ACMP Characteristics' Removed the subsubsection of 'Flash High Voltage Current Behaviors' Added mode transition figure in subsubsection of 'Switching Characteristics' Added power supply current capability derating curve in subsubsection of 'Parameter Measurement Information' Added R_{JC} information in section of 'Thermal Attributes'

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