



ZHEJIANG UNI-NE Technology CO., LTD

浙江宇力微新能源科技有限公司



U1001A Data Sheet

V 1.3

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Independent Single-Channel Gate Driver

General Description

The U1001A is a single channel MOSFET and IGBT driver with dependent low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard MOS or LSTTL output, down to 3.3V logic. Internal integrated input logic signal processing circuit, SD fast shutdown processing circuit and high current output driver circuit. The 1001A can be used to drive an N-channel power MOSFET or IGBT which operates up to 30 volts.

Key Features

- Built IN SD Function
- Gate drive supply range from 5 to 30V
- Undervoltage lockout
- 3.3V, 5V input logic compatible
- output in phase with input

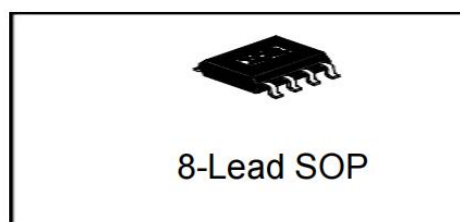
Applications

- General Purpose Gate Driver
- DC-DC converters
- Plasma display panel (PDP) applications

Product Summary

V _{OFFSET}	30V max
I _{O+/-}	2.0 A / 2.5A
V _{CC}	5V - 30V
Work Tem	-40 ~125°C

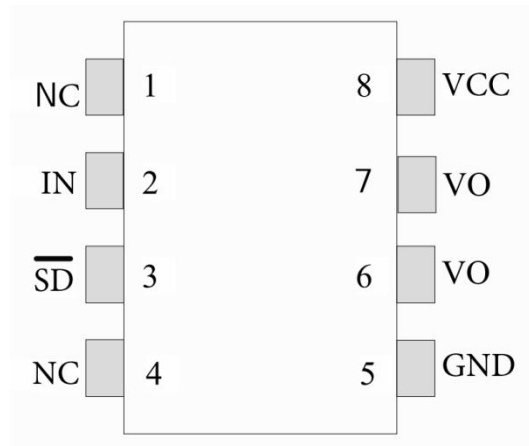
Packages



Products Information

Base Part Number	Package Type	Standard OUT		V _{OFFSET}	Logic Control
		IO+	IO-		
U1001A	SOP8	2.0A	2.5A	30V	IN & $\overline{\text{SD}}$

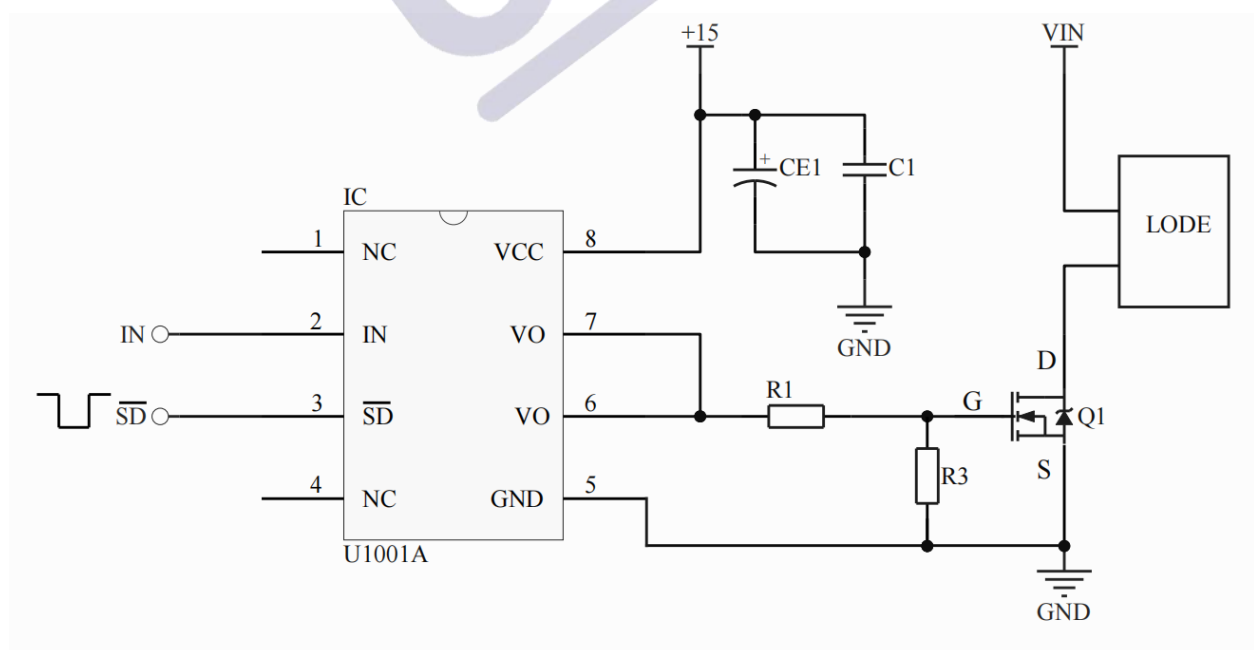
Pin Assignments



Pin Function

Number	Symbol	Description
1, 4	NC	Suggested overhang
2	IN	Logic input
3	$\overline{\text{SD}}$	Logic input for shutdown
5	GND	Ground
6, 7	VO	Gate drive output
8	VCC	Power supply

Typical Application



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
VCC	Low side and logic fixed supply voltage	-0.3	35	V
VO	Gate drive output voltage	-0.3	35	
VIN	Logic input voltage (IN)	-0.3	35	
$\overline{SD}$	Logic input voltage ($\overline{SD}$)	-0.3	7	
dVS/dt	Allowable offset supply voltage transient	—	50	V/ns
P _D	Package power dissipation @ TA ≤ +25°C	—	0.625	W
RthJA	Thermal resistance, junction to ambient	—	200	°C/W
TJ	Junction temperature	—	150	°C
TS	Storage temperature	-55	150	
TL	Lead temperature (soldering, 10 seconds)	—	300	

Electrical Characteristic

VCC = 15V, CL = 1000pF, TA = 25°C, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
ton	Turn-on propagation delay	—	320	400	ns	
toff	Turn-off propagation delay	—	200	260		
tsd	Shutdown propagation delay	—	160	—		
tr	Turn-on rise time	—	20	50		
tf	Turn-off fall time	—	18	48		

Electrical Characteristic

VCC = 15V , TA = 25°C , unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{CCUV+}	VCC supply under-voltage positive going threshold	—	4.8	—	V	
V _{CCUV-}	VCC supply under-voltage negative going threshold	—	4.5	—		
V _{CCHYS}	VCC supply under-voltage lockout hysteresis	—	0.3	—		
VIH	Logic “1” (HO) & Logic “0” (LO) input voltage	3	—	—	V	VCC = 5V to 20V
VIL	Logic “0” (HO) & Logic “1” (LO) input voltage	—	—	0.8		VCC = 5V to 20V
IIN+	Logic “1” input bias current	—	20	50	uA	
IIN-	Logic “0” input bias current	—	—	1		
VSD	SD input positive going threshold	—	—	0.8	V	VCC = 5V to 20V
VSD	SD input negative going threshold	3	—	—		VCC = 5V to 20V
VO	Low level output voltage, VO	—	—	100	mV	IO = 0A
IQCC	Quiescent VCC supply current	—	100	—	uA	VIN = 0V or 5V
IO+	Output high short circuit pulsed current	—	2.0	—	A	VO=0V PW≤10μs
IO-	Output low short circuit pulsed current	—	2.5	—		VO=15V PW≤10μs

Time waveform

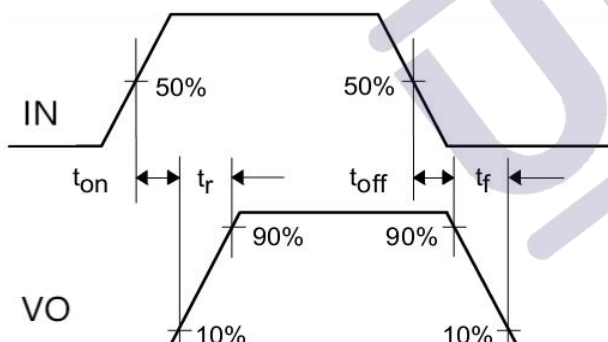


Figure 1. Switching Time Test Circuit

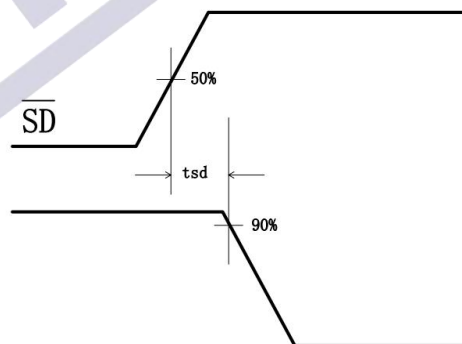


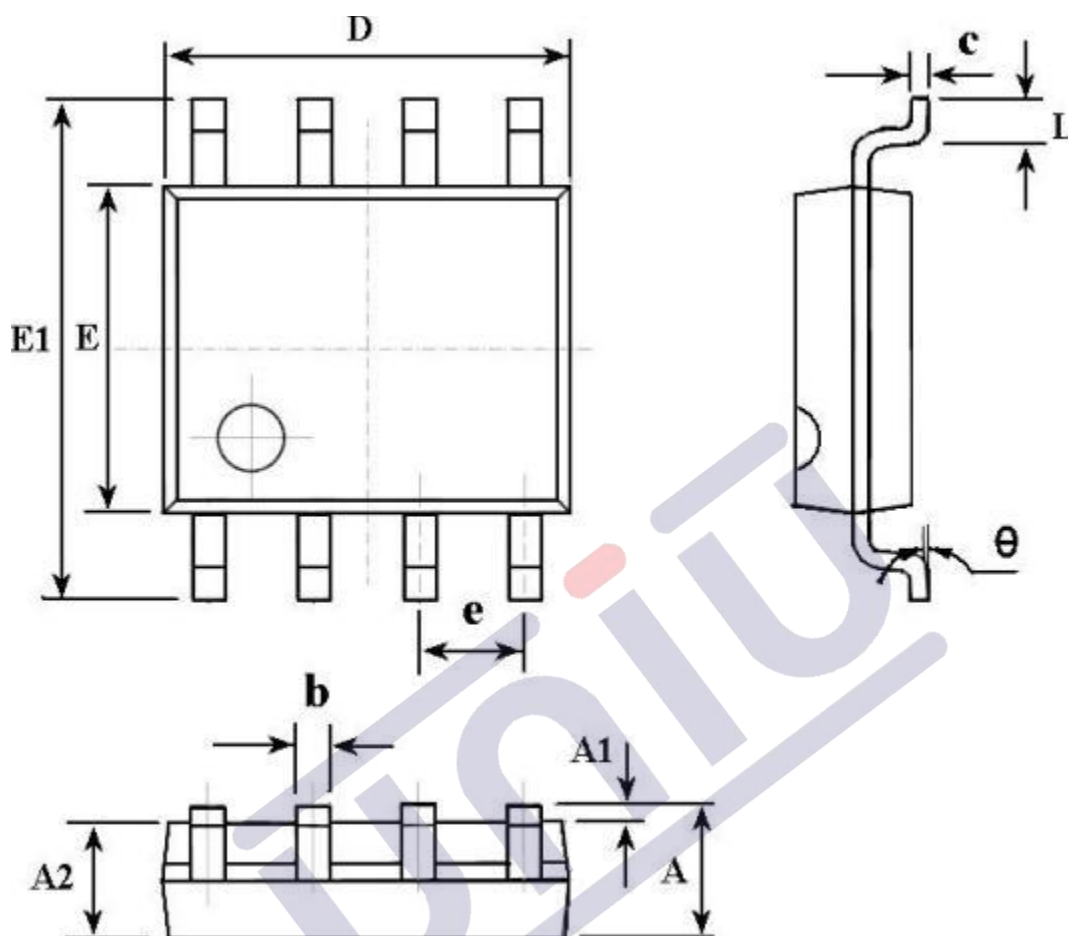
Figure 2. Switching Time Waveform Definitions

Truth Table

IN	$\overline{SD}$	VO	logic diagram
0	0	0	
0	1	0	
1	0	1	
1	1	0	

Packaging information

SOP 8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.127(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

1、版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	首次发布
2020/05/21	1.1	变更封装
2023/3/18	1.2	参数调整
2024/4/26	1.3	优化逻辑图及真值表

2、联系我们

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