



ZHEJIANG UNIU-NE Technology CO., LTD

浙江宇力微新能源科技有限公司



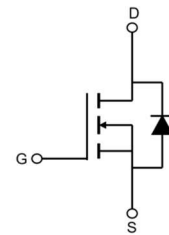
AP40N100K Data Sheet

V 1.1

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Feature

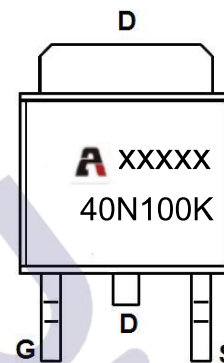
- 100V,40A
 $R_{DS(ON)} < 23m\Omega$ @ $V_{GS}=10V$ (TYP:18m Ω)
 $R_{DS(ON)} < 33m\Omega$ @ $V_{GS}=4.5V$ (TYP:25m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
40N100K	AP40N100K	TO-252	13 Inch	-	2500

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_c = 25^\circ\text{C}$)	I_D	40	A
Continuous Drain Current ($T_c = 100^\circ\text{C}$)	I_D	25	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	120	A
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	64	mJ
Power Dissipation	P_D	50	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.65	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~ +150	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^{\circ}\text{C}$ unless otherwise noted)

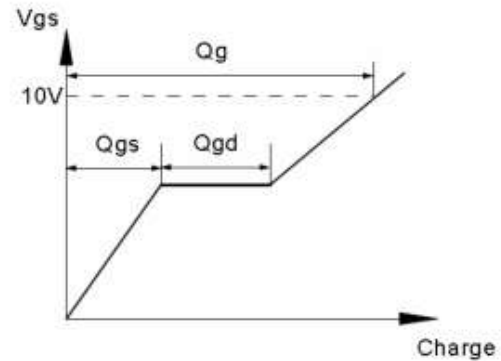
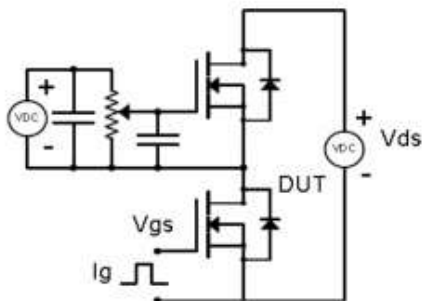
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =100V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage ⁽³⁾	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.8	V
Drain-source on-resistance ⁽³⁾	R _{DS(on)}	V _{GS} =10V, I _D =15A	-	18	23	mΩ
		V _{GS} =4.5V, I _D =10A	-	25	33	mΩ
Forward Threshold Voltage	g _{fs}	V _{DS} =10V, I _D =20A	-	22	-	S
Gate Resistance	R _g	V _{DS} =V _{GS} =0V, f =1MHz	-	1.62	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iSS}	V _{DS} =50V, V _{GS} =0V, f =1MHz	-	822	-	pF
Output Capacitance	C _{oSS}		-	310	-	
Reverse Transfer Capacitance	C _{rSS}		-	23.5	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =50V, I _D =20A, V _{GS} =10V, R _G =3Ω	-	15	-	ns
Turn-on rise time	t _r		-	3.2	-	
Turn-off delay time	t _{d(off)}		-	30	-	
Turn-off fall time	t _f		-	7.6	-	
Total Gate Charge	Q _g	V _D S=50V, I _D =20A, V _G S=10V	-	22.7	-	nC
Gate-Source Charge	Q _{gs}		-	6.2	-	
Gate-Drain Charge	Q _{gd}		-	5.3	-	
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=100A/us		31		nC
Reverse Recovery Time	T _{rr}	I _F =20A, di/dt=100A/us		34		ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V _{DS}	V _{GS} =0V, I _S =10A	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I _S		-	-	40	A

Notes:

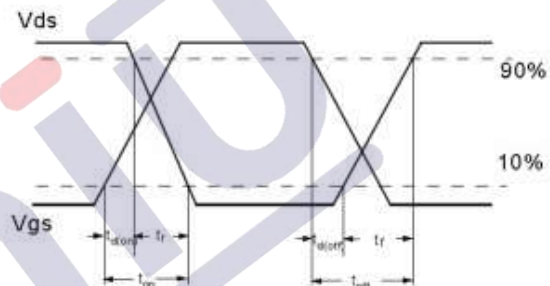
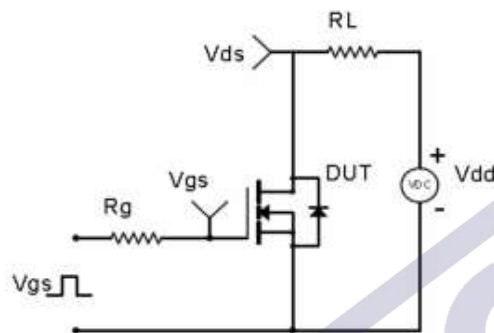
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^{\circ}\text{C}, V_{DD} = 50V, R_G = 25\Omega, L = 0.5\text{Mh}$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$

Test Circuit & Waveform

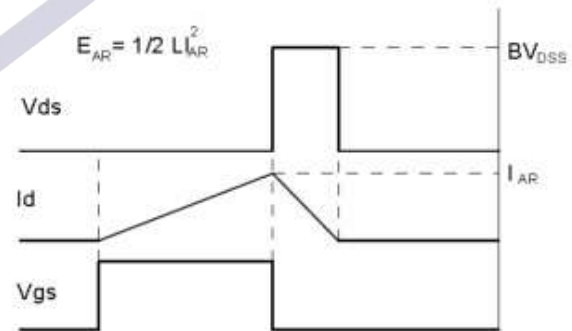
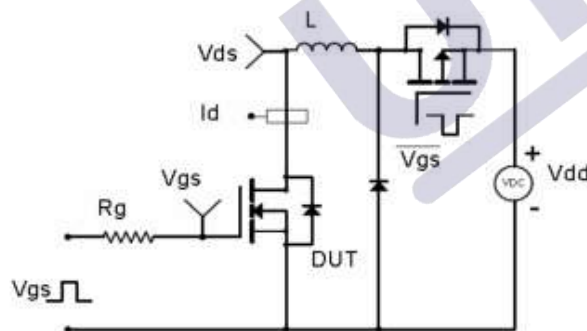
Gate Charge Test Circuit & Waveform



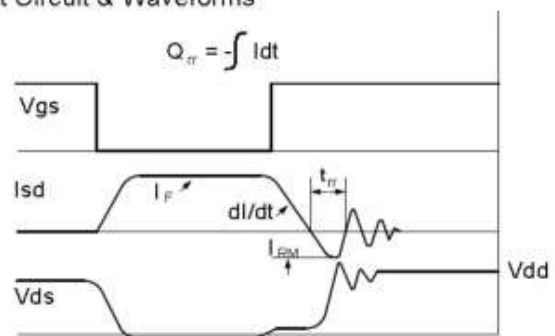
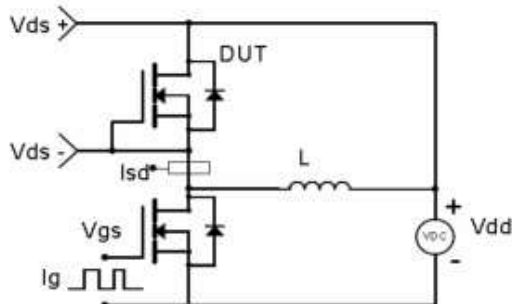
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Performance Characteristics

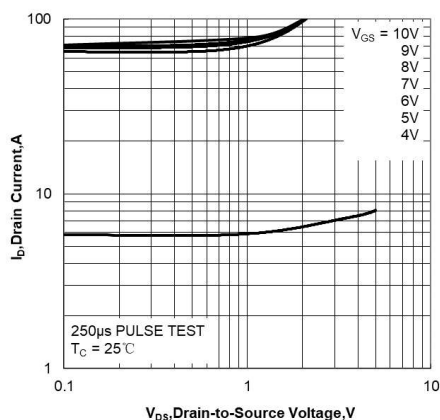


Figure 1. Output Characteristics

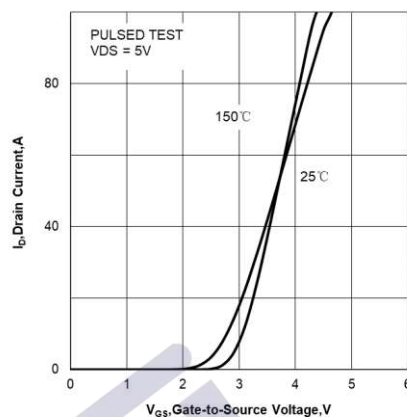


Figure 2. Transfer Characteristics

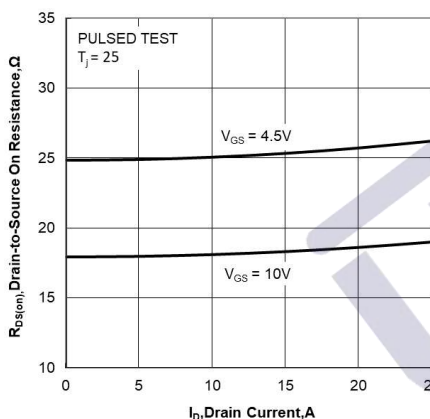
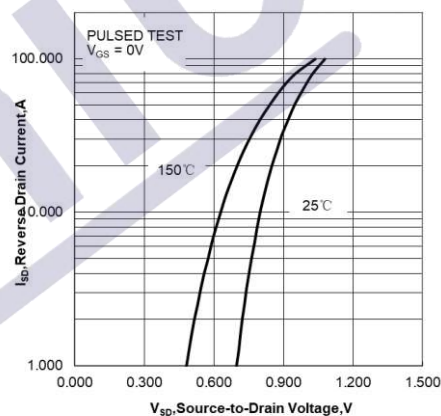
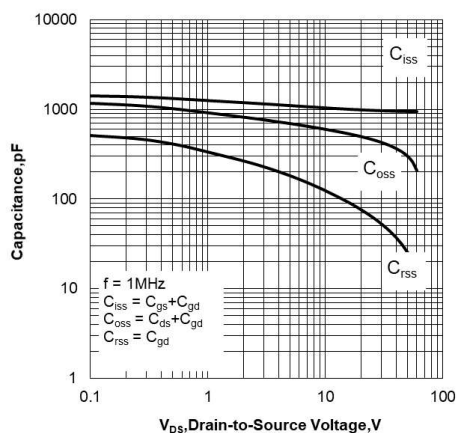
Figure 3. Drain-to-Source On Resistance
vs Drain CurrentFigure 4. Body Diode Forward Voltage
vs Source Current and Temperature

Figure 5. Capacitance Characteristics

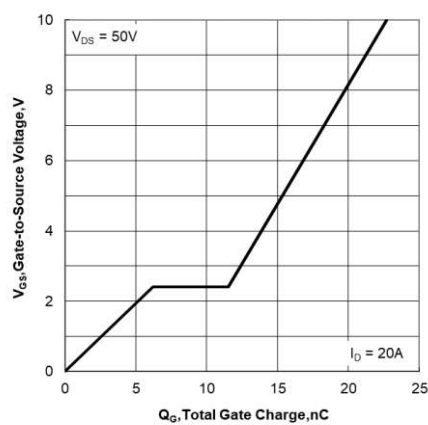


Figure 6. Gate Charge Characteristics

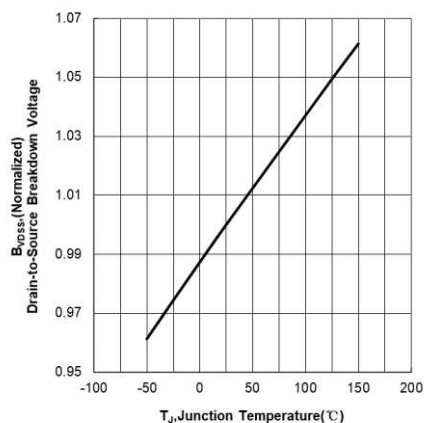


Figure 7. Normalized Breakdown Voltage
vs Junction Temperature

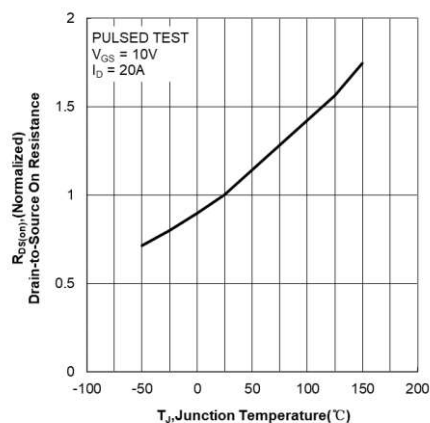


Figure 8. Normalized On Resistance vs
Junction Temperature

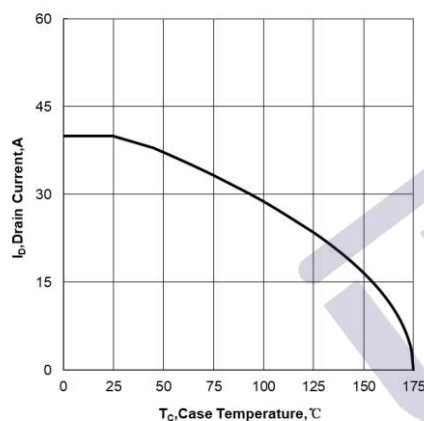


Figure 9. Maximum Continuous Drain Current
vs Case Temperature

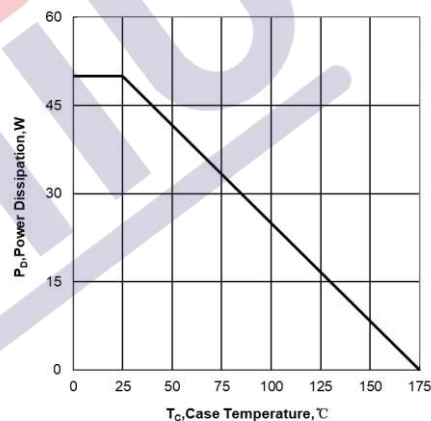


Figure 10. Maximum Power Dissipation
vs Case Temperature

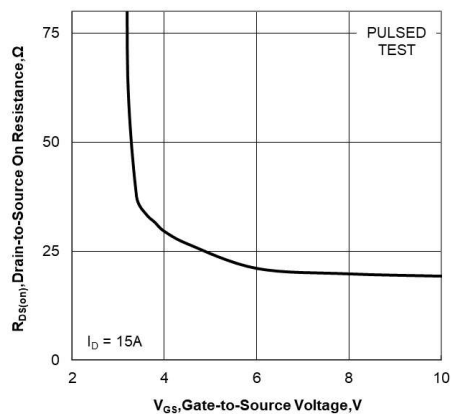


Figure11. Drain-to-Source On Resistance vs Gate
Voltage and Drain Current

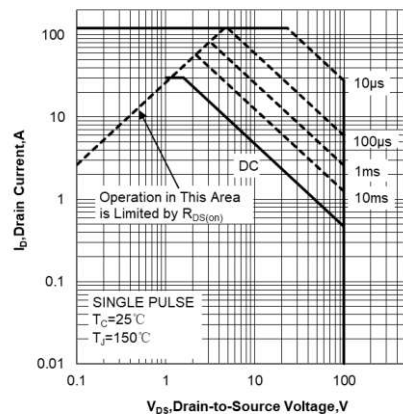


Figure 12. Maximum Safe Operating Area

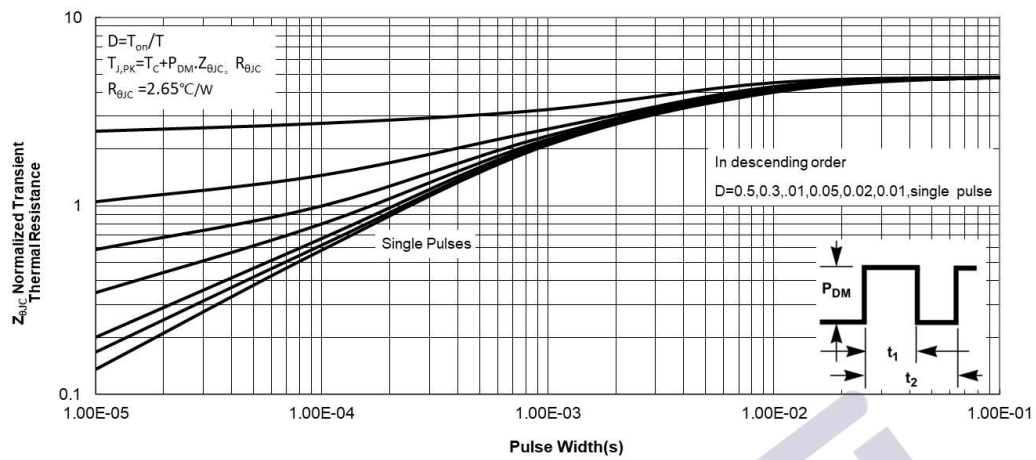
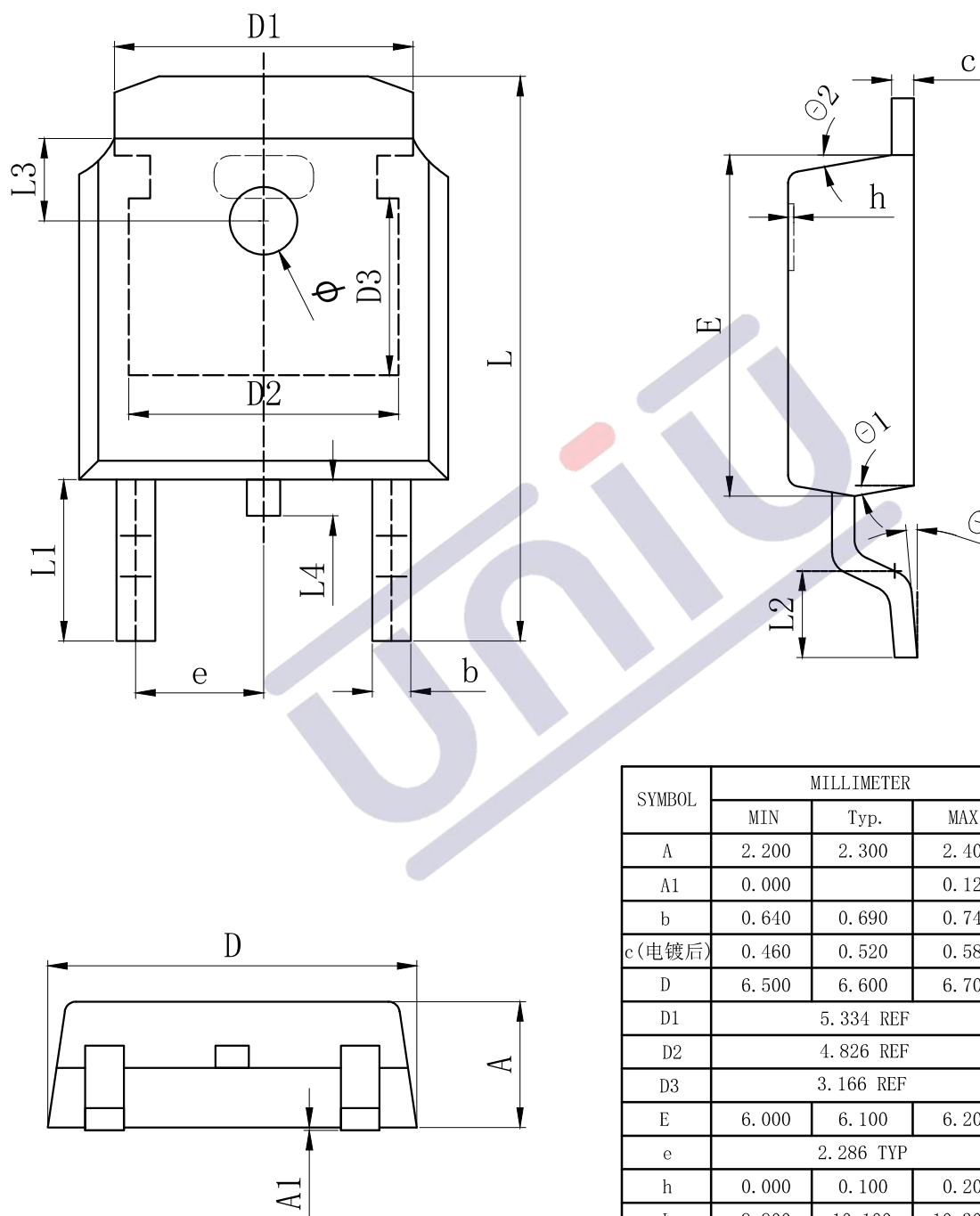


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-252 Package Information



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	2.200	2.300	2.400
A1	0.000		0.127
b	0.640	0.690	0.740
c (电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	4.826 REF		
D3	3.166 REF		
E	6.000	6.100	6.200
e	2.286 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.888 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.600	0.800	1.000
Φ	1.100	1.200	1.300
θ	0°		8°
θ 1	9° TYP		
θ 2	9° TYP		

1.版本记录

DATE	REV.	DESCRIPTION
2018/11/15	1.0	First Release
2020/09/18	1.1	Layout adjustment

2.免责声明

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