



UNI-SEMICONDUCTOR CO., LTD

宇力半导体有限公司



U3215-6 Data Sheet

V 3.1

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High Current IO+/- 2.0/2.5A HALF-BRIDGE DRIVER

General Description

The U3215/U3216 Fully operated to +600V is high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels.

The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Product Summary

V _{OFFSET}	600V max
IO+/-	2.0 A / 2.5A
VCC	3V - 20V
ton/off (typ.)	220 & 120ns
Deadtime (typ.)	100 ns
Work Tem	-40 ~125 °C

Key Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 3 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels

Applications

- Home appliances
- Industrial applications and drives
- Motor drivers
- DC, AC, PMDC and PMAC motors
- Induction heating
- HVAC

Packages

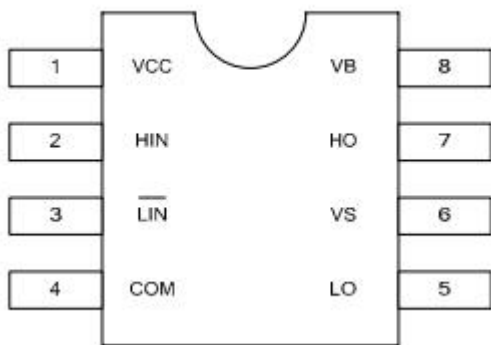


8-Lead SOP

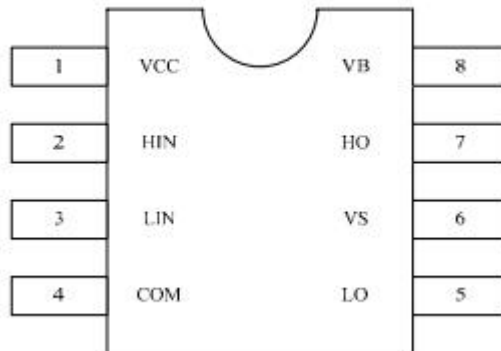
Products Information

Base Part Number	Package Type	Standard OUT		V _{OFFSET}	Logic Control
		IO+	IO-		
U3215	SOP8	2.0A	2.5A	600V	HIN & $\overline{\text{LIN}}$
U3216	SOP8	2.0A	2.5A	600V	HIN & LIN

Pin Assignments



U3215

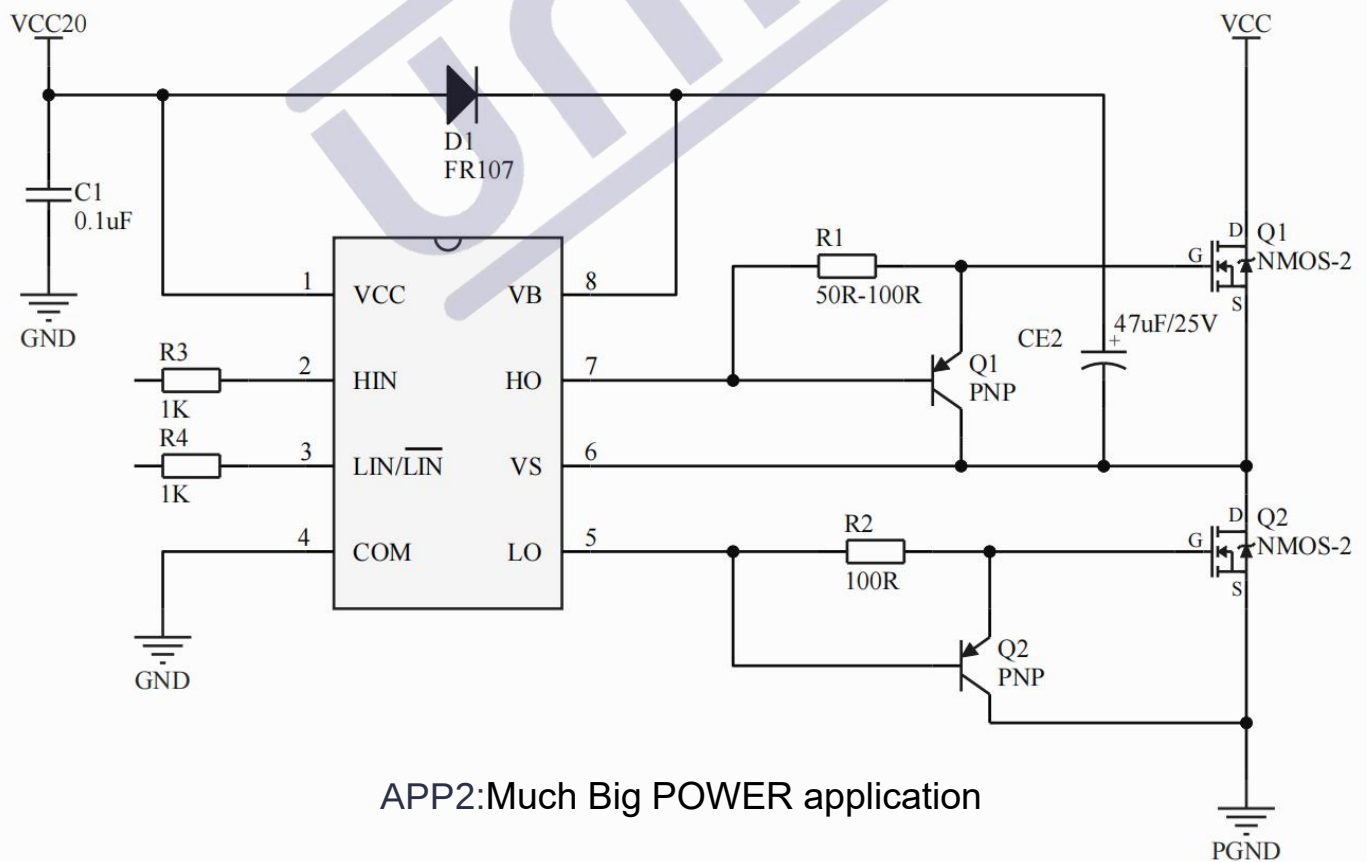
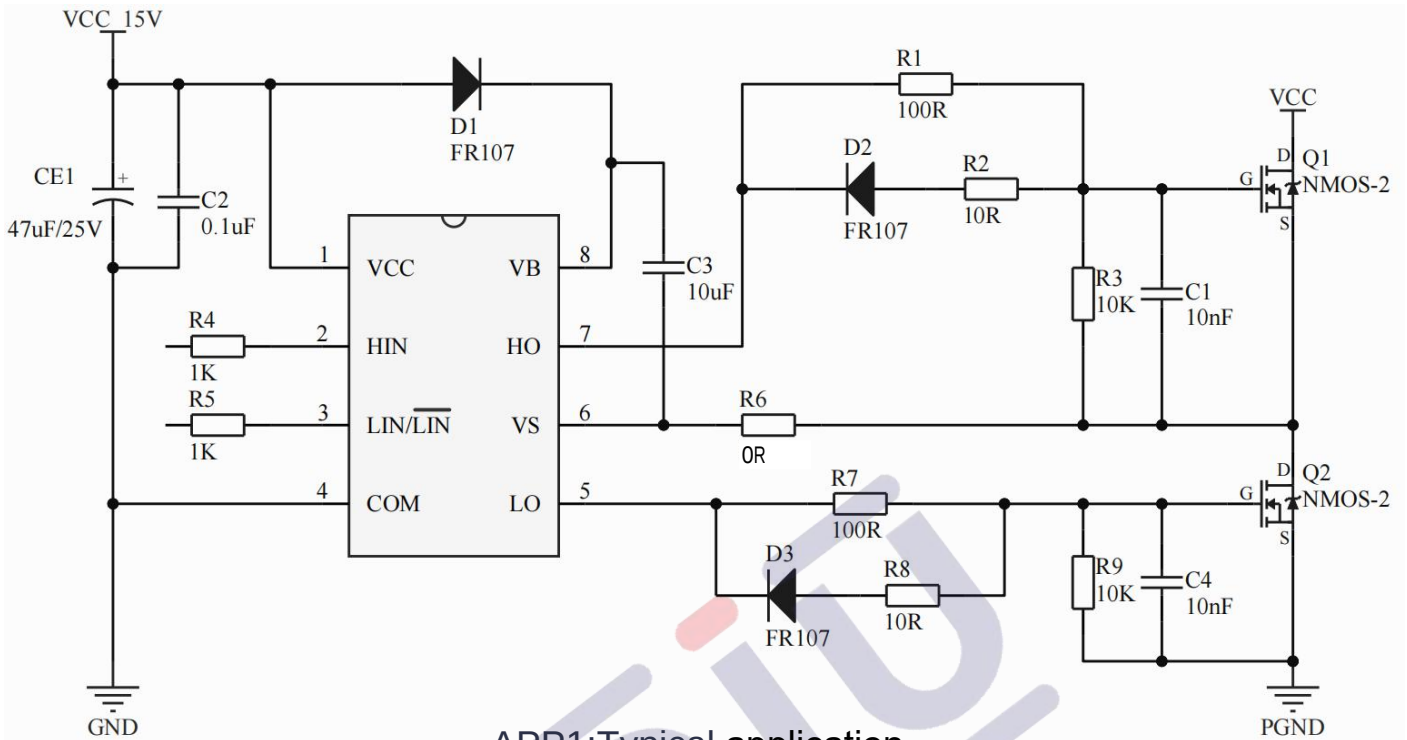


U3216

Pin Function

Number	Symbol	Type	Description
1	VCC	P	Low side and logic fixed supply
2	HIN	I	Logic input for high side gate driver outputs (HO), in phase
3	LIN	I	Logic input for low side gate driver outputs (LO), in phase
	$\overline{\text{LIN}}$	I	Logic input for low side gate driver outputs (LO), out of phase
4	COM	P	Low side return
5	LO	O	Low side gate drive output
6	VS	P	High side floating supply return
7	HO	O	High side gate drive output
8	VB	P	High side floating supply

Typical Connection



NOTE: For the by default, common operating under high pressure conditions or operating against negative pressure, this resistor can be increased. The recommended value range is 1 to 3R.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
VB	High side floating absolute voltage	-0.3	625	V
VS	High side floating supply offset voltage	VB-25	VB+0.3	
VHO	High side floating output voltage	VS-0.3	VB+0.3	
VLO	Low side output voltage	-0.3	Vcc+0.3	
Vcc	Low side and logic fixed supply voltage	-0.3	25	
VIN	Logic input voltage (HIN & LIN)	-0.3	Vcc+0.3	
dVS/dt	Allowable offset supply voltage transient	—	55	V/ns
P _D	Package power dissipation @ TA ≤ +25°C , DIP-8	—	1	W
	Package power dissipation @ TA ≤ +25°C , SOIC-8	—	0.625	
RthJA	Thermal resistance, junction to ambient , DIP-8	—	125	°C/W
	Thermal resistance, junction to ambient , SOIC-8	—	200	
TJ	Junction temperature	—	150	°C
TS	Storage temperature	-55	150	
TL	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	VS + 3	VS + 20	V
VS	High side floating supply offset voltage	-6(Note1)	600	
VHO	High side floating output voltage	VS	VB	
VLO	Low side output voltage	0	VCC	
VCC	Low side and logic fixed supply voltage	3.0	20	
VIN	Logic input voltage (HIN&LIN)	0	VCC	
TA	Ambient temperature	-40	125	°C

Note1: Logic operational for VS of -6 to +600V. Logic state held for VS of -6V to -VBS.

Electrical Characteristic

$V_{CC} = V_{BS} = V_{BIAS} = 15V$, $CL=1000pF$, $TA = 25^{\circ}C$, unless otherwise specified.

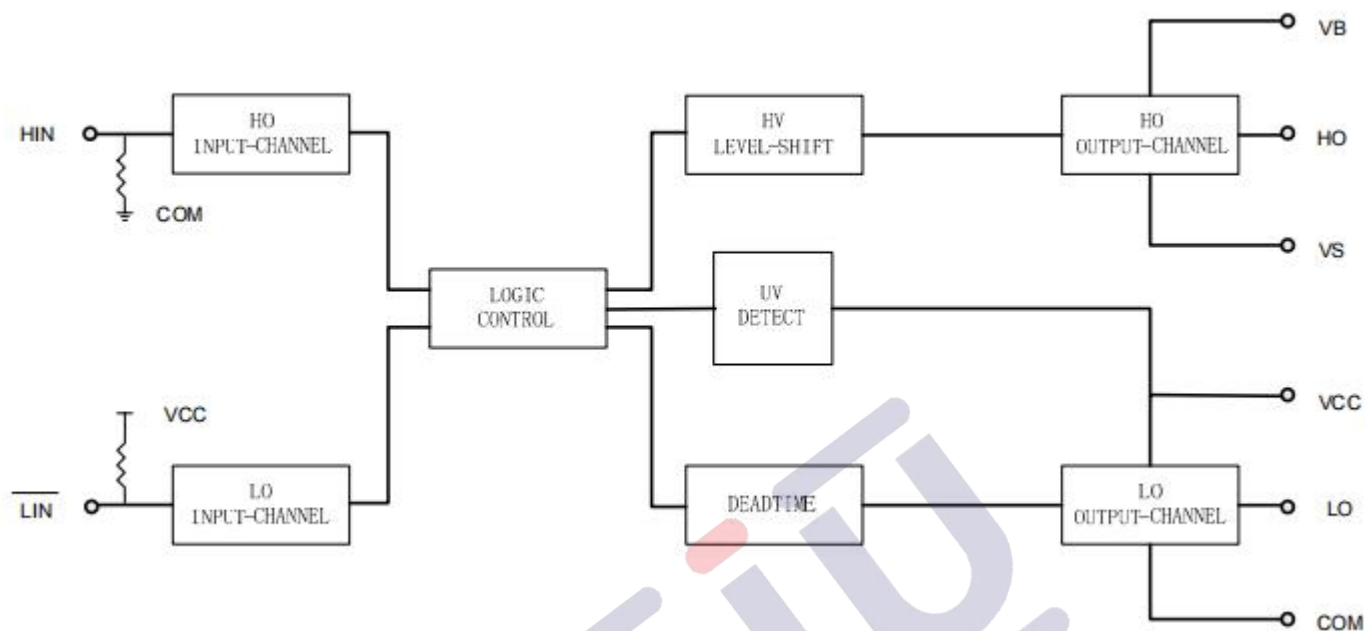
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_r	Turn-on rise time	—	72	120	ns	
t_f	Turn-off fall time	—	15	45		
t_{on}	Turn-on propagation delay	—	220	260		$V_S = 0V$
t_{off}	Turn-off propagation delay	—	120	150		$V_S = 400V$
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	—	100	190		
MT	Delay matching, HS & LS turn-on/off	—	—	70		

Electrical Characteristic

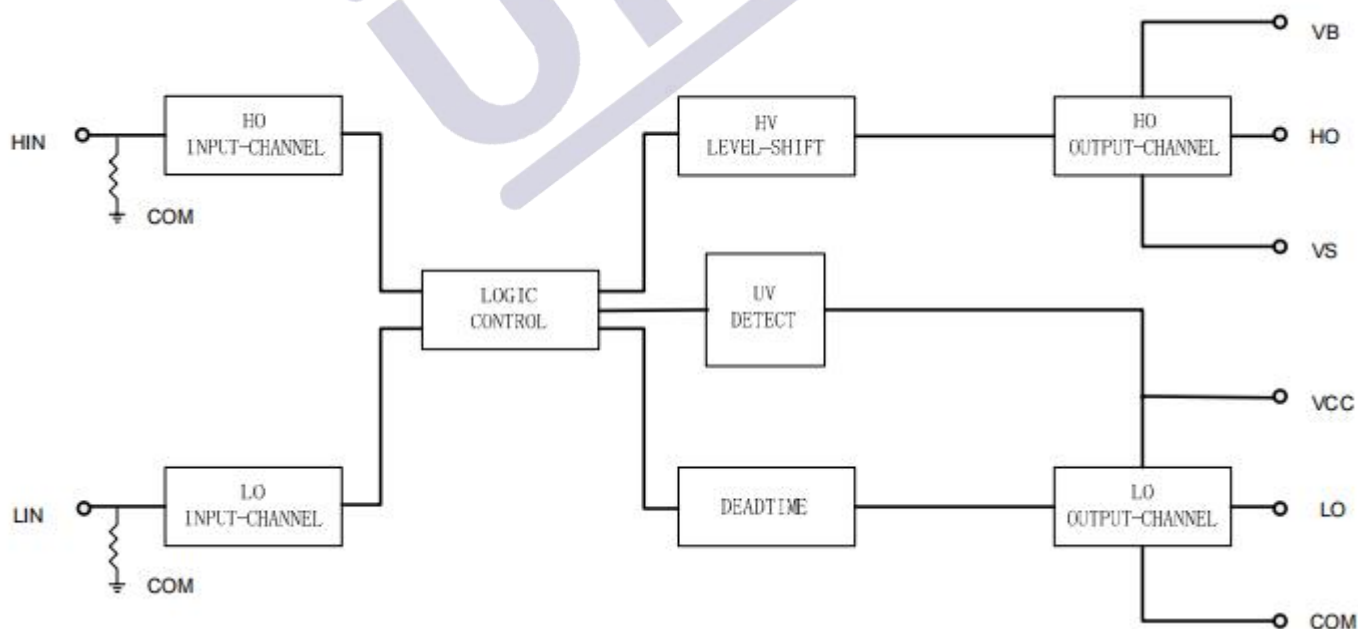
$V_{CC} = V_{BS} = V_{BIAS} = 15V$, $TA = 25^{\circ}C$, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
IQCC	Quiescent VCC supply current	—	300	500	uA	$V_{in} = 0V$ or $5V$
IQBS	Quiescent VBS supply current	—	100	200		$V_{in} = 0V$ or $5V$
ILK	Offset supply leakage current	—	—	3		$V_B = V_S = 400V$
V_{IH}	Logic "1" (HO) & Logic "0" (LO) input voltage	3	—	—	V	$V_{CC} = 3V$ to $20V$
V_{IL}	Logic "0" (HO) & Logic "1" (LO) input voltage	—	—	0.8		$V_{CC} = 3V$ to $20V$
IIN+	Logic "1" input bias current	—	3	10	uA	$V_{IN} = 5V$ $I_{IN} = 0V$
IIN-	Logic "0" input bias current	—	—	1		$V_{IN} = 5V$ $I_{IN} = 0V$
VOH	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
VOL	Low level output voltage, V_O	—	—	100		$I_O = 0A$
IO+	Output high short circuit pulsed current	—	2000	—	mA	$V_O = 0V$ $V_{IN} = V_{IH}$ $PW \leq 10 \mu s$
IO-	Output low short circuit pulsed current	—	2500	—		$V_O = 15V$ $V_{IN} = V_{IL}$ $PW \leq 10 \mu s$

Block Diagram

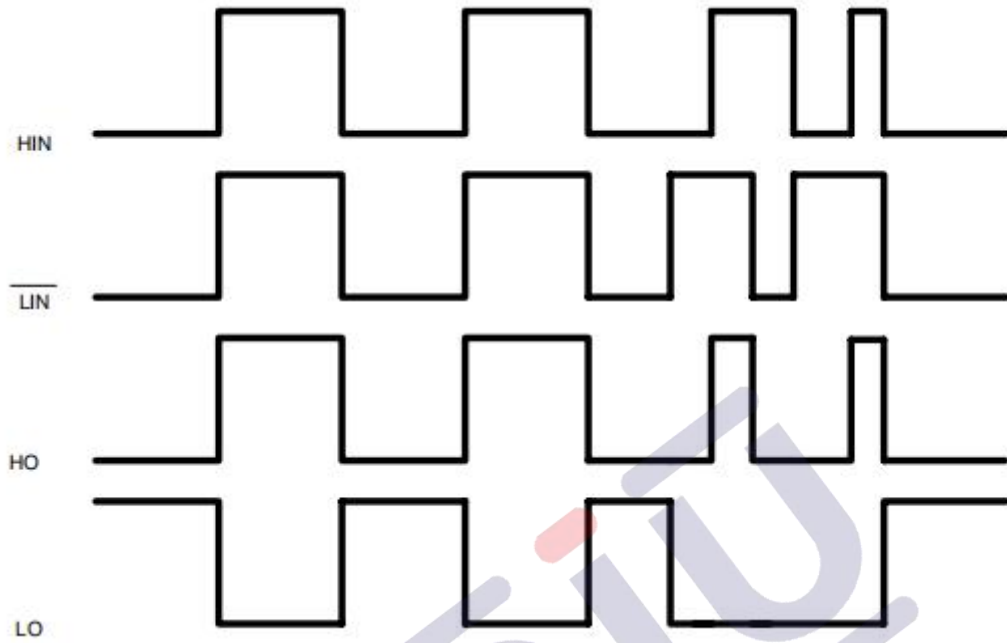


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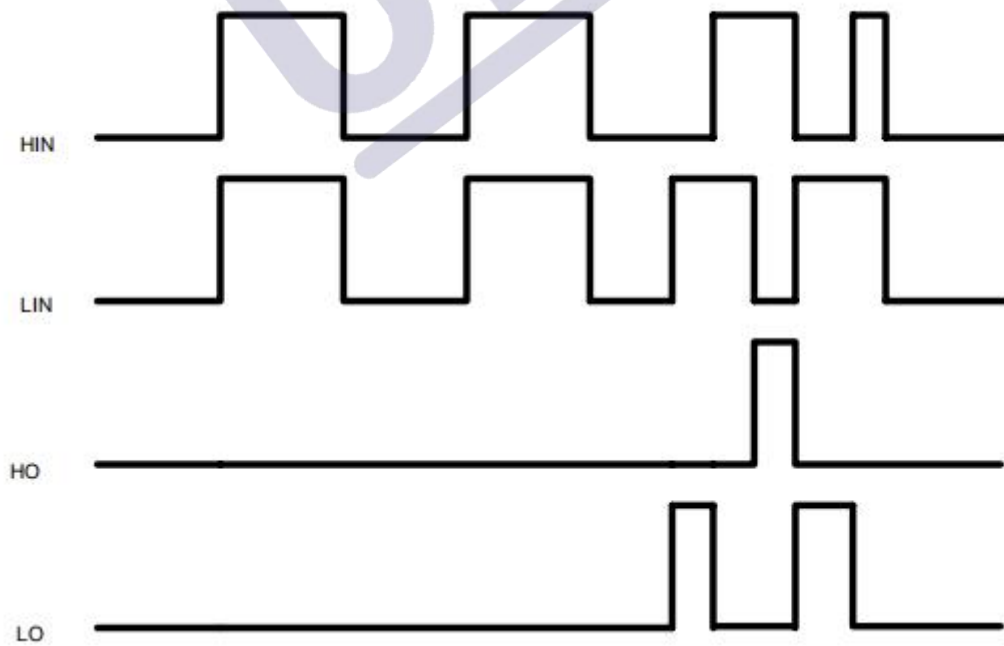


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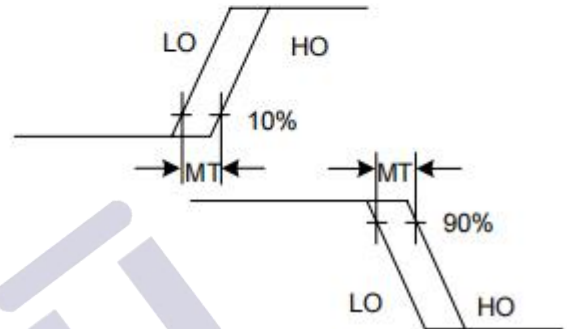
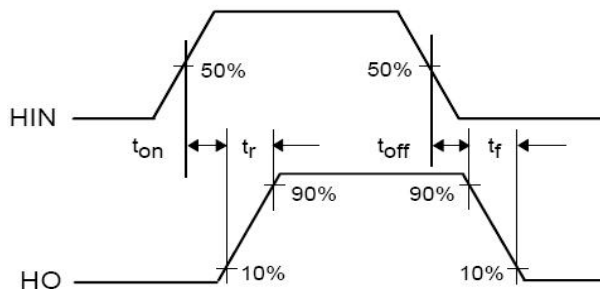
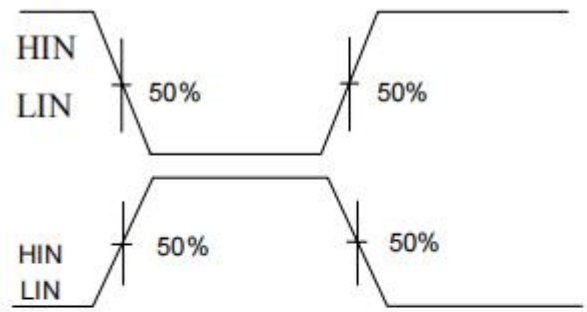
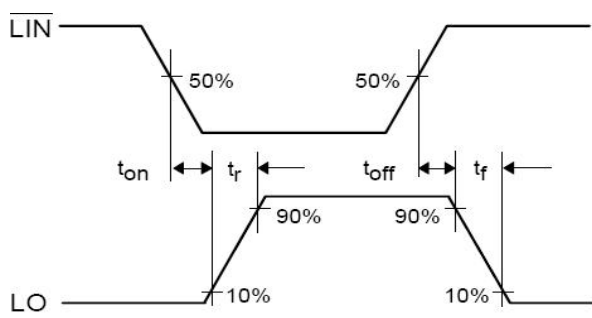
Time waveform



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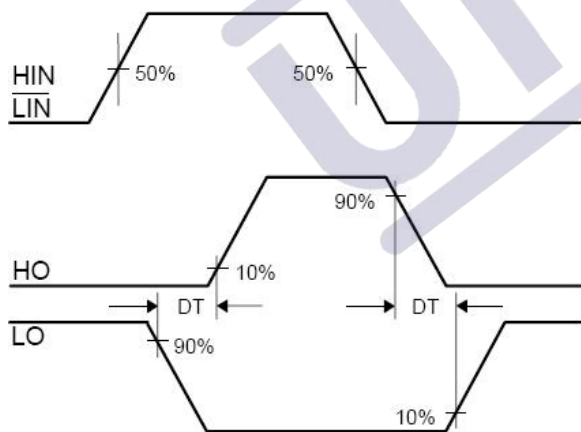


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Switching Time Waveform Definitions

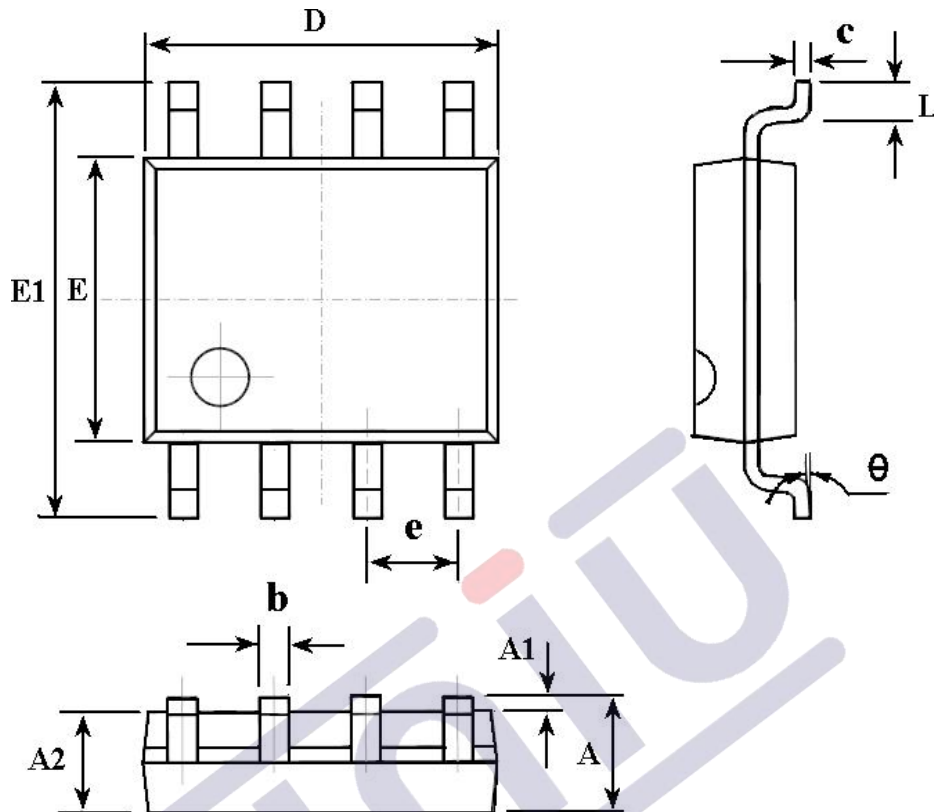
Delay matching time Definitions



Deadtime Waveform Definitions

Packaging information

SOP 8



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2019/05/21	2.0	Change the package
2021/10/18	3.0	Layout adjustment
2022/11/09	3.1	Change the Logo

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