# MSKSEMI 美森科













**ESD** 

TV

TSS

MOV

GDT

PLED

AOTL66912-MS

Product specification





# **Description**

The AOTL66912-MS use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics.

This device is specially designed to get better ruggedness.

## **Features**

- VDS = 100V ID= 350A
- RDS(ON) < 2mΩ VGS=10V</li>

# **Application**

- Battery Protection
- Power Distribution

## **Reference News**

TOLL-8	N-Channel MOSFET	Marking
Pin1 S G Pin1	G S S	MSKSEMI TL66912 MS N100

# **Absolute Maximum Ratings** (Tc=25°C unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>G</sub> s	±20	V	
Continuous Drain Current	Tc=25°C		350	А	
Continuous Diam Current	Tc=100°C	lo	200		
Pulsed Drain Current <sup>1</sup>		Ірм	1248	Α	
Single Pulse Avalanche Energy <sup>2</sup>		EAS	1250	mJ	
Total Power Dissipation	Tc=25°C	PD	390.6	W	
Operating Junction and Storage Temperature Range		Тл, Тэтс	-55 to 150	°C	
Thermal Resistance from Junction-to-Ambient <sup>3</sup>		Reja	39	°C/W	
Thermal Resistance from Junction-to-Case		Rелс	0.32	°C/W	



# Electrical Characteristics (TJ=25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Vo	oltage	V(BR)DSS	V <sub>G</sub> S = 0V, I <sub>D</sub> = 250µA	100	-	-	V
Gate-body Leakage current		lgss	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage	T <sub>J</sub> =25°C	IDSS	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	-	-	1	μΑ
Drain Current	T <sub>J</sub> =100°C			-	-	100	
Gate-Threshold Voltage		V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA	2	3	4	V
Drain-Source on-Resistance <sup>4</sup>		RDS(on)	Vgs = 10V, ID = 20A	-	1.4	2.0	mΩ
Forward Transconductance <sup>4</sup>		<b>g</b> fs	V <sub>DS</sub> = 10V, I <sub>D</sub> =20A	-	84	-	S
Dynamic Characteristic	CS <sup>5</sup>					'	
Input Capacitance	nput Capacitance			-	14300	-	
Output Capacitance Reverse Transfer Capacitance		Coss	V <sub>DS</sub> = 50V, V <sub>GS</sub> =0V, f =1MHz	-	2120	-	pF
		Crss		-	50	-	
Gate Resistance		Rg	f=1MHz	-	2.8	-	Ω
Switching Characterist	ics <sup>5</sup>	1				1	
Total Gate Charge Gate-Source Charge Gate-Drain Charge		Qg	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 50V, I <sub>D</sub> = 20A	-	250	-	nC
		Qgs		-	53	-	
		Qgd	2071	-	77	-	
Turn-on Delay Time  Rise Time  Turn-off Delay Time		td(on)		-	41	-	
		tr	V <sub>GS</sub> =10V, V <sub>DD</sub> =	-	88	-	20
		<b>t</b> d(off)	50V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	163	-	ns
Fall Time		tf		-	98	-	
Body Diode Reverse Recov	Body Diode Reverse Recovery Time		- I⊧=20A, di/dt = 100A/μs	-	106	-	ns
Body Diode Reverse Recovery Charge		Qrr		-	245	-	nC
Drain-Source Body Dic	ode Charac	teristics					
Diode Forward Voltage <sup>4</sup>		VsD	Is = 20A, VGS = 0V	-	-	1.2	V
Continuous Source Current	Tc=25°C	ls	-	-	-	312	Α

#### Note:

- A. The maximum current rating is package limited.
- B. Repetitive rating; pulse width limited by max. junction temperature.
- C.  $V_{DD}$ =32 V,  $R_G$ =25  $\Omega$ , L=0.5mH, starting  $T_j$ =25°C.
- D. P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.
- E. The value of Reja is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25°C.



# **Typical Characteristics**

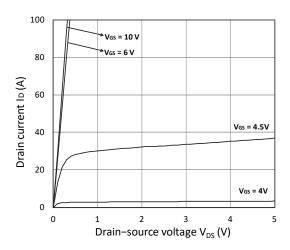


Figure 1. Output Characteristics

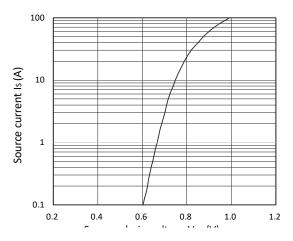


Figure 3. Forward Characteristics of Reverse

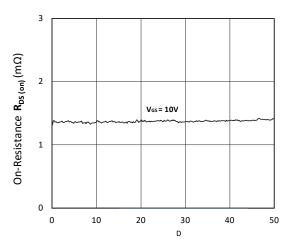


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$ 

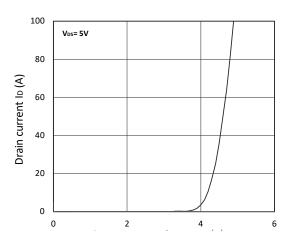


Figure 2. Transfer Characteristics

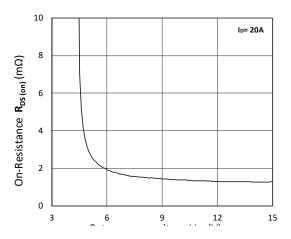


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$ 

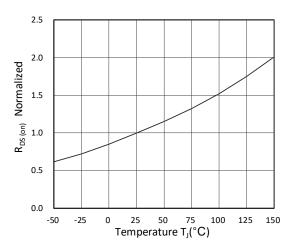


Figure 6. Normalized  $R_{\text{DS(on)}}$  vs. Temperature



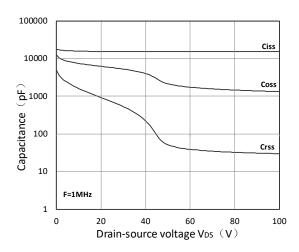


Figure 7. Capacitance Characteristics

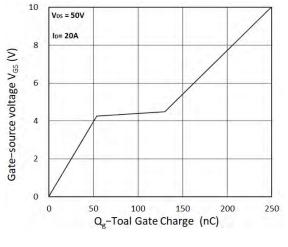


Figure 8. Gate Charge Characteristics

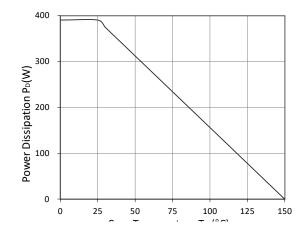


Figure 9. Power Dissipation

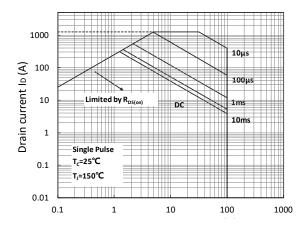


Figure 10. Safe Operating Area

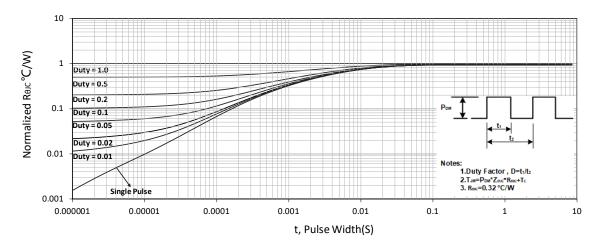


Figure 11. Normalized Maximum Transient Thermal Impedance



# **Test Circuit**

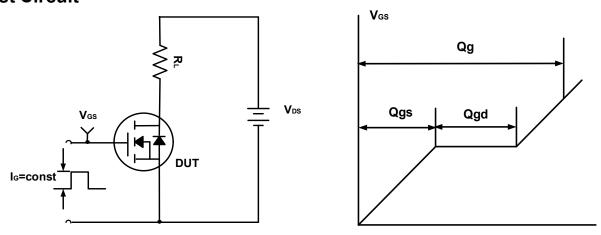


Figure A. Gate Charge Test Circuit & Waveforms

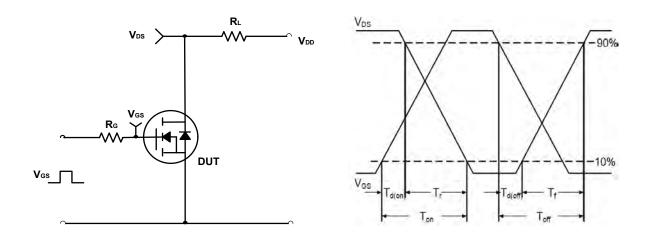


Figure B. Switching Test Circuit & Waveforms

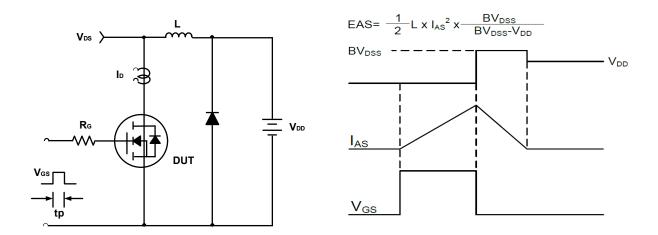
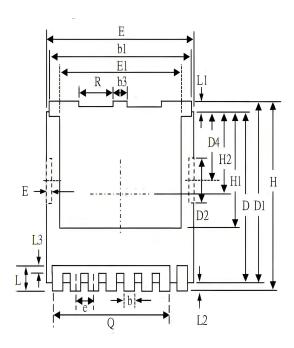


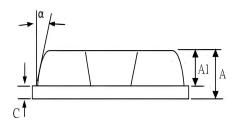
Figure C. Unclamped Inductive Switching Circuit & Waveforms



# **TOLL-8 Package Information**



BACKSIDE VIEW



- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.

SYMBOLS	MIN	NOM	MAX
A	2. 20	2. 30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
С	0.40	0.50	0.60
D	10. 28	10.38	10. 58
D1	9.80	11.08	11.80
D2	3. 10	3. 30	3.50
D4	4. 37	4. 55	4. 77
Е	9.70	9.90	10.10
E1	7.90	8.10	8.30
E2	0.50	0.70	0.90
е		1.20BCS	
Н	11.48	11.68	11.88
H1	6. 95BCS		
Н2	5. 89BCS		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	1.30
Q	8.00 REF.		
R	2.95	3. 10	3. 25
α	4°		10°

# **REEL SPECIFICATION**

P/N	PKG	QTY
AOTL66912-MS	TOLL-8	2000



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