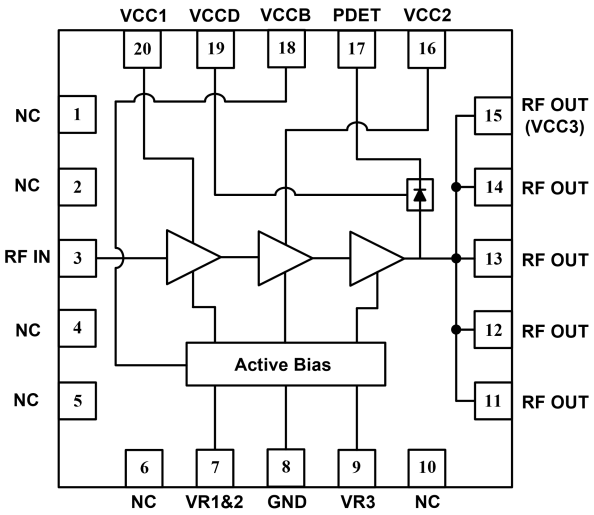
Pb-free & RoHs Product

Features

- 960~1500MHz Frequency Range
- 30dB Power Gain (Typ.)
- 38dBm Saturation Output Power
- 10dB Input Return Loss
- 3.3~5.5V Supply Voltage
- 12mA Quiescent Current
- Integrated Output Power Detector
- Integrated ESD Protection Unit
- Advanced InGaP/GaAs HBT Technology



Functional Block Diagram

Applications

- 960-1215MHz avionics
- Unmanned Aerial Vehicle System
- 1.4GHz Drone Image Transmission
- Air traffic control systems (ATC)

Product Description

The YP163038 is a high-power, high-efficiency Power Amplifier optimized for the applications in bands from 960MHz to 1500MHz (it needs different matching circuit for different frequency range), such as 960-1215MHz avionics and 1.4GHz Drone Image Transmission. The Power Amplifier provides a typical power gain of 30dB and saturation power of 38dBm with CW input, typical quiescent bias condition is 5.0V at 12mA. The device is manufactured on an advanced InGaP/GaAs Heterojunction Bipolar Transistor (HBT) process. The YP163038 is assembled in a 20-pin, 5mm×5mm, QFN package, it is internally integrated with ESD protection unit.

Ordering Information

- YP163038 1.4GHz Power Amplifier Chip
- YP163038-EVB YP163038 Evaluation Board of 960-1215MHz, 1.4GHz

Pin Description

Pin No.	Symbol	Description
3	RF IN	RF input
7, 9	VR1&2, VR3	Bias current control voltage
11, 12, 13, 14, 15	RF OUT (VCC3)	RF output and Supply voltage for stage 3
16	VCC2	Supply voltage for stage 2
17	PDET	Power detect
18	VCCB	Supply voltage for bias
19	VCCD	Supply voltage for power detector
20	VCC1	Supply voltage for stage 1e
1, 2, 4, 5, 6, 10	NC/GND	No connection or ground
8, PKG Base	GND	Ground connection

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input RF Power	RF IN	+10	dBm
Supply Voltage	VCC1,VCC2,VCC3, VCCB,VCCD	-0.5 to +6.0	V
Reference Voltage	VR1&2, VR3	-0.5 to +3.0	V
Operating Ambient Temperature	T_{OP}	-40 to +105	°C
Storage Temperature	T_{ST}	-40 to +150	°C

Caution! ESD Sensitive Device.

ESD Rating: Class1C
Value: Passes≥1000V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥1000V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Electrical Specifications

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Compliance and Nominal Conditions					VCC1=VCC2=VCC3=VCCB=5.0V, ICQ=20mA, T_{OP}=+25°C
Frequency range		1400		MHz	
Saturation output power		38		dBm	CW
Power gain		30		dB	@Pout=38dBm
Input return loss		15		dB	
Reference Voltage		2.45		V	
Quiescent current, ICQ		20		mA	VR1&2=VR3=2.45V
Operating current, ICC		2800		mA	@Pout=38dBm

Typical Performance

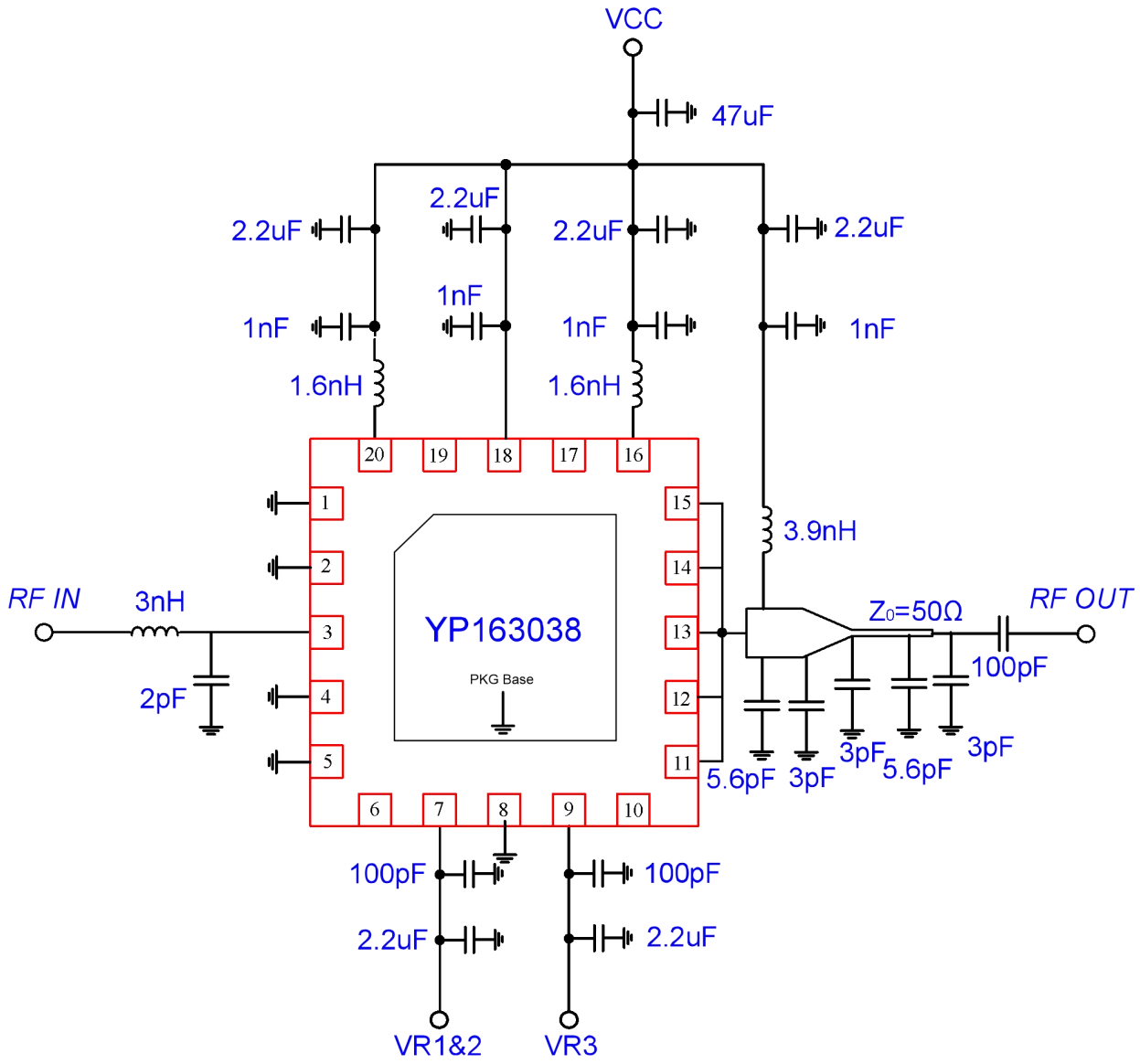
(Test Condition: Freq=960-1230MHz, VCC1=VCC2=VCC3=VCCB=5V, VR1&2=VR3=2.6V, T=+25°C)

Bias：VCC= 5.0V，VR1&2=VR3=2.6V，ICQ=380mA；

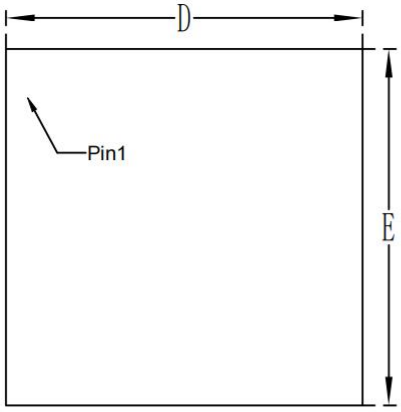
Freq (MHz)	P-1 (dBm)	ICC (A)	Gp (dB)	PAE (%)
960	33.2	1.66	29.3	24
990	34.2	1.66	31.3	31
1020	34.6	1.56	30.8	36
1050	34.2	1.3	31.4	40
1070	34.2	1.3	31.4	40
1100	33.7	1.27	31.2	36
1130	33.5	1.26	30.8	35
1160	33.3	1.28	31	33
1190	32.8	1.17	30.3	32
1230	32.4	1.18	29.8	29

Evaluation Board Schematic

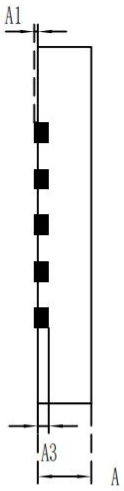
(Test Condition: Freq=960-1230MHz, VCC1=VCC2=VCC3=VCCB=5V, VR1&2=VR3=2.6V, T=+25°C)



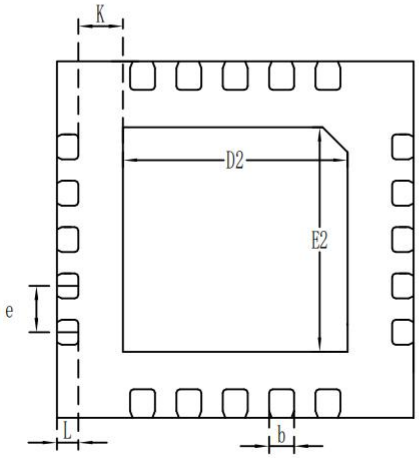
Packaging Diagram



TOP VIEW
[顶视图]



SIDE VIEW
[侧视图]



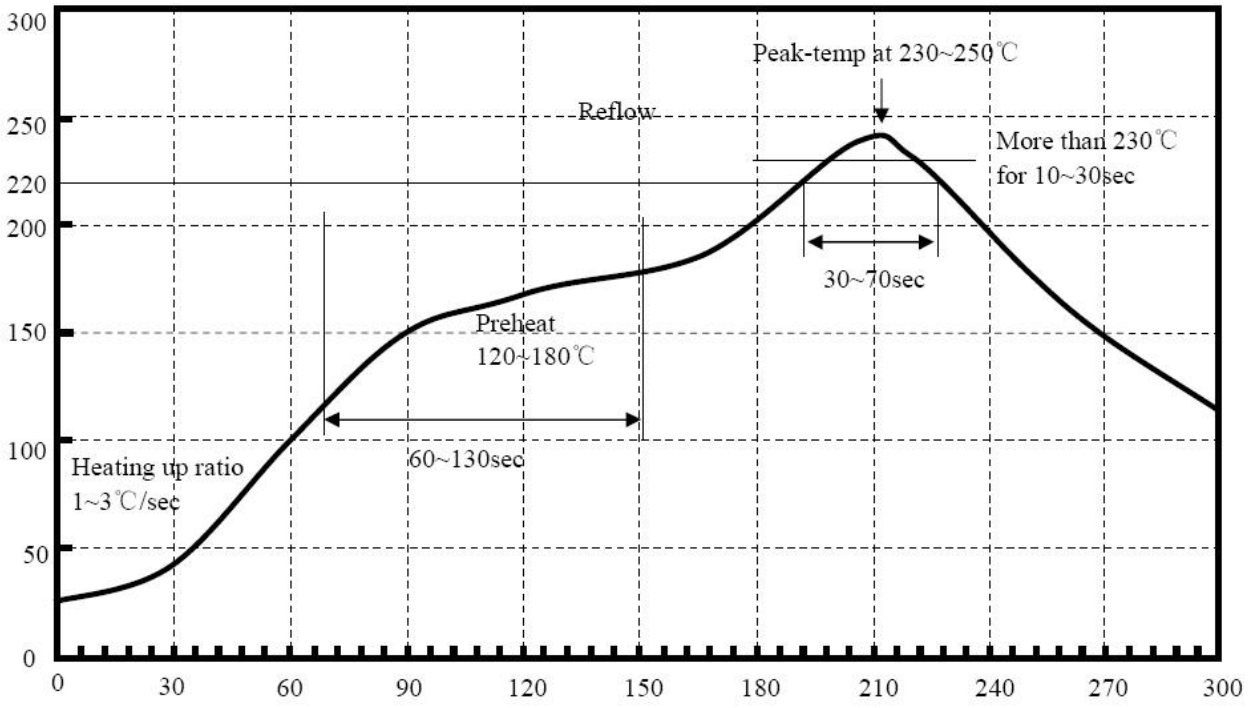
BOTTOM VIEW
[底视图]

编号	尺寸（mm）		
	Min	TYP	Max
A	0.650	0.750	0.850
A1	0.000	0.020	0.050
A3	--	0.203	--
b	0.300	0.350	0.400
D	4.900	5.000	5.100
E	4.900	5.000	5.100
e	--	0.650	--
D2	--	3.150	--
E2	--	3.150	--
L	--	0.300	--
K	0.200	0.625	--
R	0.090	0.125	--

Note 1

Vias(Φ0.3mm THRU * 25) are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.

Recommended Solder Temperature



Recommended Temperature

Sn95.5Ag4.0Cu0.5

Note 2

If these amplifiers are to be subjected to solder reflow or high temperature processes, they must be baked for 48 hours at 125℃ prior to board mount. Failure to comply may result in crack and/or delamination of critical interfaces within the package.