矽源 Silicon

Preliminary Datasheet

650V, 1A, E-Mode, N-Channel & P-Channel MOSFET

OSM1N1P65

FEATURES

- 650V breakdown voltage
- Independent N- and P-channels
- Electrically isolated N- and P-channels
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdowns
- Low input and output leakage
- SOP8 封装

APPLICATIONS

- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers

GENERAL DESCRIPTION

The OSM1N1P65 consists of a high voltage N-channel and P-channel MOSFET in an 8-Lead SOIC package. This is an enhancement-mode (normally-off) transistor utilizing an advanced Planner DMOS structure. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

OSM1N1P65 are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

VIEW AND INTERNAL SCHEMATIC DIAGRAM

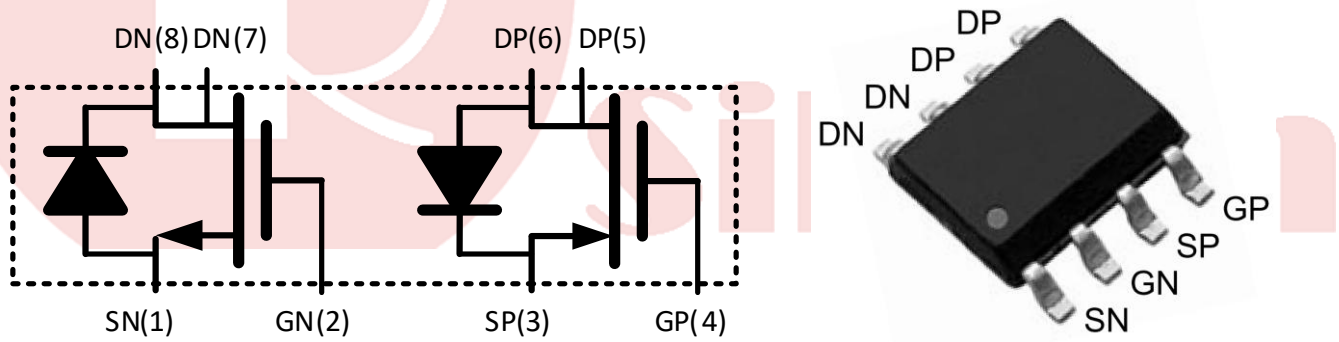


Figure 1. View and Internal Schematic Diagram

SPECIFICATIONS

N-Channel:

Table 1. Typical and limits appearing in normal type apply for T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static Parameters						
Source-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{SS} =250μA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DSS} =650V, V_{GS} =0V			1	μA
Gate-Source leakage current	I_{GSS}	V_{DSS} =0V, V_{GS} = + 30V			0.1	μA
		V_{DSS} =0V, V_{GS} = − 30V			-0.1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DSS} = V_{GS}, I_{SS} =250μA	2		4	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V			1	μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} =0V, I_{SS} =0.5A			13	Ω
Diode Forward Voltage	V_{FSS}	V_{GS}= 0V, I_{SD}=1A			1.2	V

Note: 1. 参数由设计保证
2. 测量修正。

P-Channel:

Table 2. Typical and limits appearing in normal type apply for T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static Parameters						
Source-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{SS} =250μA	-650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DSS} =-650V, V_{GS} =0V			-1.0	μA
Gate-Source leakage current	I_{GSS}	V_{DSS} =0V, V_{GS} = + 30V			0.1	μA
		V_{DSS} =0V, V_{GS} = − 30V			-0.1	μA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DSS} = V_{GS}, I_{SS} =250μA	-2		-5.0	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-650V, V_{GS}=0V			-1.0	μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} =-10V, I_{SS} =-1A			15	Ω
Diode Forward Voltage	V_{FSS}	V_{GS}= 0V, I_{SD}=1A			-1.25	V

Note: 1. 参数由设计保证
2. 测量修正。

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDSS(ON)	650V
VGS	±30V
NMOS/PMOS ISS(DC)	1A
NMOS/PMOS ISS(Pulse)	4A
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Operating Ambient Temperature Range	–40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

注意, 超出上述绝对最大额定值可能会导致器件永久性损坏。这只是额定应力值，不涉及器件在这些或任何其他条件下超出本技术规格指标的功能性操作。长期在绝对最大额定值条件下工作会影响器件的可靠性。

THERMAL DATA

绝对最大额定值仅适合单独应用，但不适合组合使用。结温高于限制值时，会损坏芯片。监控环境温度并不能保证 T_J 不会超出额定温度限值。在功耗高、热阻差的应用中，可能必须降低最大环境温度。

在功耗适中、PCB 热阻较低的应用中，只要结温处于额定限值以内，最大环境温度可以超过最大限值。器件的结温（T_J）取决于环境温度（T_A）、器件的功耗（P_D）和封装的结到环境热阻（θ_{JA}）。

最高结温 (T_J) 由环境温度(T_A) 和功耗 (P_D) 通过下式计算：

$$T_J = T_A + (P_D \times \theta_{JA})$$

封装的结到环境热阻 (θ_{JA}) 基于使用 4 层板的建模和计算方法，主要取决于应用和板布局。在功耗较高的应用中，需要特别注意热板设计。θ_{JA} 的值可能随 PCB 材料、布局和环境条件不同而异。θ_{JA} 的额定值基于 4" × 3" 的 4 层电路板。有关板结构的详细信息，请参考 JESD 51-7 和 JESD 51-9。

Ψ_{JB} 是结到板热特性参数，单位为 °C/W. 封装的 Ψ_{JB} 基于使用 4 层板的建模和计算方法。JESD51-12——"报告和使用电子封装热信息指南"中声明，热特性参数和热阻不是一回事。Ψ_{JB} 衡量沿多条热路径流动的器件功率，而 θ_{JB} 只涉及一条路径。因此，Ψ_{JB} 热路径包括来自封装顶部的对流和封装的辐射，这些因素使得 Ψ_{JB} 在现实应用中更有用。最高结温 (T_J) 由板温度 (T_B) 和功耗 (P_D)通过下式计算：

$$T_J = T_B + (P_D \times \Psi_{JB})$$

有关 Ψ_{JB} 的详细信息，请参考 JESD51-8 和 JESD51-12。

THERMAL RESISTANCE

θ_{JA} 和 Ψ_{JB} 针对最差条件，即器件焊接在电路板上以实现表贴封装。

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8			°C /W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

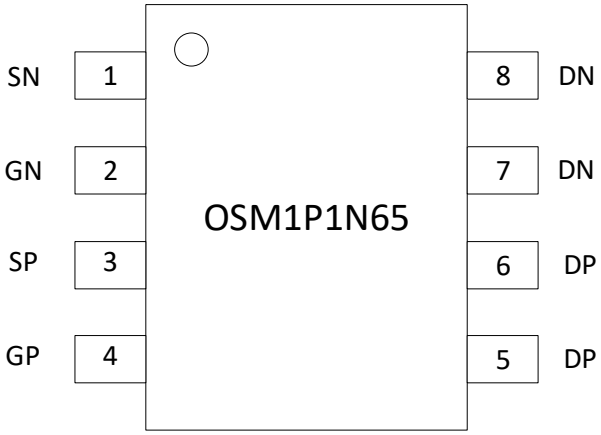
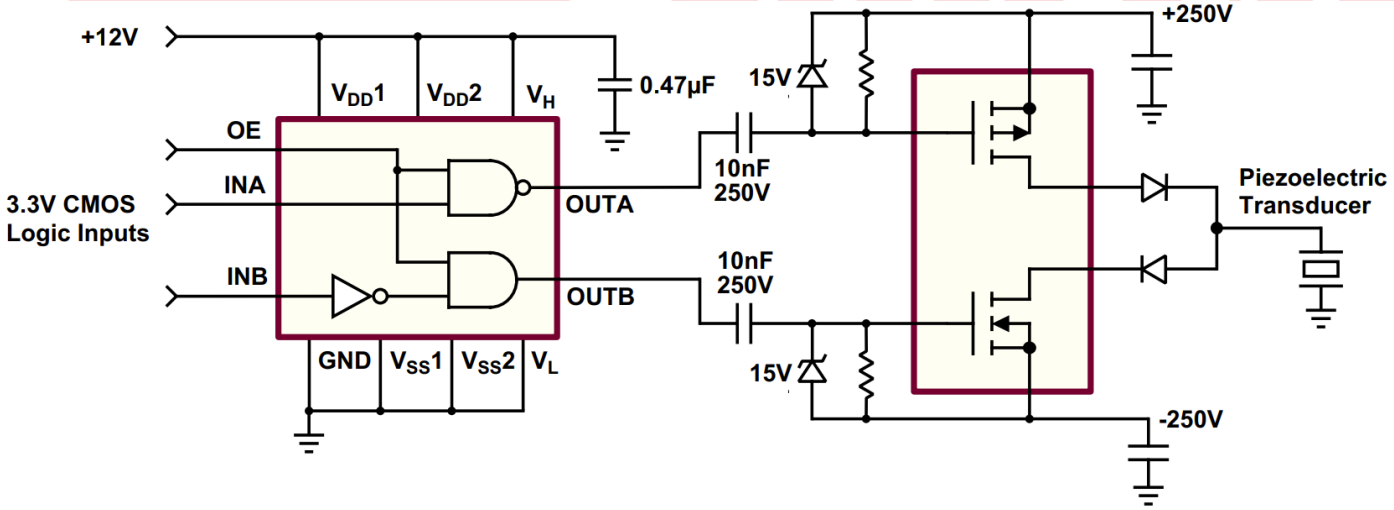


Figure 2. Pin Configuration (Bottom View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SN	N-MOSFET Source
2	GN	N-MOSFET Gate
3	SP	P-MOSFET Source
4	GP	P-MOSFET Gate
5-6	DP	P-MOSFET Drain
7-8	DN	N-MOSFET Drain

APPLICATION:



OUTLINE DIMENSIONS

尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17° TYP4	
C	1.30	1.60	θ2	13° TYP4	
C1	0.55	0.65	θ3	0° ~ 8°	
C2	0.55	0.65	θ4	4° ~ 12°	

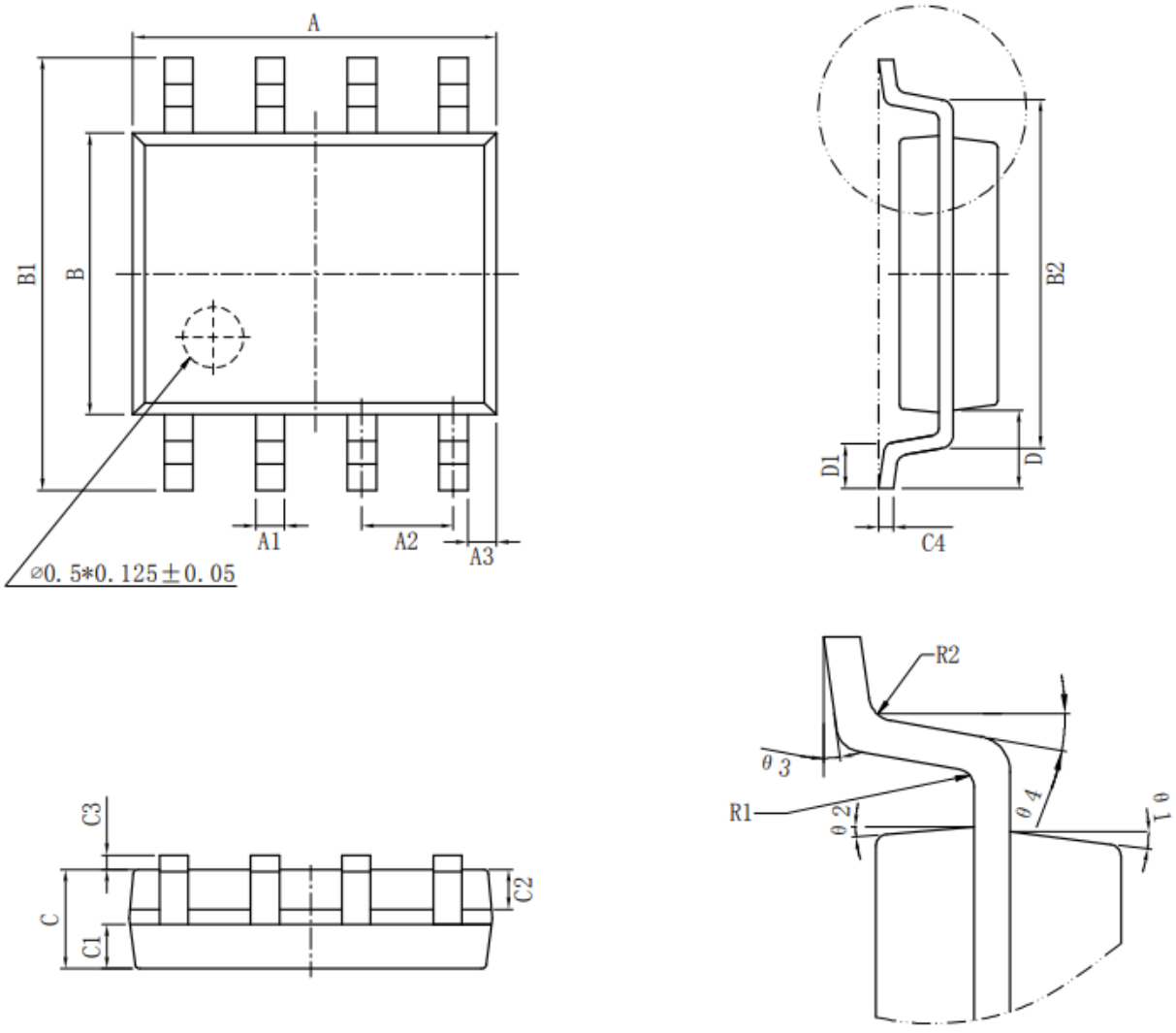


Figure 3. SOP8 Package

版本说明

版本	改动页码	改动图片	改动内容	改动公式	备注
1.0					initial