Datasheet

Earth Leakage Current Detector

SS4125C

FEATURES

- 输入电压: 45 V_{AC} to 220 V_{AC}（50Hz-60Hz）
- 静态工作电流: 200μA（典型）
- 电磁干扰（EMC）防护能力：
  - 无外部滤波电路: ≥10V/m
  - 增加外部 π 型滤波: ≥18V/m
- 适用于检测 AC 型漏电信号
- 漏电峰值检测限制
- 高频漏电流抑制能力
- 外部固定延迟调整
- 外部反延时调整（随不同倍率漏电流变化）
- 下进线应用
- 高输入灵敏度：V_T= 4.95mV（典型）
- 双输出驱动信号：
  - 10V（type）高压 MOS 驱动(OS_HV)
  - 5V（type）可控硅驱动(OS_LV)
- 不能跳闸时，同步输出:
  - OS_LV 输出 3 个 30ms：100ms 占空比脉冲控制信号
  - OS_HV 输出 3 个 30ms：100ms 占空比脉冲控制信号
- 符合国标 GB16916，GB16917 和 GB14048 标准
- 宽的温度范围（Ta= -40 ~ +125℃）
- 8-lead SOP

APPLICATIONS

- 下进线塑壳式断路器
- 高速漏电保护装置
- 防漏电插座
- 带有漏电保护的小家电

GENERAL DESCRIPTION

SS4125C 是一款针对上下进线应用的高性能、高可靠的高频漏电流抑制延时型 AC 漏电保护器专用芯片，用于检测火线和零线上的漏电信号。

SS4125C 检测到有效频率内的有效信号时，OA 端口通过外部电容产生积分信号（峰值限制），高频检测电路输出延迟使能信号，当积分信号与延迟使能信号均满足阈值，输出驱动高电平信号。当断路器不能正常跳闸时，内部数字处理器将输出占空比为 30ms:100ms 的 3 个脉冲控制信号，从而保证断路器彻底关断，有效地保护触电危险。同时 SS4125C 针对不同的应用场景，具有双路输出驱动，可同时驱动高压 MOS 和可控硅，增强了产品的应用场景。

芯片的反延时特性可通过调节 OA 端口外接电容来实现，固定延迟可通过调节 DLY 端口的外部电容来实现。当芯片检测到高频漏电信号时，高频检测模块识别后，不输出延迟使能信号，即使积分输出满足了阈值，在与逻辑下输出驱动信号无法使能。

本芯片可稳定通过 GB14048 中 10V/m 电磁干扰、5KHz/100KHz EFT 群脉冲、雷击浪涌、周波跌落、工频磁场等等可靠性实验。

TYPICAL APPLICATION CIRCUIT

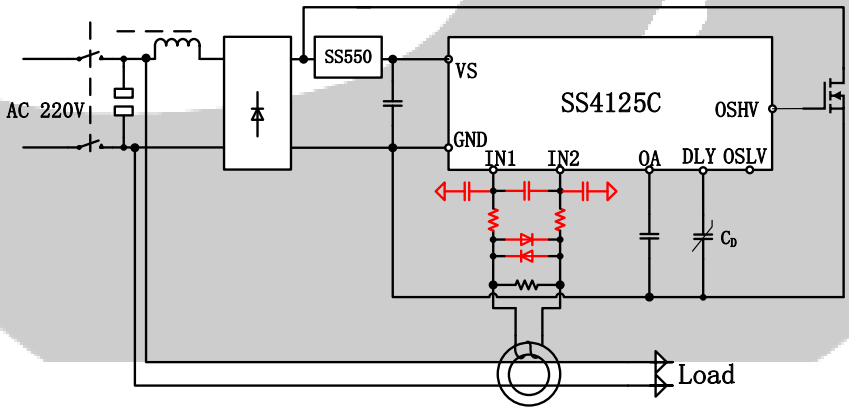

Figure 1. Typical Application Circuit

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SPECIFICATIONS

T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
电源端稳压电压	V_{S1}	钳位二极管电压@钳位电流 I_S=1mA; 常温		12		V
电源端稳压电压	V_{S2}	钳位二极管电压@钳位电流 I_S=1mA; 全温区	11		13	
供电电流(功耗 1)	I_{S1}	V_S=12V; IN1 – IN2=0mV; 常温	168		252	μA
供电电流(功耗 2)	I_{S2}	V_S=12V; IN1 – IN2=0mV; 全温区	150		295	μA
OS_HV 输出驱动电压	V_{OS_LV}	V_S=12V; IN1 – IN2=25mV		10	12	V
OS_LV 输出驱动电压	I_{OS_LV}	V_S=12V; IN1 – IN2=25mV		5	6	V
OS_LV 输出驱动电流 1	I_{OS_LV1}	OS=0.8V; IN1 – IN2=25mV; 常温	250		850	μA
OS_LV 输出驱动电流 2	I_{OS_LV2}	OS=0.8V; IN1 – IN2=25mV; 全温区	130		1500	μA
漏电动作电压	V_T	|IN1 – IN2|; C_{OD}=100nF	4.75	4.95	5.25	mV
漏电比较高电压	V_{REFSC_H}			1.5		V
漏电比较高电压	V_{REFSC_L}			1.25		V
OA 钳位电压	V_{CLAMP_OA}	IN1 – IN2 > 5mV		1.55		V
延迟注入电流	I_{DLY}	IN1 – IN2=25mV	2.7	3	3.3	μA
延迟比较电压	$V_{REFCDLY}$			1.5		V
漏电信号锁存时间	T_{ON}	IN1 – IN2=25mV	28			ms
OS 驱动脉冲个数		V_S=12V; IN1 – IN2=25mV			3	
高频漏电流抑制频率	f_{SUP}	C_{DLY} > 82nF		100		Hz

* 遵守国标 GB16916 标准要求

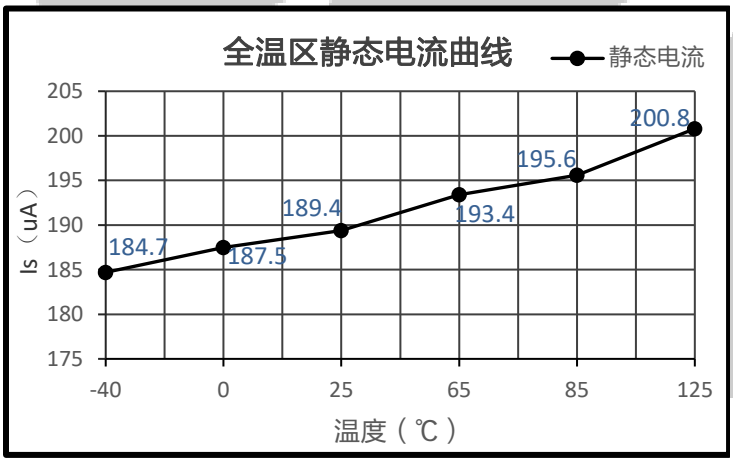


Figure2. I_S Curve In-40℃~125℃

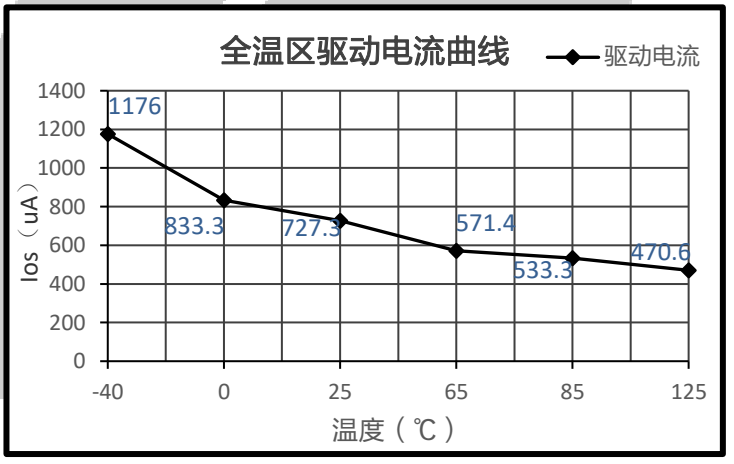


Figure3. I_{OS_LV} Curve In-40℃~125℃

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
I_{SMAX}	8mA
VS to GND	-0.3V to +24V
OSHV to GND	-0.3V to +15V
OSLV to GND	-0.3V to +6V
Input Voltage to GND	-0.3V to +6V
Output Voltage to GND	-0.3V to +6V
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Operating Ambient Temperature Range	–40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

注意, 超出上述绝对最大额定值可能会导致器件永久性损坏。这只是额定应力值，不涉及器件在这些或任何其他条件下超出本技术规格指标的功能性操作。长期在绝对最大额定值条件下工作会影响器件的可靠性。

THERMAL DATA

绝对最大额定值仅适合单独应用，但不适合组合使用。结温高于限制值时，会损坏芯片 。监控环境温度并不能保证 T_J 不会超出额定温度限值。在功耗高、热阻差的应用中，可能必须降低最大环境温度。

在功耗适中、PCB 热阻较低的应用中，只要结温处于额定限值以内，最大环境温度可以超过最大限值。器件的结温（T_J ）取决于环境温度（T_A ）、器件的功耗（P_D ）和封装的结到环境热阻（θ_{JA} ）。

最高结温 (T_J) 由环境温度(T_A) 和功耗 (P_D) 通过下式计算：

$$T_J = T_A + (P_D \times \theta_{JA})$$

封装的结到环境热阻 (θ_{JA}) 基于使用 4 层板的建模和计算方法，主要取决于应用和板布局。在功耗较高的应用中，需要特别注意热板设计。θ_{JA} 的值可能随 PCB 材料、布局和环境条件不同而异。θ_{JA} 的额定值基于 4" × 3" 的 4 层电路板。有关板结构的详细信息，请参考 JESD 51-7 和 JESD 51-9。

Ψ_{JB} 是结到板热特性参数，单位为 °C/W. 封装的 Ψ_{JB} 基于使用 4 层板的建模和计算方法。JESD51-12——"报告和使用电子封装热信息指南"中声明，热特性参数和热阻不是一回事。Ψ_{JB} 衡量沿多条热路径流动的器件功率，而 θ_{JB} 只涉及一条路径。因此，Ψ_{JB} 热路径包括来自封装顶部的对流和封装的辐射，这些因素使得 Ψ_{JB} 在现实应用中更有用。最高结温 (T_J) 由板温度 (T_B) 和功耗 (P_D)通过下式计算：

$$T_J = T_B + (P_D \times \Psi_{JB})$$

有关 Ψ_{JB} 的详细信息，请参考 JESD51-8 和 JESD51-12。

THERMAL RESISTANCE

θ_{JA} 和 Ψ_{JB} 针对最差条件，即器件焊接在电路板上以实现表贴封装。

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOP	96	55	°C /W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

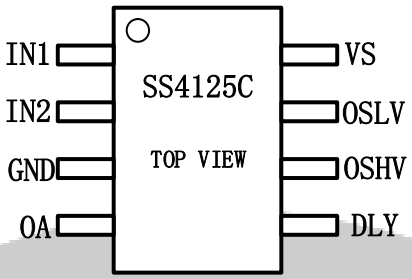


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	运放输入管脚 1
2	IN2	运放输入管脚 2
3	GND	芯片地
4	OA	滤波、反时线延时可调输出管脚（峰值限制）
5	DLY	固定延迟管脚，外接延迟电容
6	OSHV	高压 MOS 触发输出管脚
7	OSLV	可控硅触发输出管脚
8	VS	电源管脚

THEORY OF OPERATION

SS4125C 是一款高性能、高可靠 AC 型漏电保护器专用芯片，用于检测火线和零线上的漏电信号。采用小于 12V 电源供电，最小 SCR 驱动电流 0.2mA，最小高压 MOS 驱动电流 5mA。在无驱动时静态电流典型值低至 200μA，因此 SS4125C 可使用小功率分流电阻，降低了系统成本。

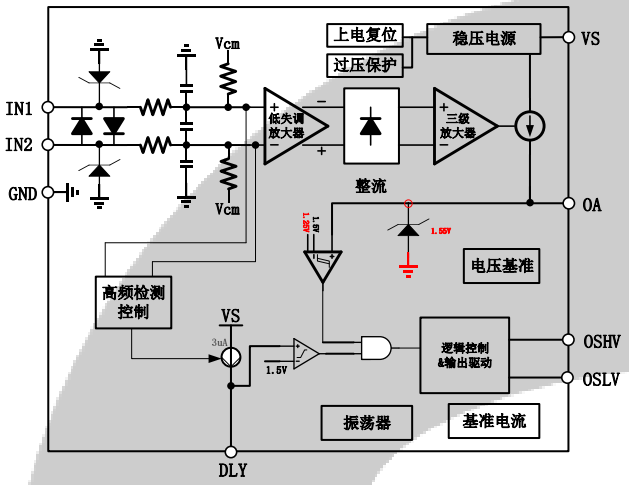


Figure 5. 芯片内部框图

工作原理：

SS4125C 检测到有效频率内的有效信号时，OA 端口通过外部电容产生积分信号（峰值限制），高频检测电路输出延迟使能信号，当积分信号与延迟使能信号均满足阈值，输出驱动高电平信号。

芯片的反延时特性可通过调节 OA 端口外接电容来实现，固定延迟可通过调节 DLY 端口的外部电容来实现。当芯片检测到高频漏电信号时，高频检测模块识别后，不输出延迟使能信号，即使积分输出满足了阈值，在与逻辑下输出驱动信号无法使能。

DLY 端口的电容需要满足最小值，最小值需要抑制 OA 端口最大电压（如最大漏电流时 OA 端口输出最高电压）下降到 1.25V 的时间内，DLY 端口不能上升到 1.5V，否则会出现误动的可能。

图 6 中，AC 是输入漏电流； OA_OUT 是 OA 比较器的输出；f_OUT 为高频滤波器判断输出（高电平表示输入频率正常，低电平表示超出设定频率），DLY_OUT 为延迟比较器输出。

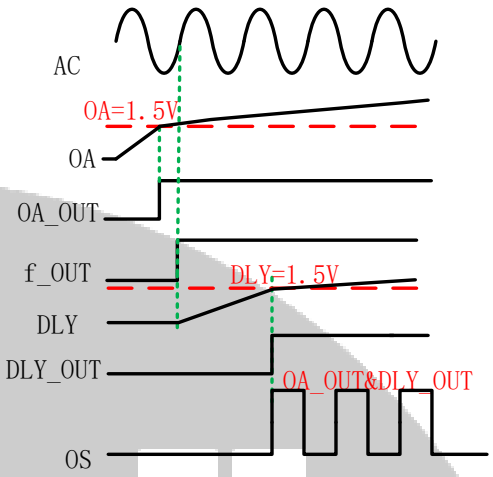


Figure 6. 工作原理图

DLY 工作原理

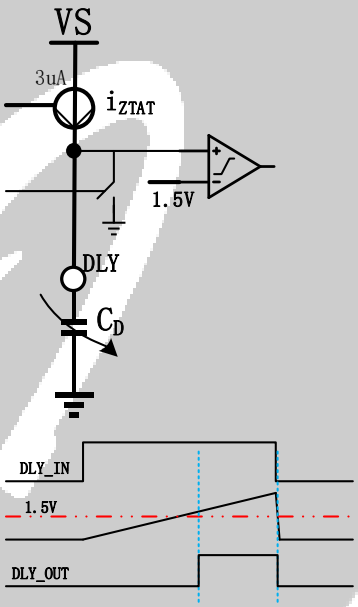


Figure 7. RC Time set circuit diagram

DLY 是输出固定延时控制端口。通过连接外部的电容，并调节电容大小，可以产生不同的输出控制信号延迟。

$$T_D = \frac{C_D \times V_{REF}}{I_D}$$

当 VREF = 1.5V， CD = 3.42uF(1μF+2.2μF+0.22μF)，ID = 3μA 时，

TD ≈ 1.71s

当 VREF = 1.5V， CD = 1.83uF(1.5μF+0.33μF)，ID = 3μA 时，

TD ≈ 0.915s

当 VREF = 1.5V， CD = 0.8uF(0.47μF+0.33μF)，ID = 3μA 时，

TD ≈ 0.4

反延时工作原理

OA 端口外接电容，可实现在不同倍率下漏电流的延时反比例曲线。SS4125C 的电流放大倍数在 300 倍左右，当不同倍率的漏电流施加后，在 OA 端口产生不同幅度的输出驱动电流，因电容与电流满足电荷公式满足:

$$i \times t = U \times C_{OA}$$

$$i = \frac{I_{RC} \times R_S}{CT \times 1K}$$

其中 IRC 为输入漏电流，CT 为互感器匝数，RS 为互感器采样电阻, U 为比较电压 1.5V, 从而得出时间 t 与输入漏电流和电容之间的公式：

$$t = \frac{CT \times 1K \times 1.5 \times C_{OA}}{I_{RC} \times R_S}$$

应用电路：

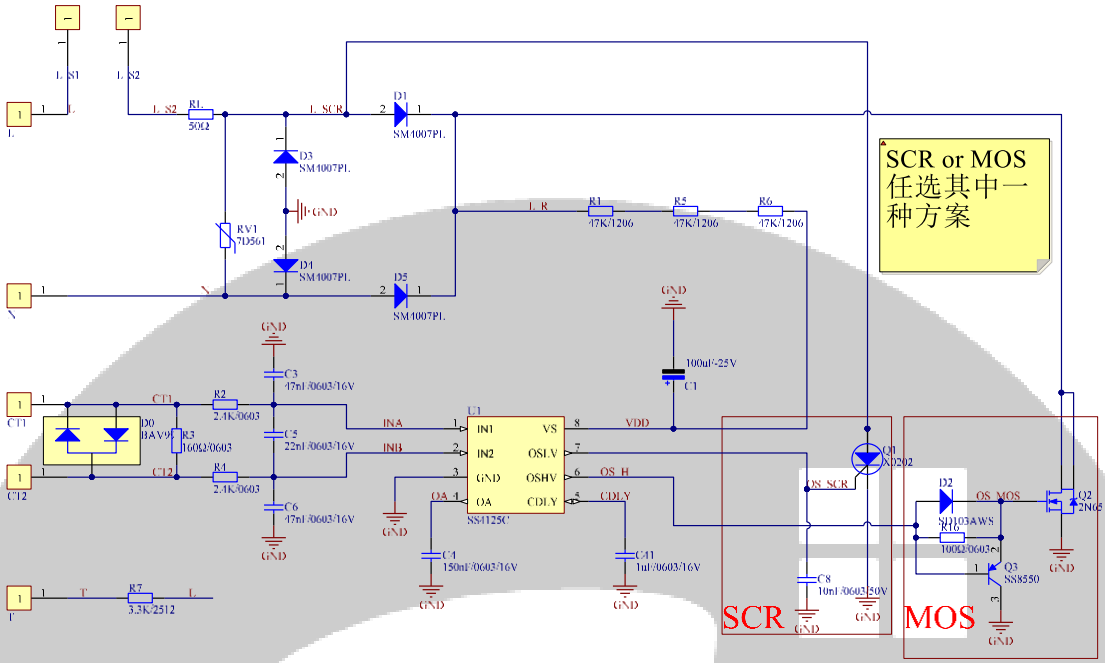


Figure 8. SS4125C high performance application

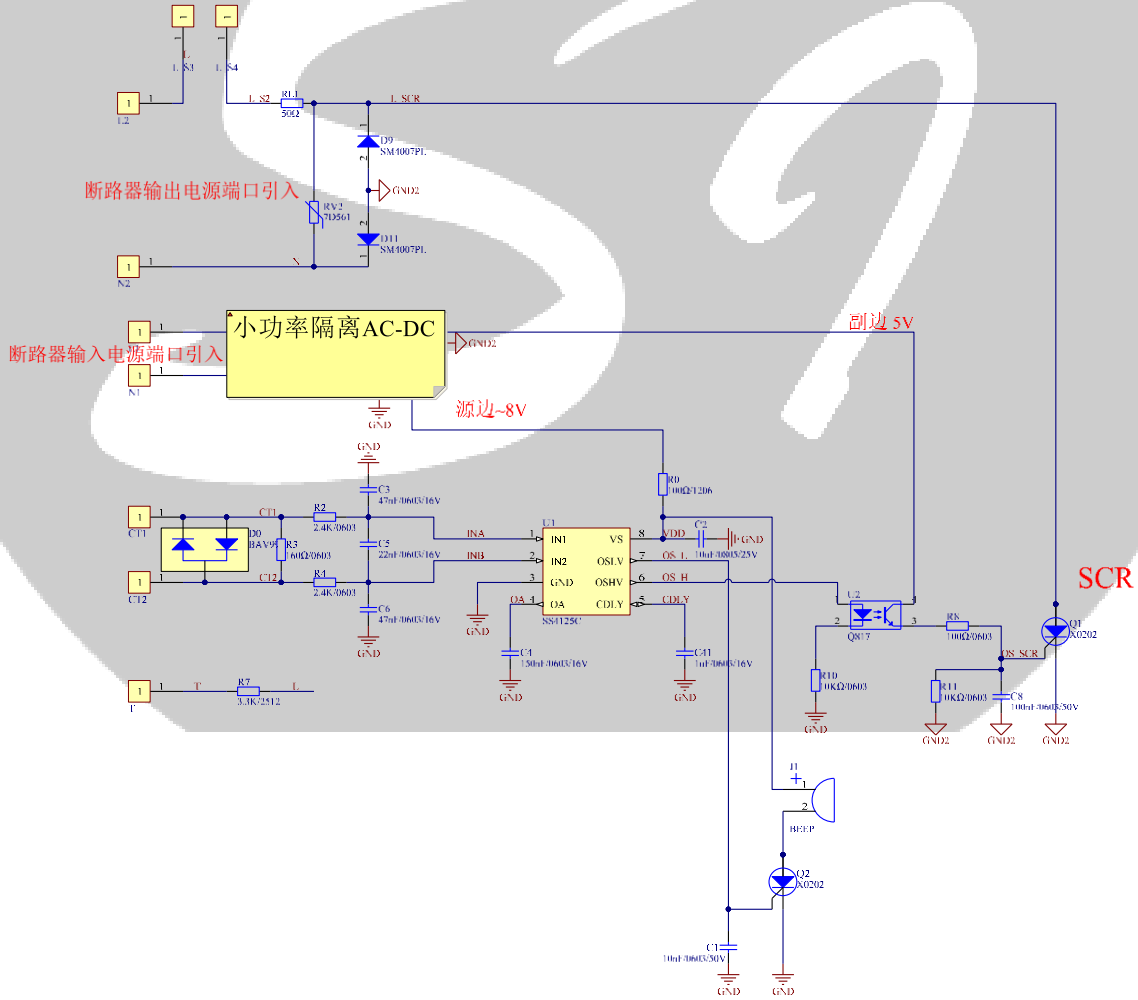


Figure 9. SS4125C high performance application with Beep Warning

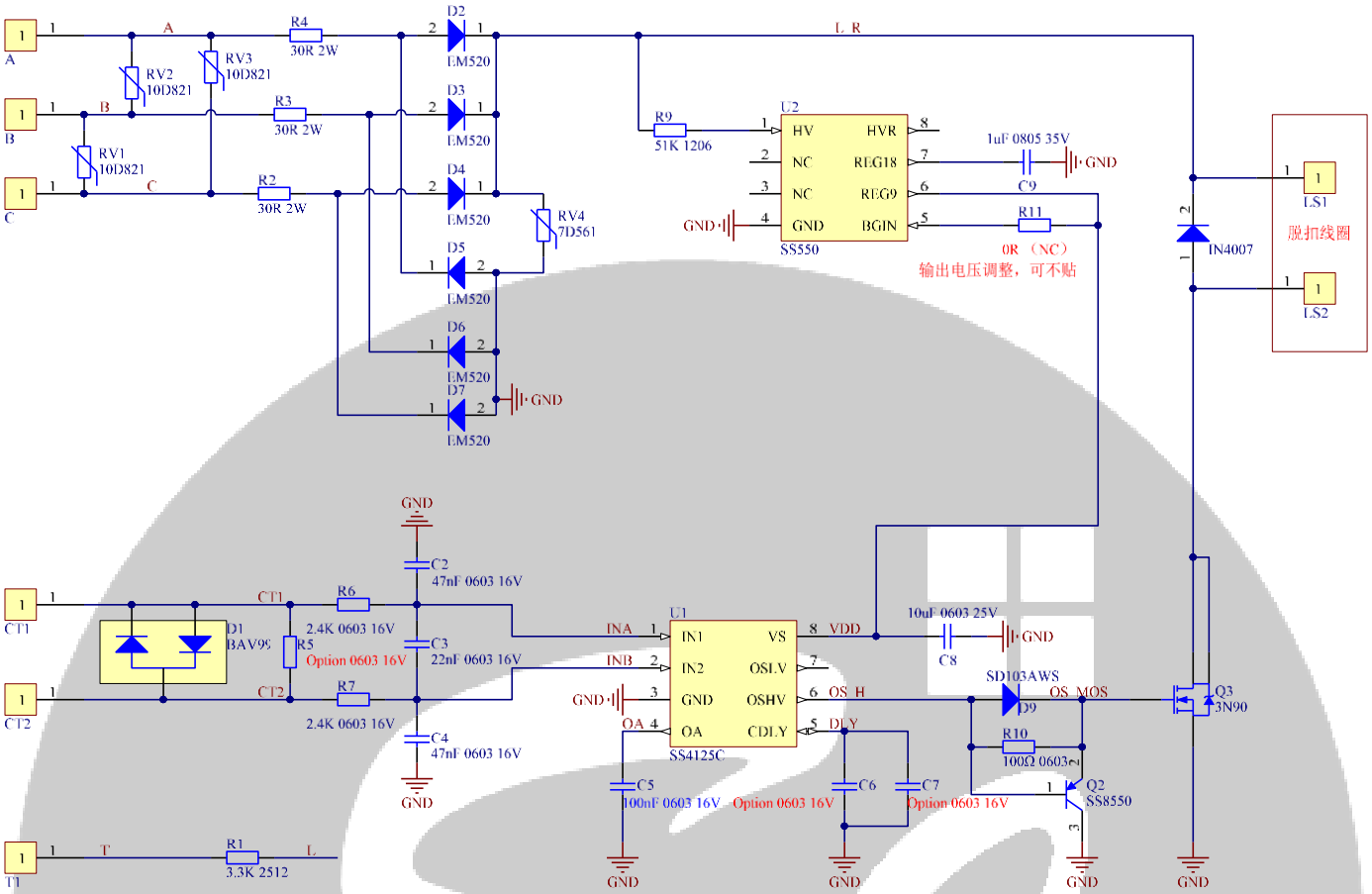


Figure 10. SS4125C 三相上、下进线应用典型电路

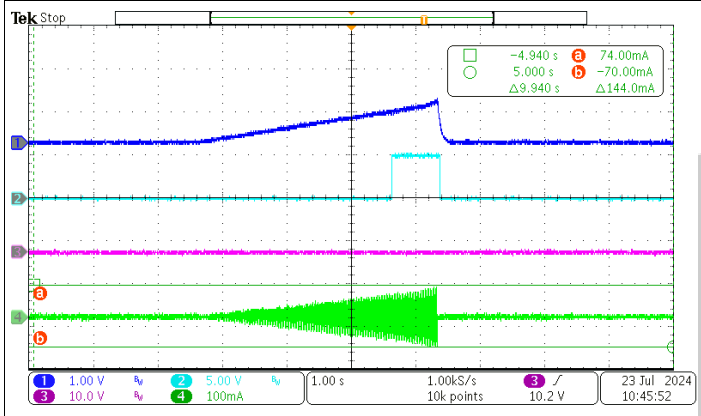
Table 5.三相上、下进线应用电路参数

延时电容					
	无延时	*0.1S*	*0.2S*	*0.5S*	*1S*
C_{OA}（图10 中的C5）	*100nF*	*100nF*	*100nF*	*100nF*	*100nF*
C_{DLY}（图10 中的C6+C7）	*33nF*	*150nF*	*220nF+47nF*	*470nF+150nF*	*1uF+220nF*
采样电阻（N=780）					
100mA			*51R（图10 中的R5）*		
300mA			*17R（图10 中的R5）*		
500mA			*10R（图10 中的R5）*		
*Note:**动作电流可通过调节采样电阻(R5)实现***					

TYPICAL PERFORMANCE CHARACTERISTICS

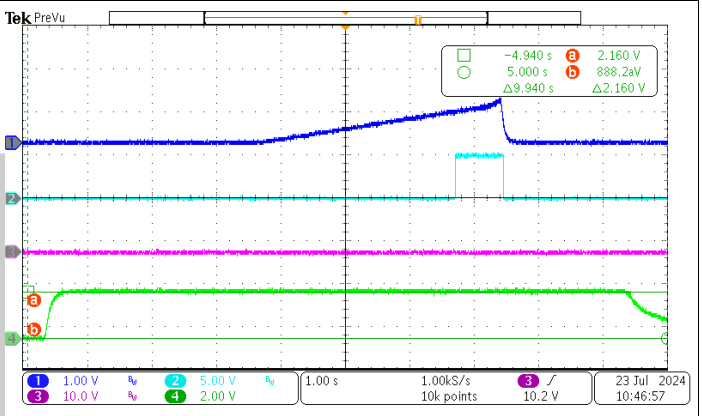
三相无延时漏电功能测试波形，外围参数参考 Table5，T_A = 25℃

Residual Current 50mA



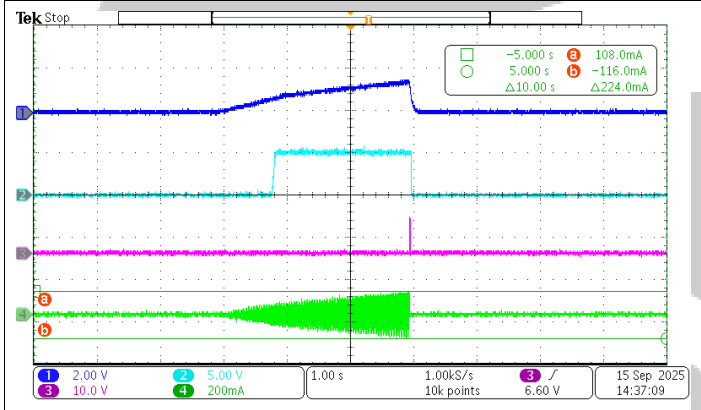
CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：LC,100mA/div

Residual Current 50mA



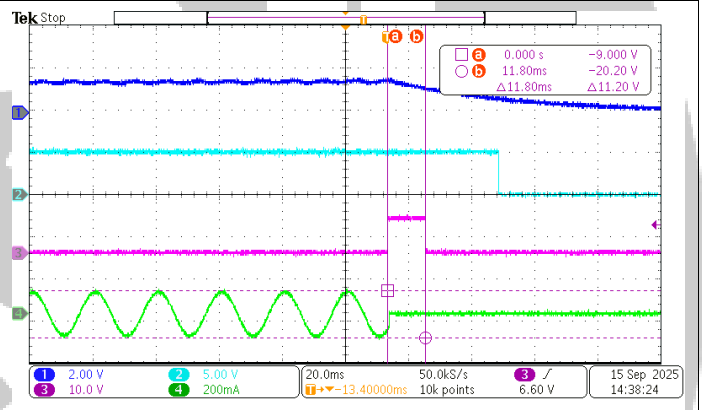
CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：CT2,2V/div

Residual Current Test 100mA(Whole-上进线)



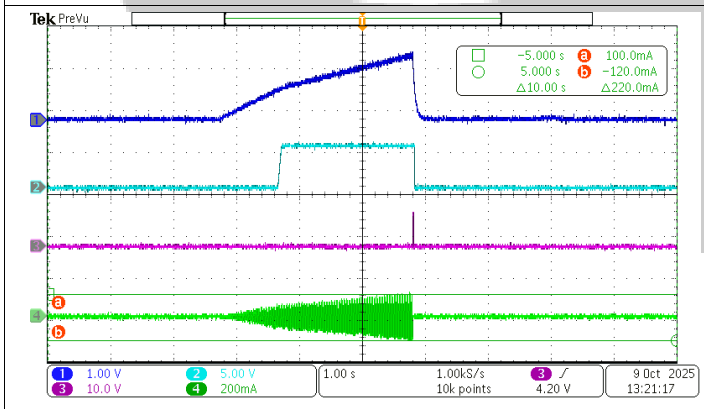
CH1：OA(Pin4),2V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div
Leakage Current:77.17mA　Time=3.08s

Residual Current Test 100mA(Part-上进线)



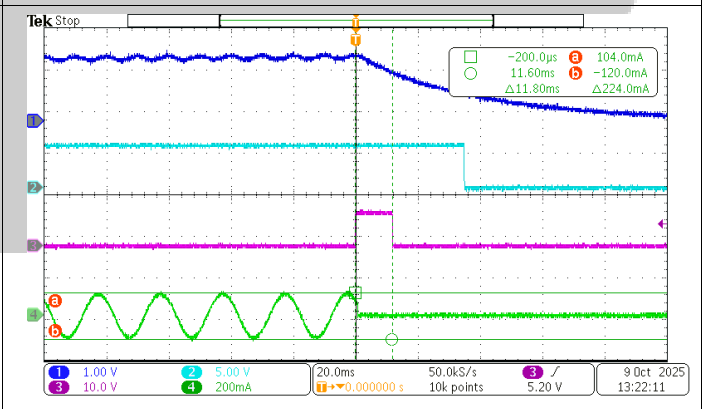
CH1：OA(Pin4),2V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div
Leakage Current:77.77mA　Time=3.98s

Residual Current Test 100mA(Whole-下进线)

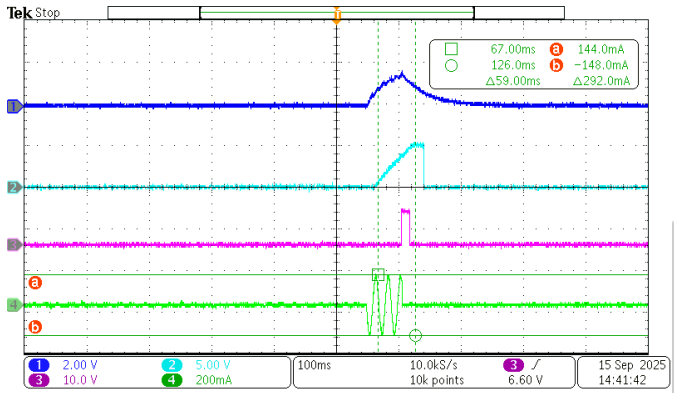
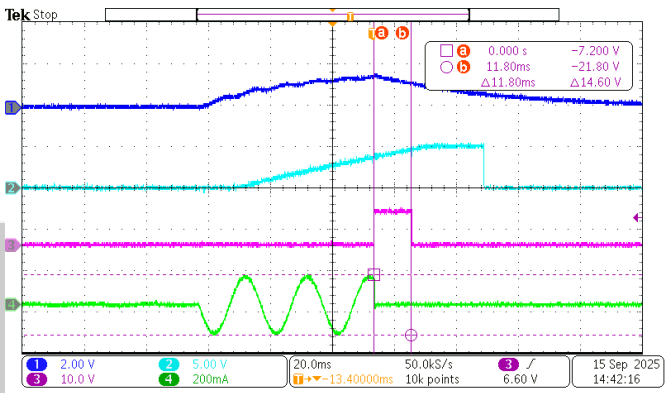
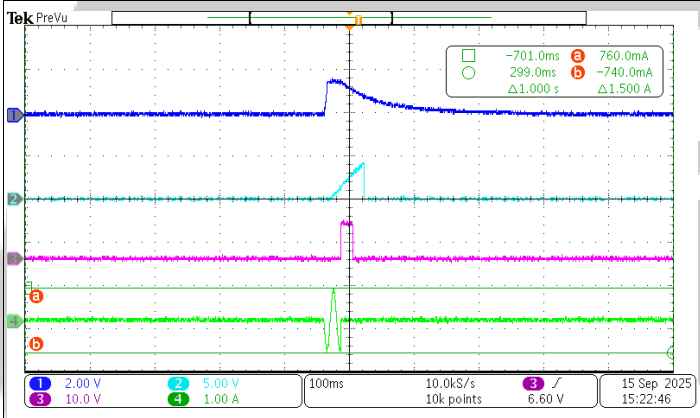
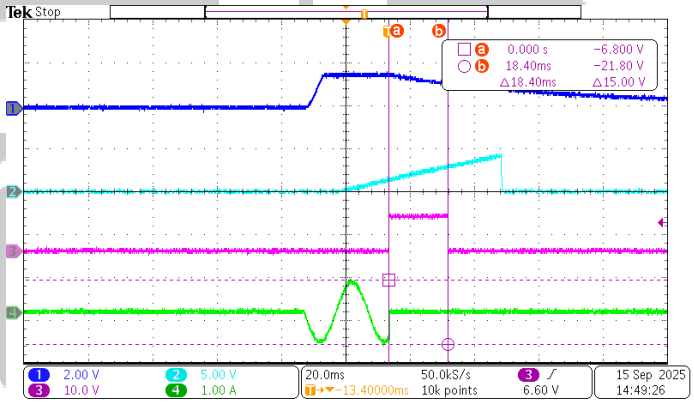
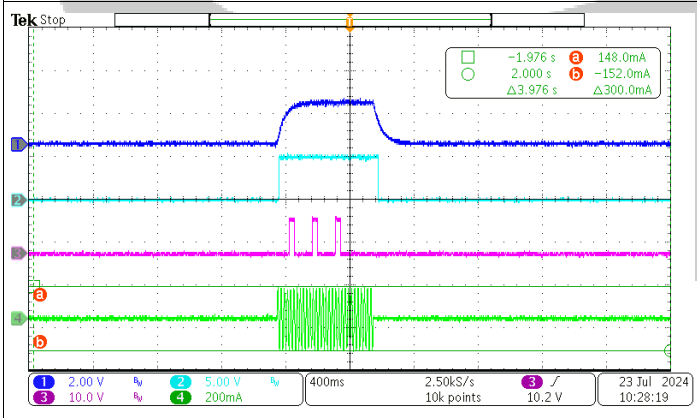
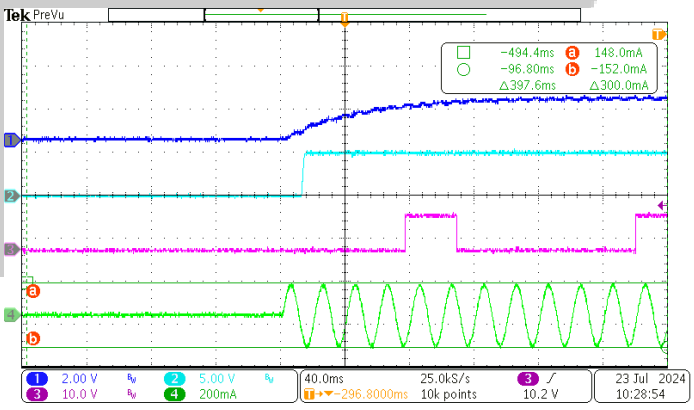


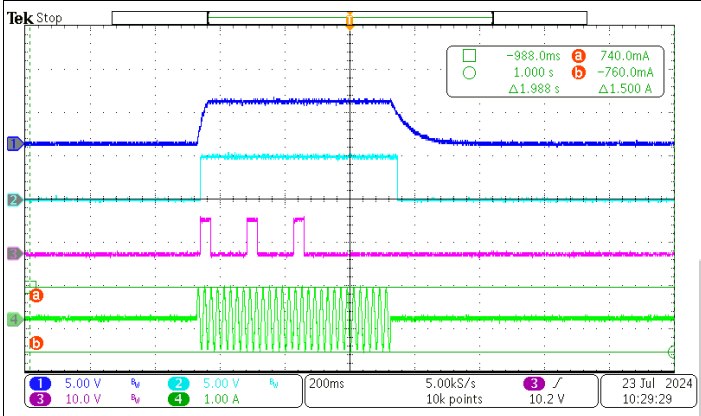
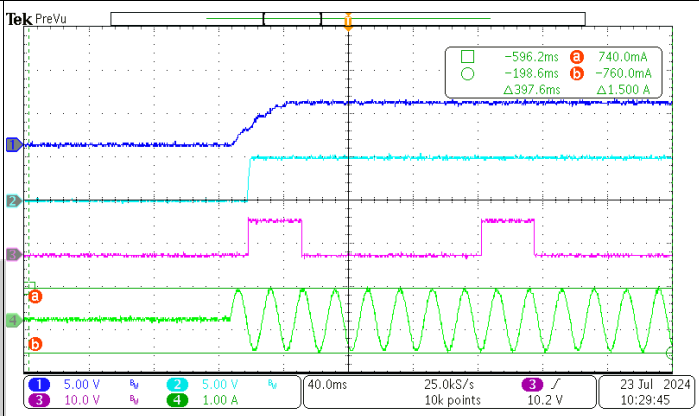
CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div
Leakage Current:77.33mA　Time=3.12s

Residual Current Test 100mA(Part-下进线)

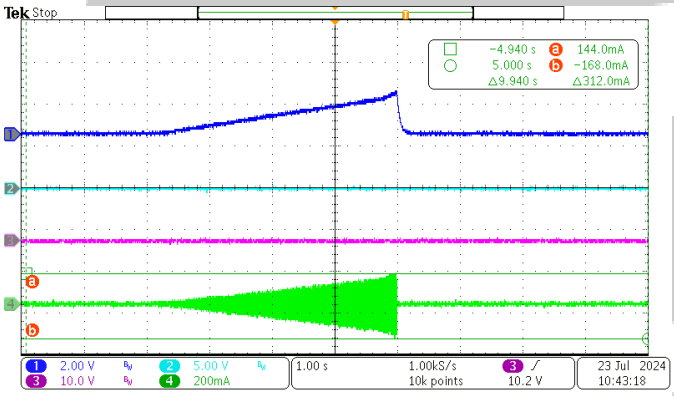
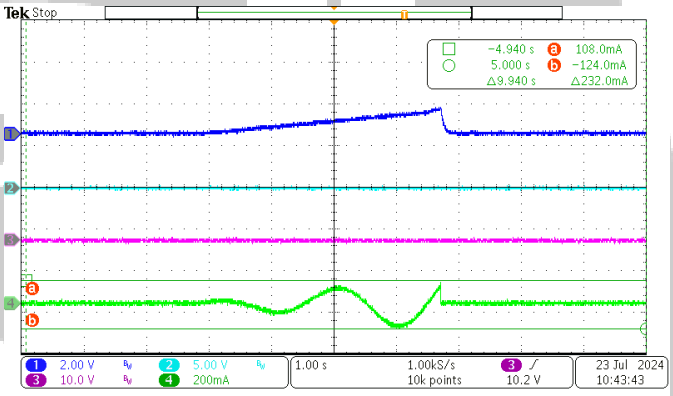
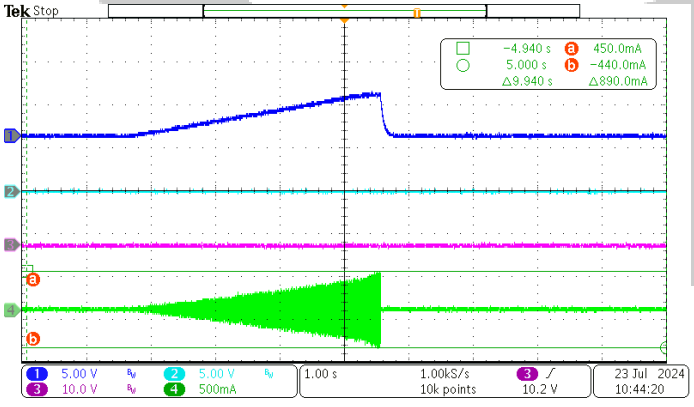
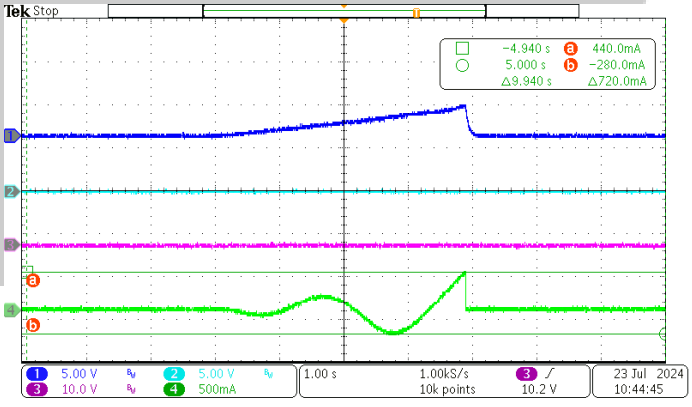


CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div
CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div
Leakage Current:77.34mA　Time=3.11s

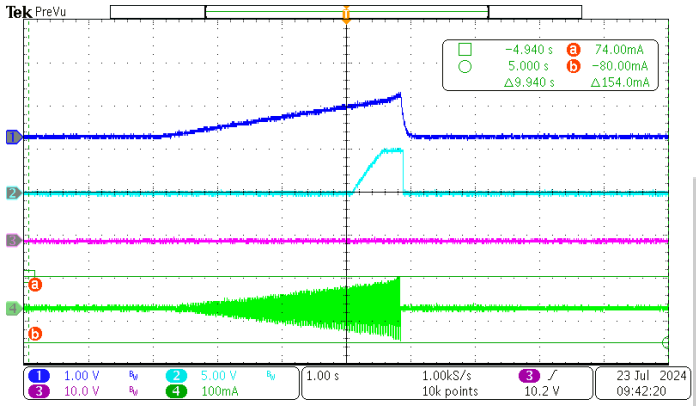
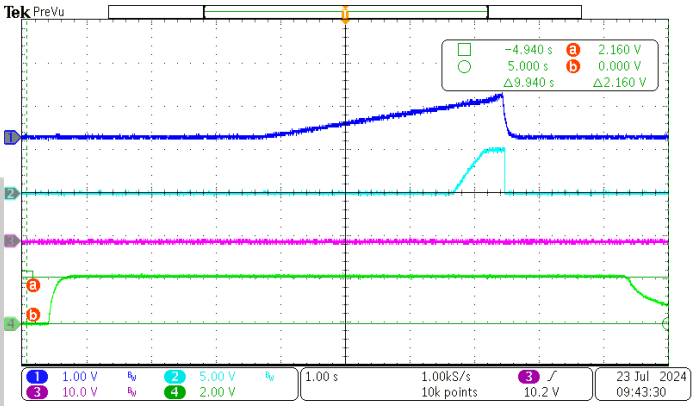
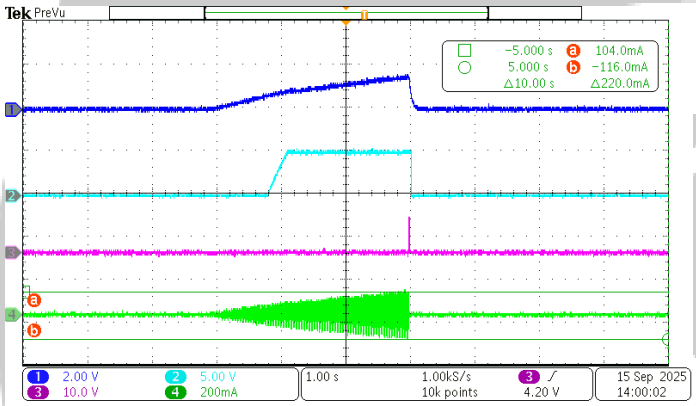
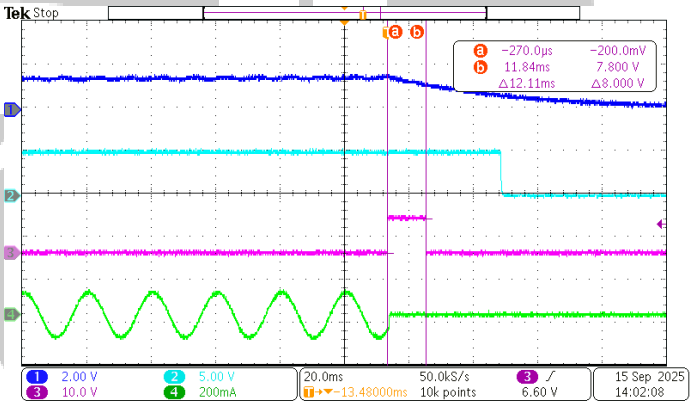
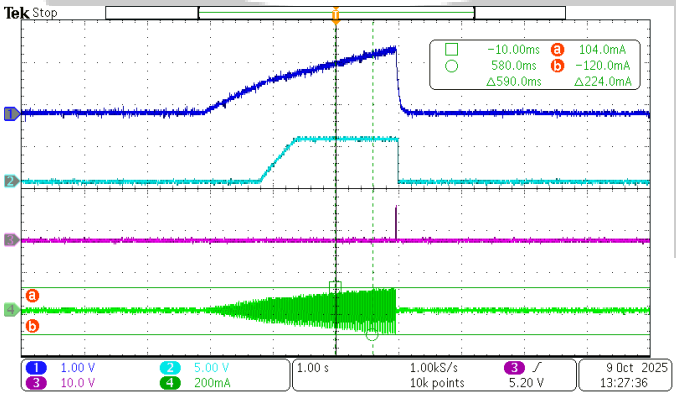
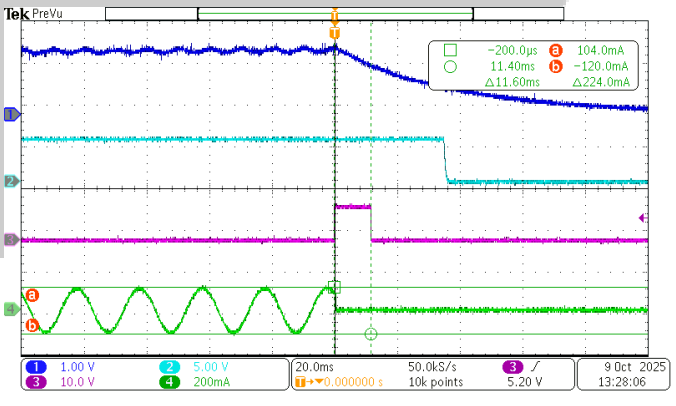
Release Time Test Residual Current 100mA(Whole)	Release Time Test Residual Current 100mA(Part)
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div Release Time:57ms	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div Release Time:56.9ms
Release Time Test Residual Current 500mA(Whole)	**Release Time Test Residual Current 500mA(Part)**
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,1A/div Release Time:27.2ms	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,1A/div Release Time:27ms
断开 MOS， Residual Current Test 100mA(Whole)	**断开 MOS， Residual Current 100mA(Part)**
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div

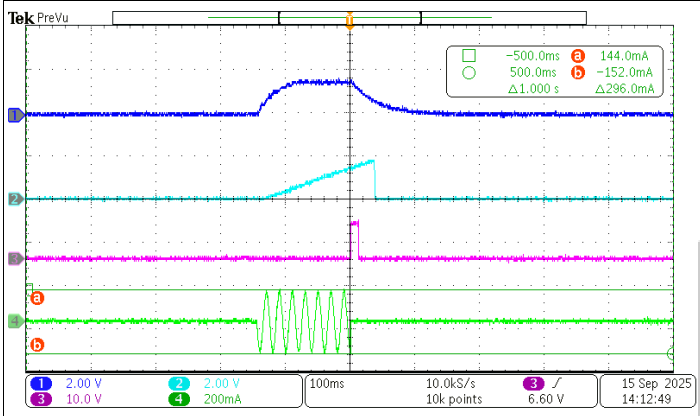
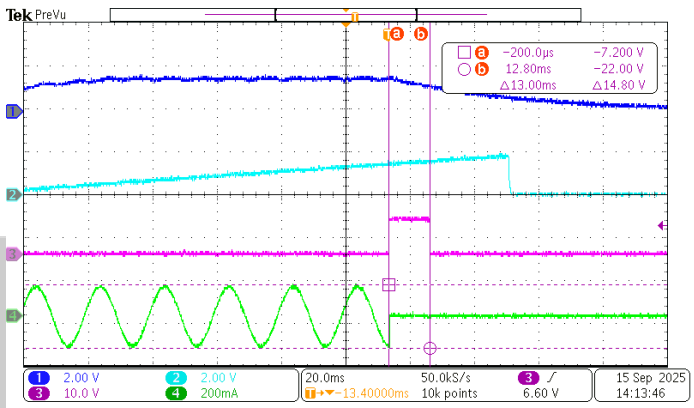
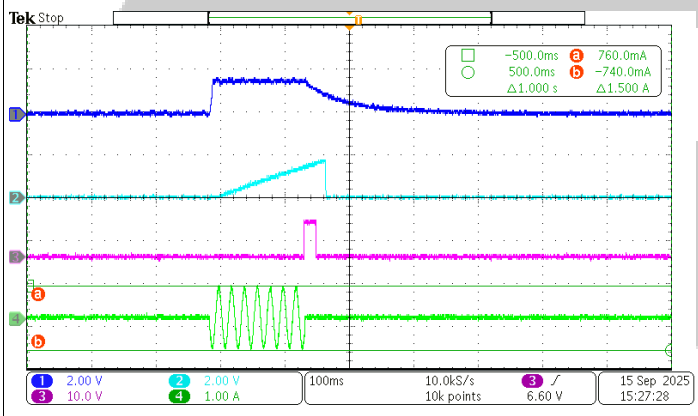
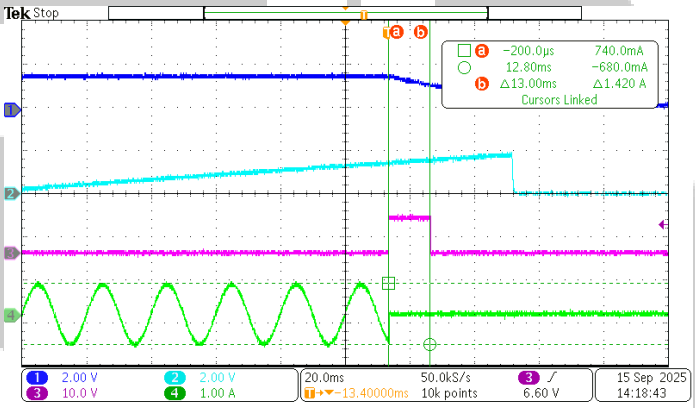
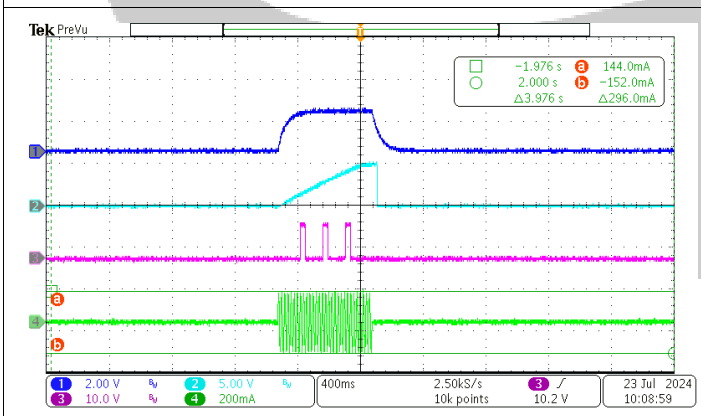
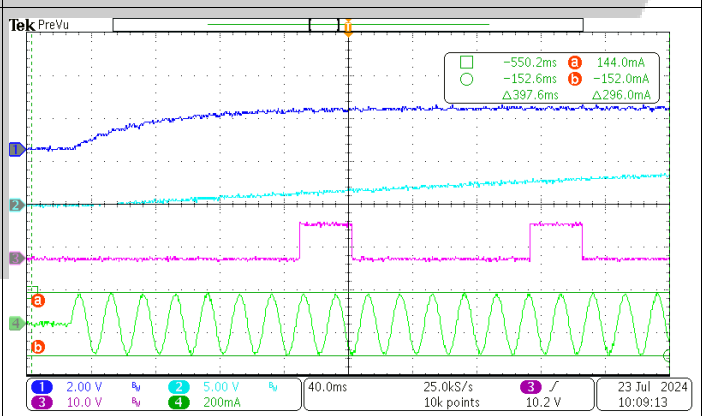
断开 MOS Residual Current 300mA(Whole)	断开 MOS Residual Current 300mA(Whole)
	
CH1：OA(Pin4),5V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,1A/div	CH1：OA(Pin4),5V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,1A/div

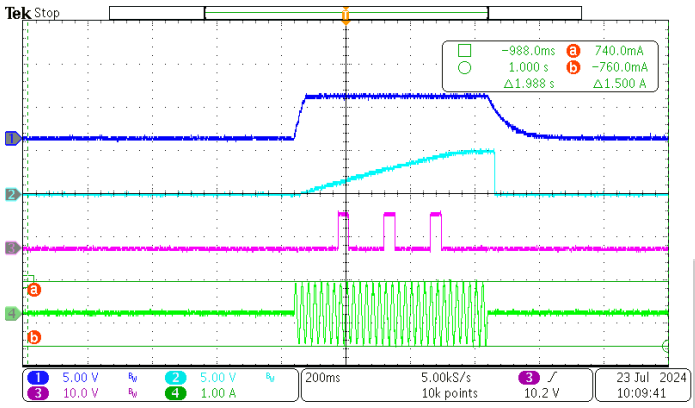
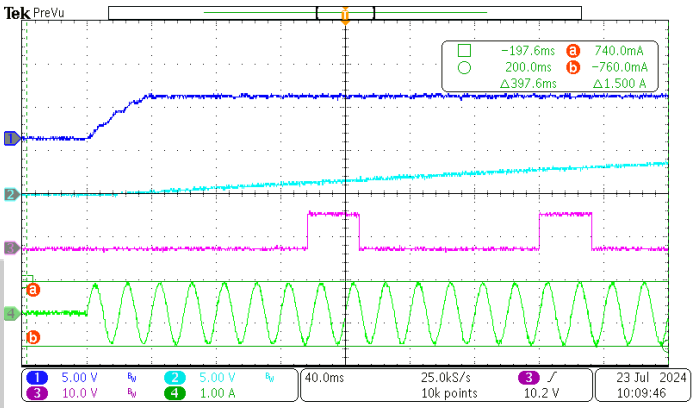
高频抑制功能波形

f=100Hz, Residual Current 100mA	f=1000Hz,Residual Current 100mA
	
CH1：OA(Pin4), 2V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div	CH1：OA(Pin4), 2V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div
f=100Hz, Residual Current 300mA	**f=1000Hz, Residual Current 300mA**
	
CH1：OA(Pin4), 5V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,500mA/div	CH1：OA(Pin4), 5V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,500mA/div

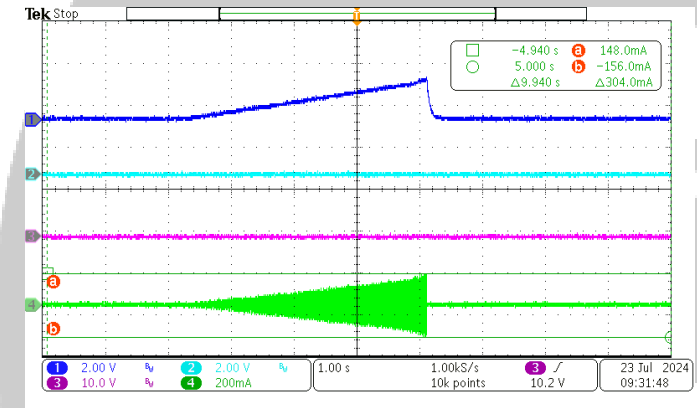
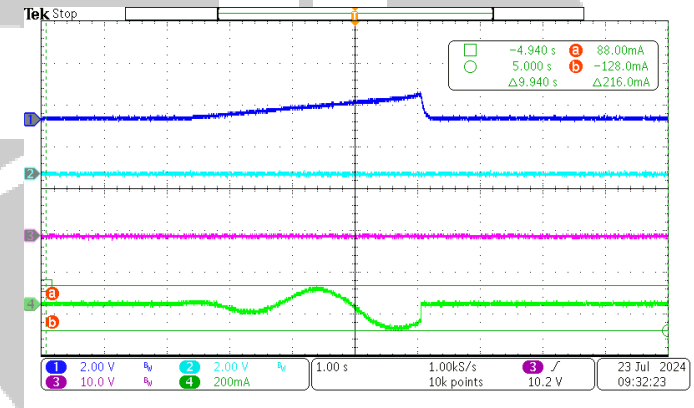
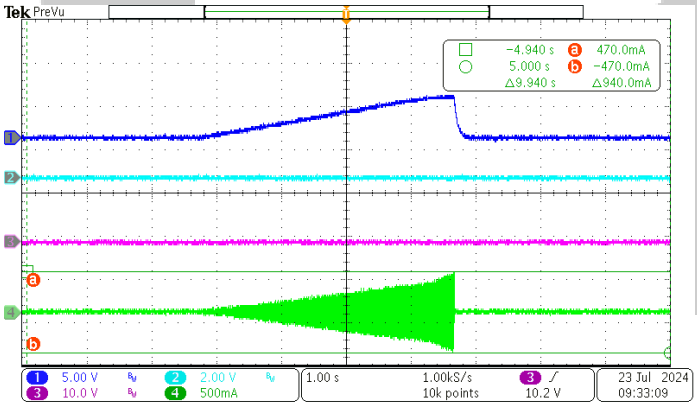
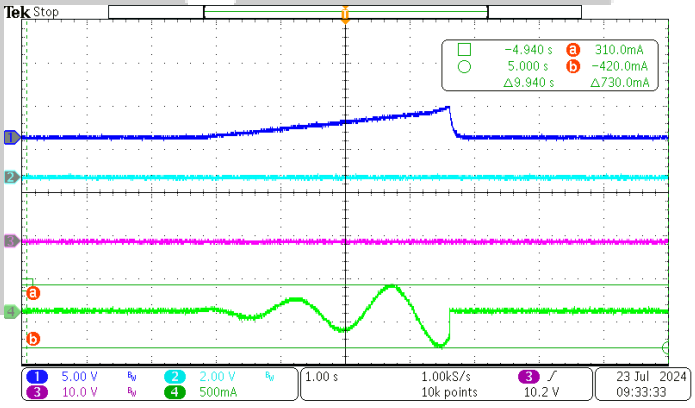
三相 0.2s 延时漏电功能测试波形，外围参数参考 Table5，T_A = 25℃

Residual Current 50mA	Residual Current 50mA
	
CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,100mA/div	CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：CT2,2V/div
Residual Current Test 100mA(Whole-上进线)	**Residual Current Test 100mA(Part-上进线)**
	
CH1：OA(Pin4),2V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div Leakage Current:77.16mA　Time=3.10	CH1：OA(Pin4),2V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div Leakage Current:77.04mA　Time=3.09s
Residual Current Test 100mA(Whole-下进线)	**Residual Current Test 100mA(Part-下进线)**
	
CH1：OA(Pin4), 1V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div Leakage Current:77.26mA　Time=3.13	CH1：OA(Pin4),1V/div　CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div　CH4：LC,200mA/div Leakage Current:77.22mA　Time=3.10s

Release Time Test Residual Current 100mA(Whole)	Release Time Test Residual Current 100mA(Part)
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),2V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div Release Time:145.7ms	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),2V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div Release Time:145ms
Release Time Test Residual Current 500mA(Whole)	**Release Time Test Residual Current 500mA(Part)**
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),2V/div CH3：OSH(Pin6),10V/div CH4：LC,1A/div Release Time:134.4ms	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),2V/div CH3：OSH(Pin6),10V/div CH4：LC,1A/div Release Time:143.9ms
断开 MOS，Residual Current Test 100mA(Whole)	**断开 MOS，Residual Current 100mA(Part)**
	
CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div	CH1：OA(Pin4),2V/div CH2：DLY(Pin5),5V/div CH3：OSH(Pin6),10V/div CH4：LC,200mA/div

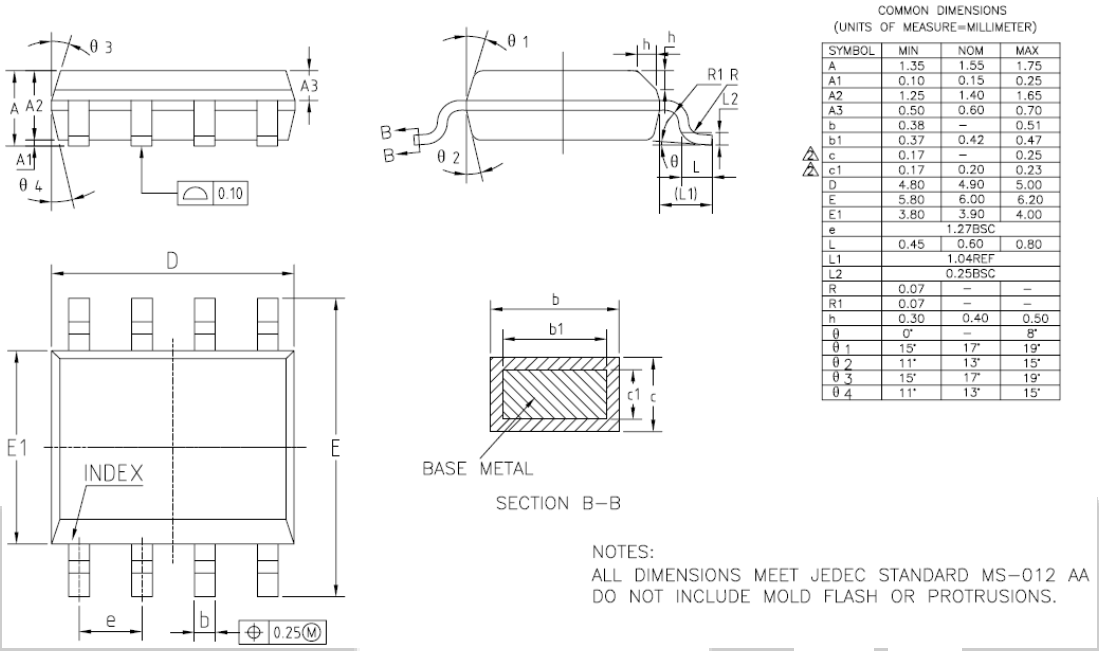
断开 MOS， Residual Current 500mA(Whole)	断开 MOS， Residual Current 500mA(Whole)
	
CH1： VS(Pin4),5V/div CH2： DLY(Pin5),5V/div CH3： OSH(Pin6),10V/div CH4： LC,1A/div	CH1： VS(Pin4),5V/div CH2： DLY(Pin5),5V/div CH3： OSH(Pin6),10V/div CH4： LC,1A/div

高频抑制功能波形

f=100Hz, Residual Current 100mA	f=1000Hz,Residual Current 100mA
	
CH1： OA(Pin4), 2V/div CH2： DLY(Pin5),2V/div CH3： OSH(Pin6),10V/div CH4： LC,200mA/div	CH1： OA(Pin4), 2V/div CH2： DLY(Pin5),2V/div CH3： OSH(Pin6),10V/div CH4： LC,200mA/div
f=100Hz, Residual Current 300mA	**f=1000Hz, Residual Current 300mA**
	
CH1： OA(Pin4),5V/div CH2： DLY(Pin5),2V/div CH3： OSH(Pin6),10V/div CH4： LC,500mA/div	CH1： OA(Pin4),5V/div CH2： DLY(Pin5),2V/div CH3： OSH(Pin6),10V/div CH4： LC,500mA/div

Note：断开 MOS 测试是指断开供电与 MOS 之间连接通路

OUTLINE DIMENSIONS



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

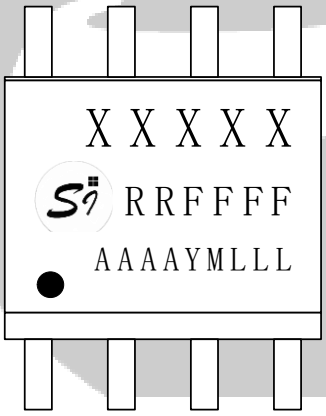
SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°

Figure 11. 8-Lead Small Outline Package [SOP]

Dimensions show in millimeters

ORDERING GUIDE

型号	封装形式	温度范围	MK code	包装方式	卷盘尺寸
SS4125C	SOP8	-40℃ to +125 ℃	4125C G3PPDA AAAAYMLLL	3000/盘	13 寸卷盘



1、SI =Logo;
2、• =Pin1;
3、XXXXX =Device name ;
4、RR =Product version;
5、FFFF =Function;
6、AAAA =Company Encode;
7、YM =Year&Month;
8、LLL =Trace No.

注：本公司保留不预先通知而修改此文件的权利

版本更新

版本号	发布日期	页数	章节或图表	更改说明
1.0	2025.06	16		首次发布
1.1	2025.10	16	Table5、应用波形图	更新测试波形