Features

- Operating voltage range：4.5V to 28V
- Load current limitation
- Output short-circuit protection
- Standby current <1.0μA
- On-state resistance Typ=145mΩ
- Thermal shutdown indication
- OFF-state open-load detection
- Overvoltage clamp
- Undervoltage protection
- Multiplexed analog feedback of load current with high precision proportional current mirror
- RoHS compliant and lead free

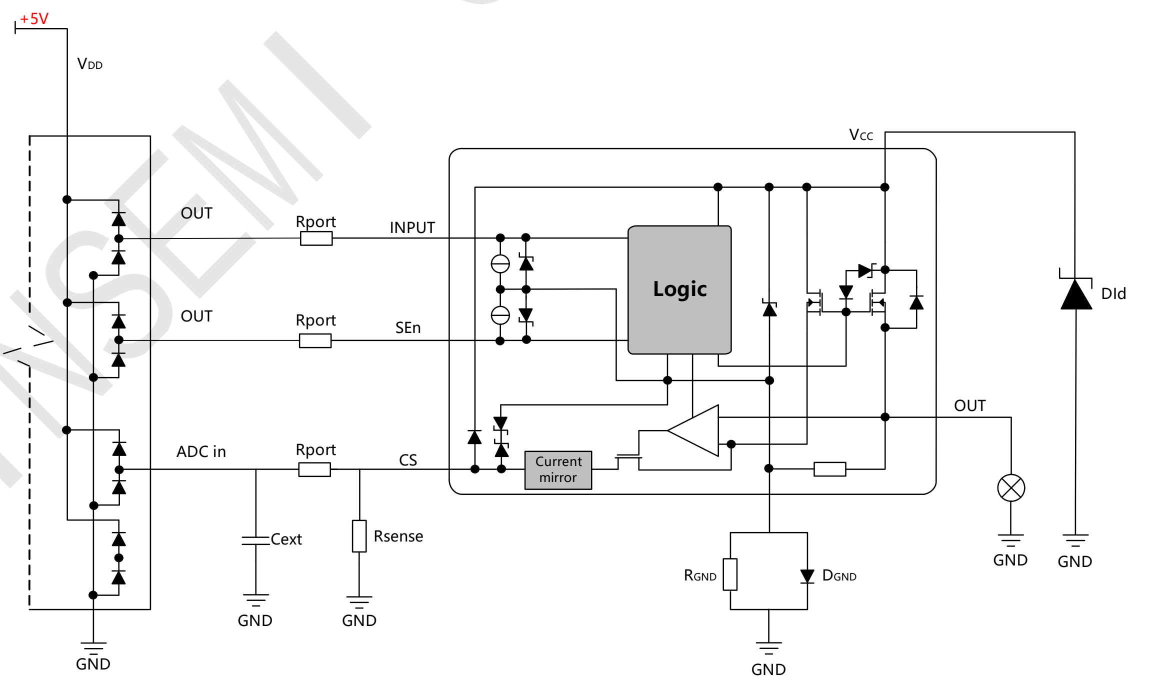
Application

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps

General Description

- WS7140S is single channel high-side drivers with current sense analog feedback for automotive applications, the devices are designed to drive 12 V automotive grounded loads through a 3 V and 5 V.
- WS7140S integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.
- A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.
- A sense enable pin allows OFF-state diagnosis to be disabled during the module low power mode as well as external sense resistor sharing among similar devices.
- WS7140S is available in ESOP-8L package.

Typical Application Circuit

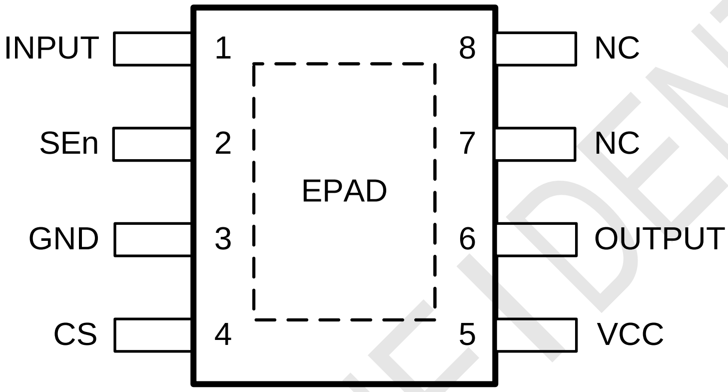


Ordering Information

Package	Top Mark	Part No.
8-Pin ESOP-8L, Pb-free	WS7140S XXYMXX	WS7140S

Pin Configuration

Top view



ESOP-8L

Pin Description

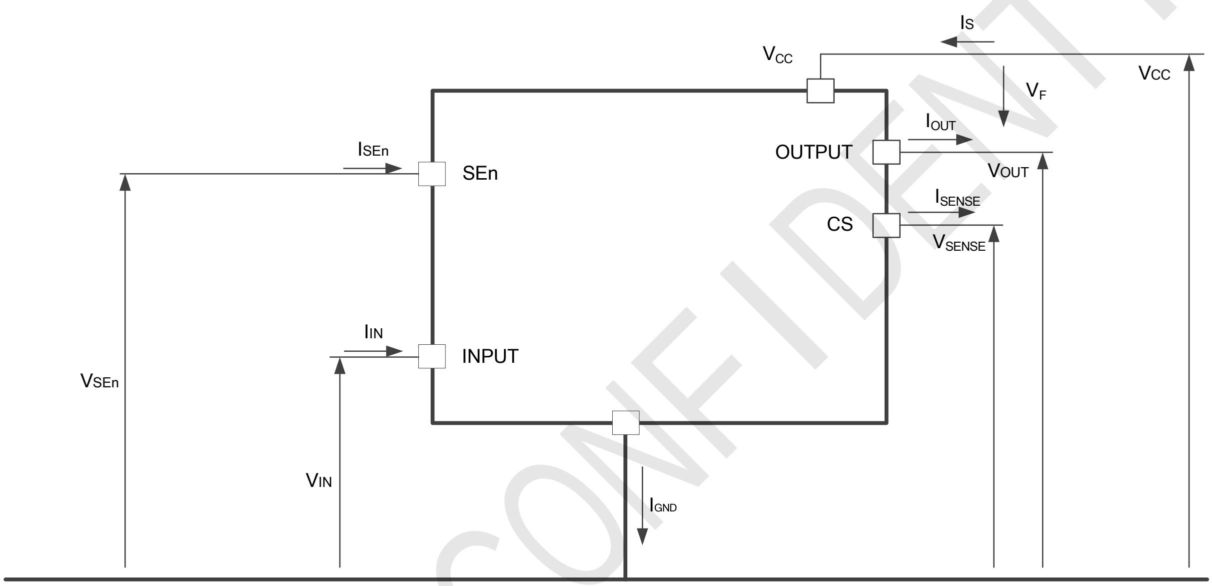
Pin Name	Pin NO.	Pin Description
INPUT	1	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
SEn	2	Active high compatible with 3 V and 5 V CMOS outputs pin, it enables the CS diagnostic pin.
GND	3	Ground connection. Must be reverse battery protected by an external diode / resistor network.
CS	4	Multiplexed analog sense output pin; it delivers a current proportional to the load current.
V_{CC}	5	Battery connection.
OUTPUT	6	Power outputs.
NC	7/8	No connect.
EPAD	EPAD	Exposed pad for thermal dissipation enhancement. Must be soldered on the large ground plane on the PCB to increase the thermal dissipation. The pad must be connected to GND electrically.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	CS	OUTPUT	INPUT	SEn
Floating	Not allowed	X	X	X
To ground	Through 1K resistor	Not allowed	Through 15K resistor	Through 15K resistor

Note1：X do not care.

Current and Voltage Conventions



Note2: $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	35	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
V_{IN}, V_{SEn}	INPUT, SEn DC input voltage	-0.3 to 6.0	V
I_{SENSE}	CS pin DC output current	20	mA
	CS pin DC output current in reverse	-20	
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

ESD Susceptibility (Note4)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$[3]	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_{CC} connected (HBM)	±4	kV
$V_{ESD(CDM)}$[4]	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 4, 5, 8)	±750	V

Note4：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002.

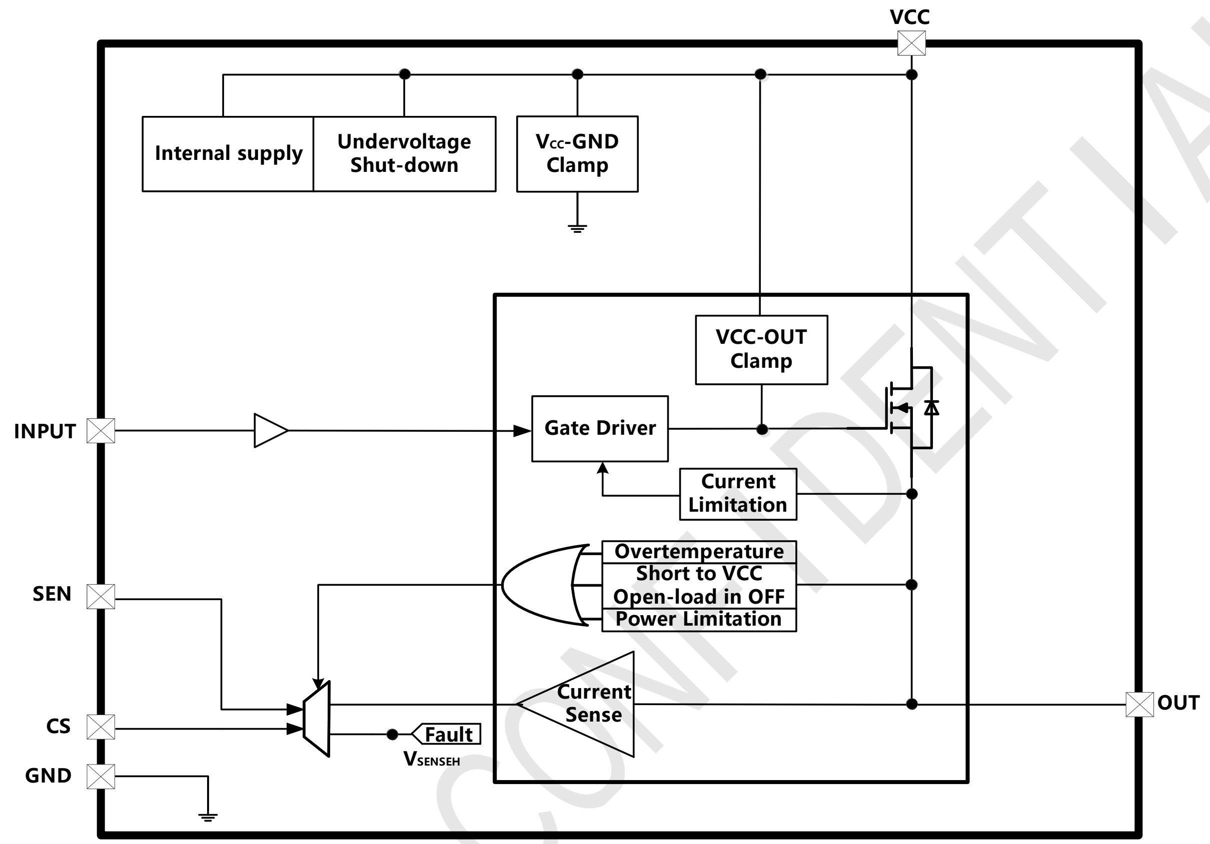
4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011.

Thermal Resistance (Note5)

Symbol	Parameter	Value	Unit
T_{JA}	Junction-to-Ambient Thermal Resistance	43	℃/W

Note5：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Functional Block



Electrical Characteristics (Note6)

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{CC}		4.5	13	28	V
Under voltage shutdown	V_{USD}				4.5	V
Under voltage shutdown reset	$V_{USDReset}$				5	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=1A, T_j = 25℃		145		mΩ
		I_{OUT}=1A, T_j =150℃			280	
		I_{OUT}=1A, V_{CC} =4.5V, T_j = 25℃			240	
Nominal load current	$I_{L(NOM)}$	T_A=25℃		2.0		A
Nominal load current at T_A=85℃	$I_{L(NOM)\_85}$	T_A=85℃, T_j < 150℃		1.8		A
Inverse Current Capability	$I_{L(INV)}$	V_{CC}<V_{OUT}, V_{IN}=5V, T_A=25℃		2.0		A
V_{CC} clamp voltage	V_{CLAMP}	I_S=20 mA, 25℃ < T_j < 150℃	35	42	48	V
		I_S=20 mA, T_j =-40℃	33			
Supply current in standby at V_{CC} = 13 V	I_{STBY}	V_{CC} = 13V, V_{IN}=V_{OUT}=V_{SEn}=0V, T_j =25℃			1.0	μA
		V_{CC} =13V, V_{IN}=V_{OUT}=V_{SEn} =0V, T_j= 125℃			3.0	μA
Standby mode blanking time	t_{D_STBY}	V_{CC}=13V, V_{IN}=V_{OUT}=0V，V_{SEn}=5 V to 0 V	100	450	900	us
Supply current	$I_{S(ON)}$	V_{CC}=13V, V_{SEn}=0V, V_{IN}=5V, I_{OUT}=0A		3	6	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_{CC}=13V, V_{SEn}=5V, V_{IN}=5V, I_{OUT}=1A			6	mA
Off-state output current at V_{CC} =13V	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_{CC} =13V, T_j =25℃	0	0.05	0.5	μA
		V_{IN} =V_{OUT}=0V, V_{CC} =13V, T_j =125℃	0		3.0	μA
Output - V_{CC} diode voltage at T_j=150℃	V_F	I_{OUT} =-0.2A, T_j =150℃			0.9	V

Switching/V_{CC} = 13 V, -40℃ < T_j< 150℃, unless otherwise specified

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	R_L=13Ω	10	35	120	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$		10	60	120	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	R_L=13Ω	0.05	0.2	0.7	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		0.05	0.45	0.7	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	R_L=13Ω	-60	-10	60	us

Logic input (IN, SEn)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_L				0.9	V
Low level logic input current	I_L	V_{INL}=0.9V	0.5			uA
Logic input high level voltage	V_H		2.1		6.0	V
High level logic input current	I_H	V_{INH}=2.1V			12	uA
Logic input hysteresis voltage	$V_{(hyst)}$		0.1	0.3	0.7	V

Protections (7 V < V_{CC}< 18 V, -40℃ < T_j < 150℃)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
DC short circuit current	I_{LIMH}	V_{CC}=13V	4	6	10	A
		4.5V < V_{CC}< 16V			10	
Short circuit current during thermal cycling	I_{LIML}	V_{CC}=13V, T_R< T_j< T_{TSD}		2		
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃, V_{CC}=13V		60		℃
Current limit thermal hysteresis	T_R			40		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=1A, L= 6mH, T_j = -40℃	V_{CC}-33			V
		I_{OUT}=1A, L= 6mH, T_j =25℃ to 150℃	V_{CC}-35	V_{CC}-38	V_{CC}-43	

Current sense / 7 V < V_{CC}< 18 V, -40℃ < T_j < 150℃						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Current sense clamp voltage	V_{SENSE_CL}	V_{SEn}=0V, I_{SENSE} =1mA		-15		V
		V_{SEn}=0V, I_{SENSE} = -1mA		7		

Current sense characteristics						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{OUT}/I_{SENSE}	K_1	I_{OUT}=0.15A, V_{SEn}=5V	-50%	530	+50%	
I_{OUT}/I_{SENSE}	K_2	I_{OUT}=0.7A, V_{SEn}=5V	-15%	520	+15%	
I_{OUT}/I_{SENSE}	K_3	I_{OUT}=1A, V_{SEn}=5V	-10%	520	+10%	
I_{OUT}/I_{SENSE}	K_4	I_{OUT}=2A, V_{SEn}=5V	-8%	520	+8%	
Current sense leakage current	I_{SENSE0}	CS disabled: V_{SEn} =0V	0		0.5	uA
		CS disabled: -1V<V_{SENSE}<5V	-0.5		3	
		CS enabled: V_{SEn}=5V, V_{IN}= 5V, I_{OUT}=0A	0		100	
		CS enabled: V_{SEn}=5V, V_{IN}= 0V, I_{OUT}=0A	0		2	
Output voltage for CS shutdown	V_{OUT_MSD}	V_{SEn}=5V, R_{SENSE} =2.7K, V_{IN}=5V, I_{OUT}=1A		5		V
CS saturation voltage	V_{SENSE_SAT}	V_{CC}=7V,R_{SENSE}=2.7K,V_{SEn}=5V,V_{IN}=5V, I_{OUT} =2A, T_j =150 ℃	5			V
CS saturation current	I_{SENSE_SAT}	V_{CC}=7V, V_{SENSE}=4V, V_{IN}=5V, V_{SEn}=5V, T_j =150℃	4			mA
Output saturation current	I_{OUT_SAT}	V_{CC}=7V, V_{SENSE}=4V, V_{IN}=5V, V_{SEn}=5V, T_j =150 ℃	2.2			A

OFF-state diagnostic						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
OFF-state open load voltage detection threshold	V_{OL}	V_{SEn}=5V, V_{IN}=0V	2	3	4	V
OFF-state output sink current	$I_{L(off2)}$	V_{IN} = 0 V, V_{OUT} = V_{OL},T_j = -40℃ to 150℃	-450	-200	-80	uA
OFF-state diagnostic delay time from falling edge of INPUT	t_{DSTKON}	V_{SEn}=5V, V_{IN}= 5V to 0 V, V_{OUT}=4V, I_{OUT} =0A	100	350	700	us

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	$t_{D\_OL\_V}$	V_{IN}=0V, V_{OUT}=4V, V_{SEn} = 0V to 5V			150	us
OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	V_{SEn}=5V,V_{IN}=0V, V_{OUT}=0V to 4V		5	30	us

Fault diagnostic feedback

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense output voltage in fault condition	V_{SENSEH}	V_{CC}=13V, R_{SENSE} =1K, V_{IN}=0V, V_{SEn} = 5V, I_{OUT}=0A, V_{OUT}=4V	5.0	6.0	6.6	V
Current sense output current in fault condition	I_{SENSEH}	V_{CC}=13V, V_{SENSE} =5V	10	20	30	mA

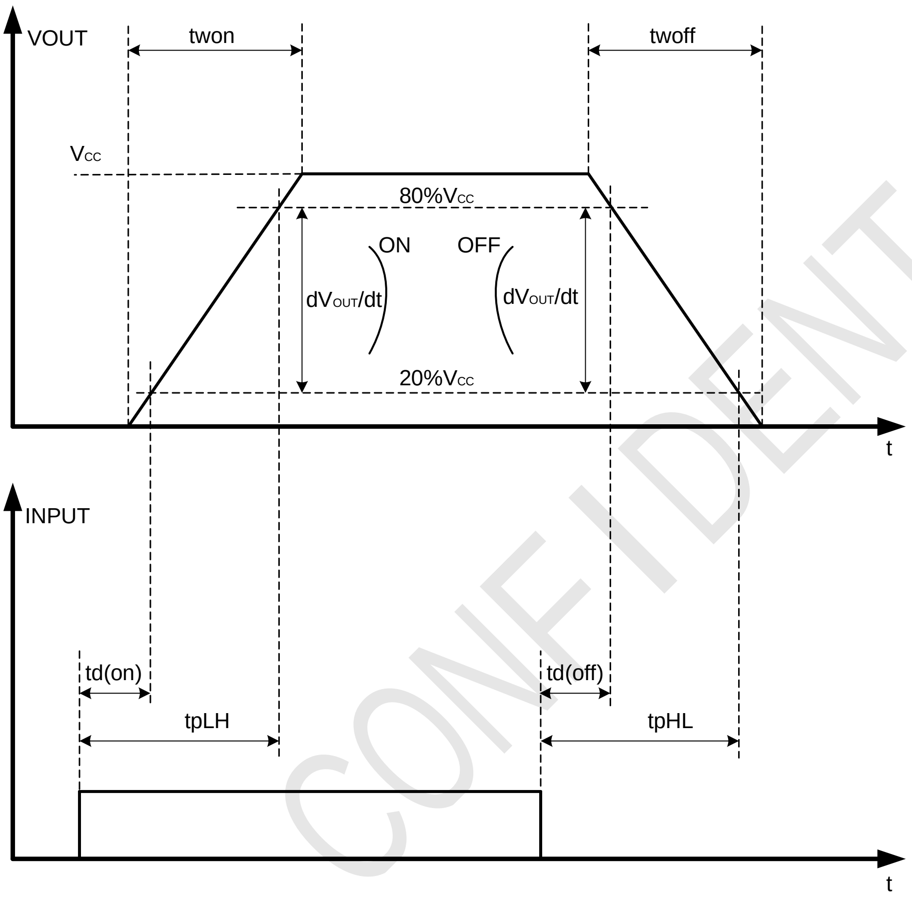
Current sense timings

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense settling time from rising edge of SEn	$t_{DSENSE1H}$	V_{IN}=5V, V_{SEn}=0V to 5V, R_{SENSE}=1K, R_L=13Ω			60	us
Current sense disable delay time from falling edge of SEn	$t_{DSENSE1L}$	V_{IN}=5V, V_{SEn}=5V to 0V, R_{SENSE}=1K, R_L=13Ω		5	20	us
Current sense settling time from rising edge of INPUT	$t_{DSENSE2H}$	V_{IN}=0V to 5V, V_{SEn}=5 V, R_{SENSE} =1K, R_L=13Ω		60	150	us
Current sense settling time from rising edge of I_{OUT}(dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$	V_{IN}=5V,V_{SEn}=5V,R_{SENSE}=1K, I_{SENSE}=90% of $I_{SENSEMAX}$, R_L=13Ω			150	us
Current sense turn-off delay time from falling edge of INPUT	$t_{DSENSE2L}$	V_{IN}=5V to 0V, V_{SEn}=5V, R_{SENSE}=1K, R_L=13Ω		100	250	us

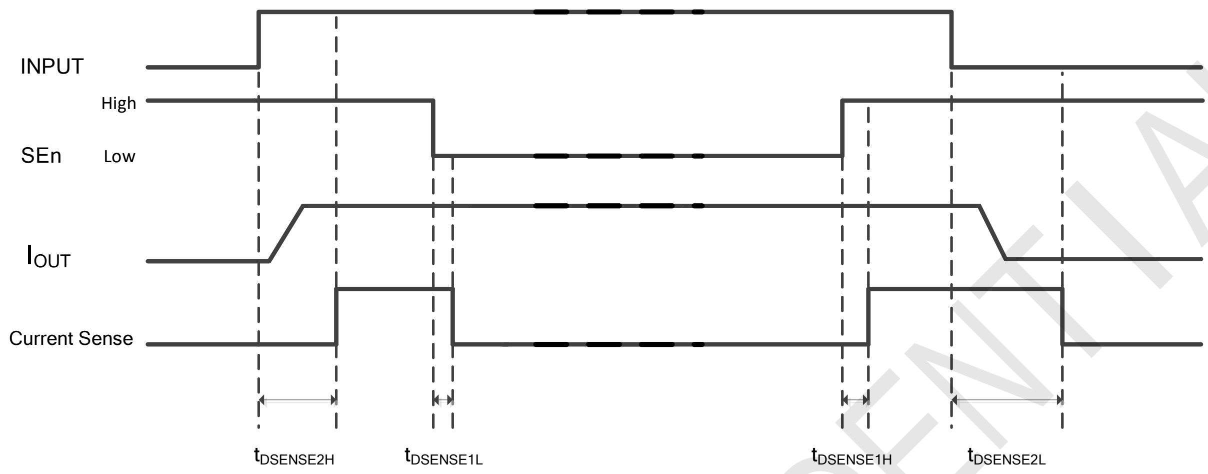
Note6: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

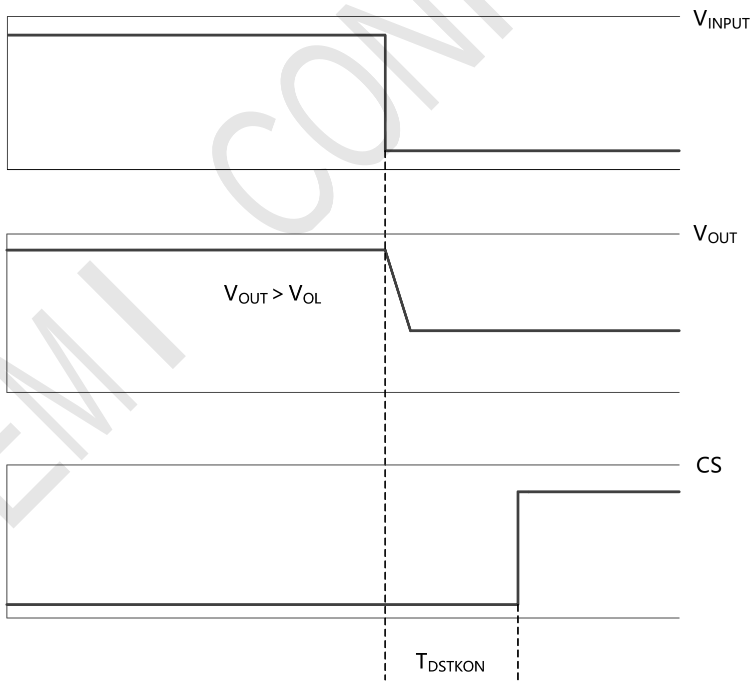


Table 2. Truth table

Mode	Conditions	IN	SEn	OUT	Current sense	Comments
Standby	All logic INs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150℃$	L	See Table 3	L	See Table 3	
		H		H	See Table 3	
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	See Table 3	L	See Table 3	
		H		H	See Table 3	Output cycles with temperature hysteresis
Undervoltage	$V_{CC} < V_{USD}$	X	X	L	Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	See Table 3	H	See Table 3	
	Open-Load	L		H	See Table 3	External pull-up
Negative output voltage	Inductive loads turn-off	L	See Table 3	<0	See Table 3	

Table 3. Current sense output

SEn	MUX Channel	Current sense output			
		Normal	Overload	OFF-state	Negative output
L		Hi-Z			
H	Channel diagnostic	$I_{SENSE} = I_{OUT}/K$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z

Functional Description

Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175℃), it automatically switches off and the diagnostic indication is triggered.

Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

Diode (D_{GND}) in the ground line

A resistor (typ.R_{GND}=4.7K) should be inserted in parallel to D_{GND} if the device drives an inductive load. This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. WS suggests to insert a resistor (R_{prot}=15K) in line both to prevent the micro-controller I/O pins from latching-up and to protect the HSD inputs. The value of these resistors is a compromise between the leakage current of micro-controller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of micro-controller I/Os.

CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the current mirror of channel output current. The signal are routed through an analog multiplexer which is controlled by mean of SEn pin, according to the address map in CS multiplexer addressing Table.

Current monitor

When current mode is selected in the CS, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE}*I_{SENSE} = R_{SENSE}*I_{OUT}/K$

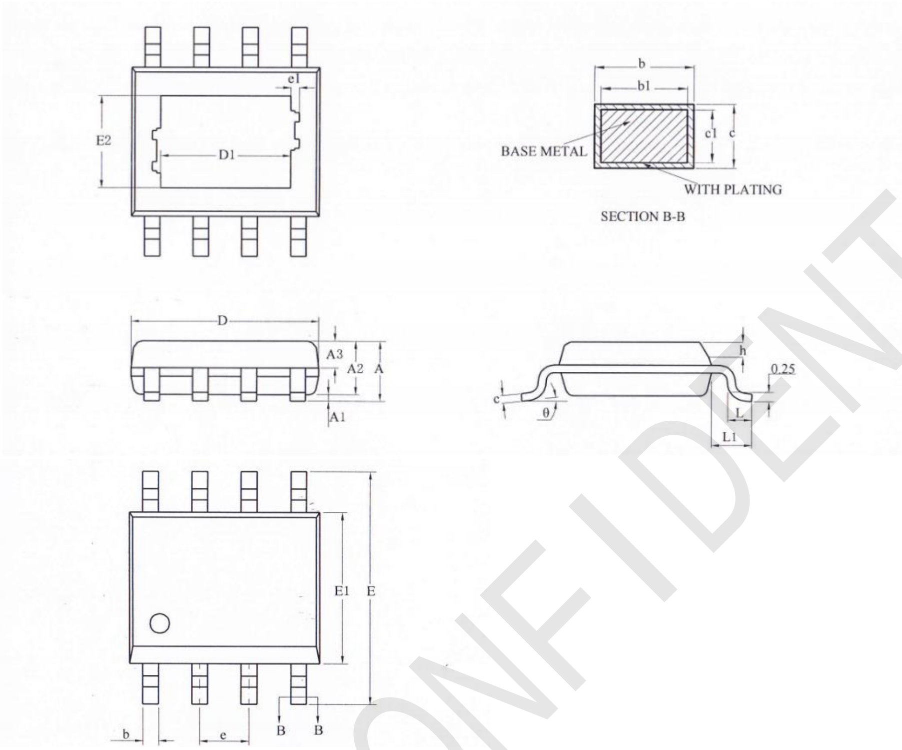
Where:

- V_{SENSE} is voltage measurable on R_{SENSE} resistor

I_{SENSE} is current provided from CS pin in current output mode

Package Outline

ESOP-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.65
A1	0.05		0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39		0.47
b1	0.38	0.41	0.44
c	0.20		0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
D1	3.10REF		
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.21REF		
e	1.27BSC		
h	0.25		0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0		8°

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