

SQS484CENW-T1_GE3-VB Datasheet

N-Channel 40V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^f	Q_g (TYP.)
40	0.013 at $V_{GS} = 10$ V	28	6.8 nC
	0.015 at $V_{GS} = 4.5$ V	25	

FEATURES

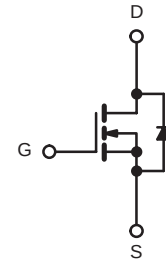
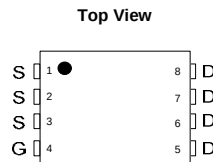
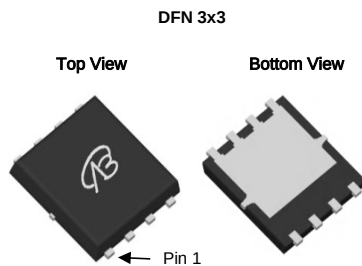
- Trench Gen IV power MOSFET
- Tuned for the lowest $R_{DS} - Q_{oss}$ FOM
- 100 % R_g and UIS tested
- Q_{gd} / Q_{gs} ratio < 1 optimizes switching characteristics



RoHS
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HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- Motor drive switch
- Battery and load switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	30	A
	$T_C = 70^\circ\text{C}$		25.3	
	$T_A = 25^\circ\text{C}$		11.4 ^{a, b}	
	$T_A = 70^\circ\text{C}$		9.2 ^{a, b}	
Pulsed Drain Current ($t = 100 \mu\text{s}$)		I_{DM}	70	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	I_S	19	
	$T_A = 25^\circ\text{C}$		2.2 ^{a, b}	
Single Pulse Avalanche Current	$L = 0.1 \text{ mH}$	I_{AS}	11	mJ
Single Pulse Avalanche Energy		E_{AS}	6	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	23	W
	$T_C = 70^\circ\text{C}$		14.8	
	$T_A = 25^\circ\text{C}$		2.6 ^{a, b}	
	$T_A = 70^\circ\text{C}$		1.7 ^{a, b}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering Recommendations (Peak temperature) ^{c, d}			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, e}	$t \leq 10 \text{ s}$	R_{thJA}	38	48	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady state	R_{thJC}	4.3	5.4	

Notes

- Surface mounted on 1" x 1" FR4 board.
- $t = 10 \text{ s}$.
- The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 94°C/W .
- Based on $T_C = 25^\circ\text{C}$.

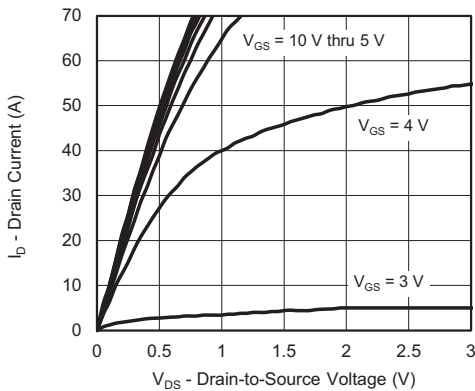
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	22.1	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-5.1	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0	-	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 V / -16 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	-	0.013	-	Ω
		V _{GS} = 4.5 V, I _D = 5 A	-	0.015	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5 A	-	52	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	1800	-	pF
Output Capacitance	C _{oss}		-	155	-	
Reverse Transfer Capacitance	C _{rss}		-	20	-	
C _{rss} /C _{iss} Ratio			-	0.018	0.036	
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 5 A	-	14.2	22	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 5 A	-	6.8	11	
Gate-Source Charge	Q _{gs}		-	3	-	
Gate-Drain Charge	Q _{gd}		-	1.5	-	
Output Charge	Q _{oss}	V _{DS} = 20 V, V _{GS} = 0 V	-	6.5	-	
Gate Resistance	R _g	f = 1 MHz	0.4	2	4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	16	30	ns
Rise Time	t _r		-	56	110	
Turn-Off Delay Time	t _{d(off)}		-	13	25	
Fall Time	t _f		-	27	55	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	-	7	15	
Rise Time	t _r		-	22	45	
Turn-Off Delay Time	t _{d(off)}		-	13	25	
Fall Time	t _f		-	8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	19	A
Pulse Diode Forward Current	I _{SM}		-	-	30	
Body Diode Voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	-	20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	10	20	nC
Reverse Recovery Fall Time	t _a		-	10.5	-	ns
Reverse Recovery Rise Time	t _b		-	9.5	-	

Notes

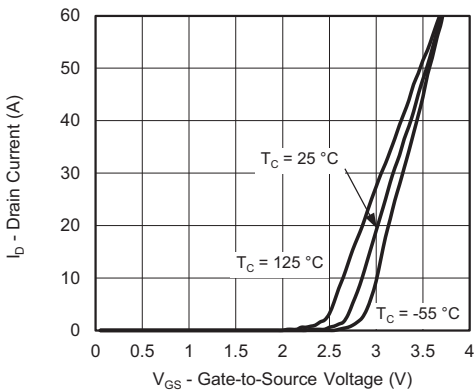
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

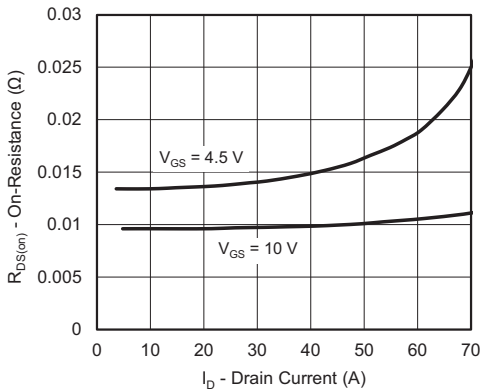
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



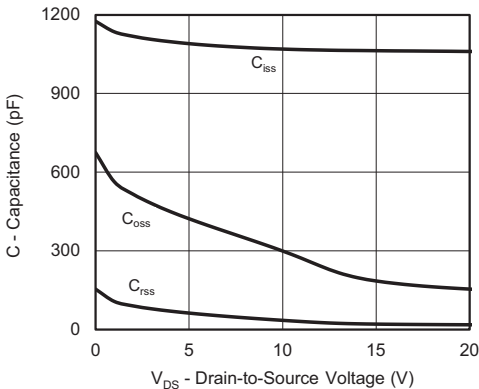
Output Characteristics



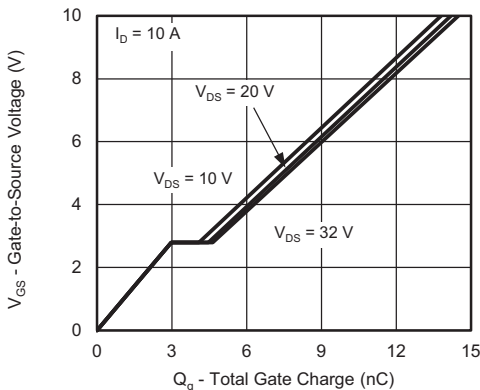
Transfer Characteristics



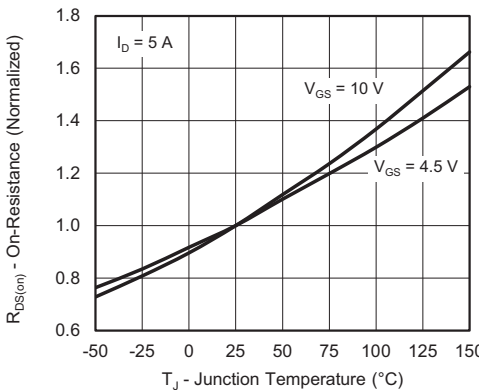
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

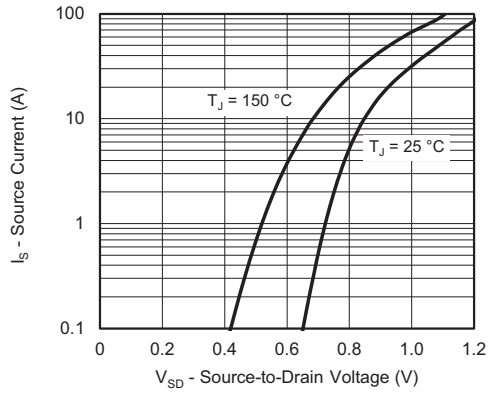


Gate Charge

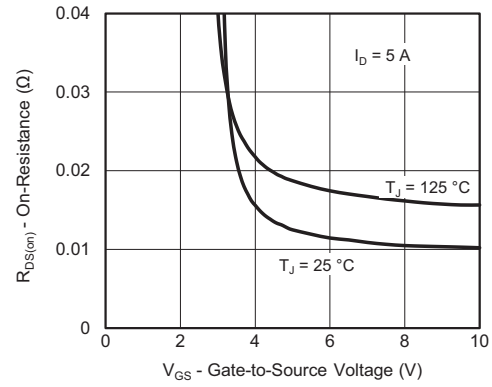


On-Resistance vs. Junction Temperature

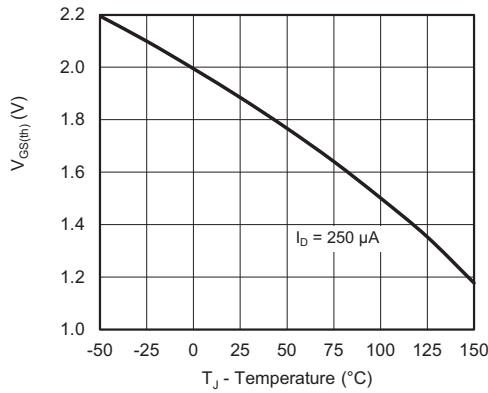
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



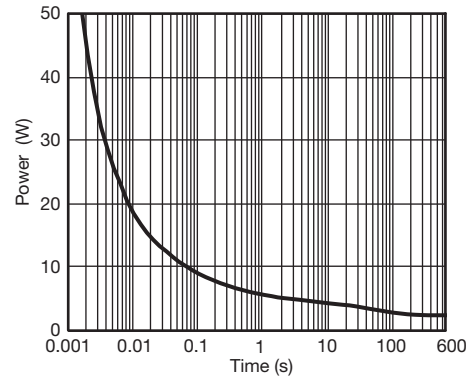
Source-Drain Diode Forward Voltage



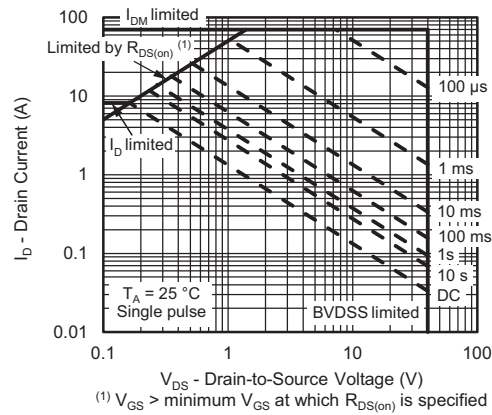
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

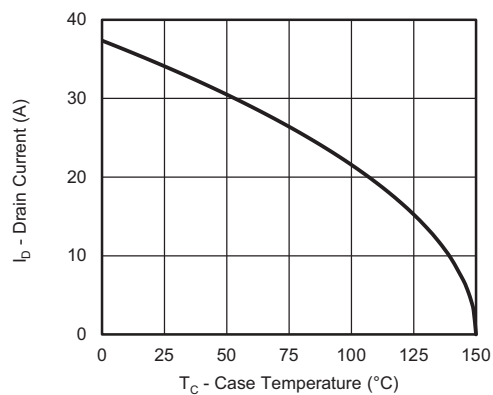


Single Pulse Power, Junction-to-Ambient

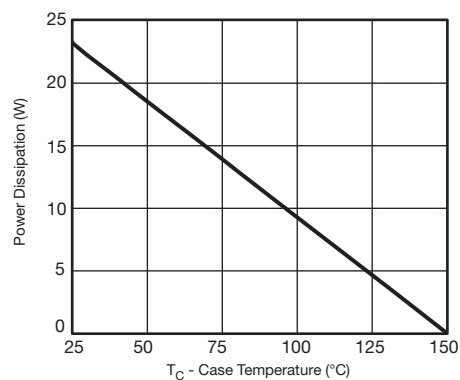


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a

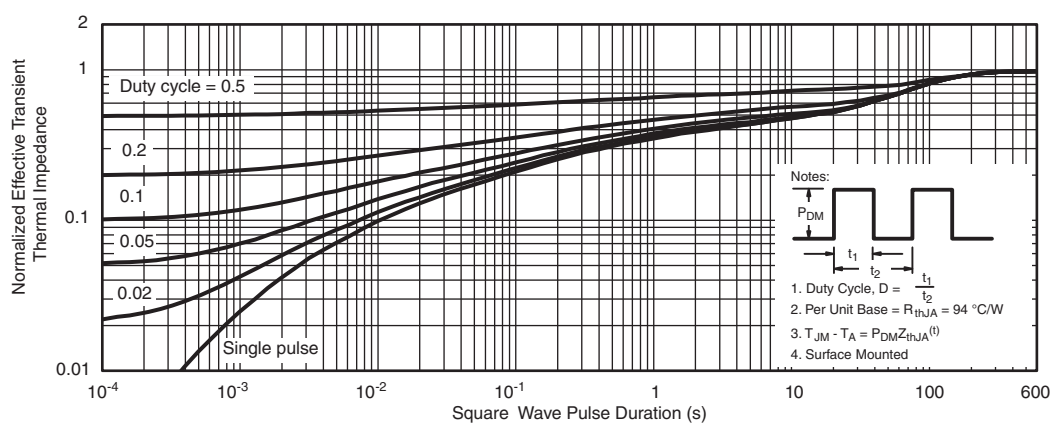


Power Derating

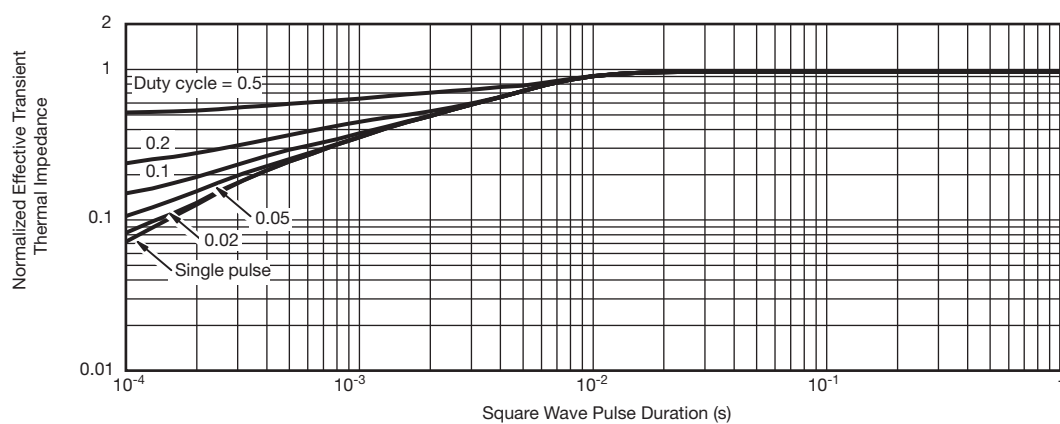
Note

- a. The power dissipation P_D is based on $T_J (\text{max.}) = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

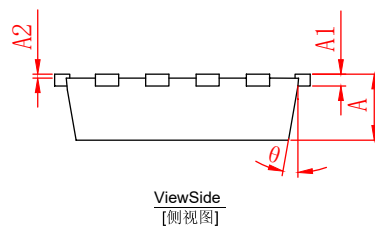
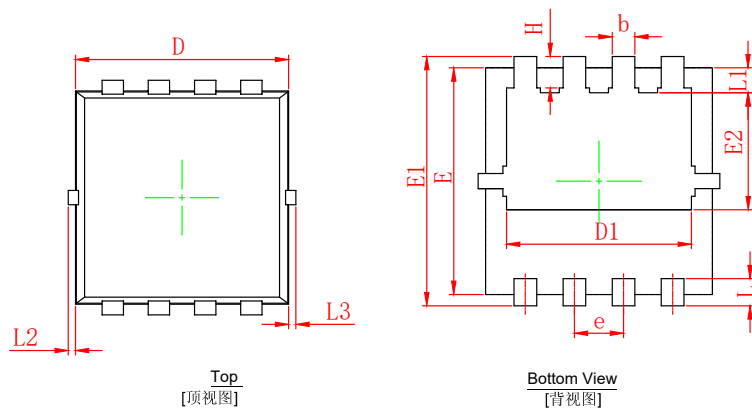


Normalized Thermal Transient Impedance, Junction-to-Ambient



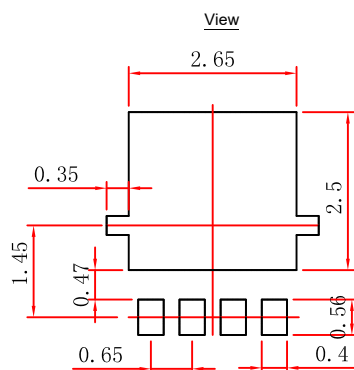
Normalized Thermal Transient Impedance, Junction-to-Case

PDFNWB3×3-8L Package Outline Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.650	0.850	0.026	0.033
A1	0.203REF.		0.008REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.050	2.550	0.081	0.100
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.450	1.650	0.057	0.065
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
Φ	9°	13°	9°	13°

Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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