Dual Channel PWM Controller with I²C Interface Control for IMVP9.1 CPU Core Power Supply

General Description

The RT3628AE is a synchronous buck controller which supports 2 output rails and can fully meet Intel IMVP9.1 requirements. The RT3628AE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3628AE features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3628AE integrates a high accuracy ADC for platform and function settings, such as ICCMAX, switching frequency, over-current threshold and AQR trigger level. The RT3628AE provides VR Ready and thermal indicators. It also features complete fault protection functions, including over-voltage (OV), under-voltage (UV), over-current (OC) and under-voltage lockout (UVLO). The RT3628AE supports several functions which can be set by I²C interface, like thermal balance adjustment, dynamic load line, voltage offset setting, fix VID setting, protection report, protection disable and Current/PSYS/Temperature report.

Applications

- IMVP9.1 Intel Core/AXG Supply
- Desktop and Notebook Computer
- AVP Step-Down Converter

Features

- **Intel IMVP9.1 Compliant**
- **8/7/6/5/4 Phase (CORE VR) + 1 Phase (AXG VR) PWM Controller**
- **G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming and Reporting**
- **Accurate Current Balance**
- **Diode Emulation Mode at Light Load Condition**
- **Fast Transient Response : Adaptive Quick Response (AQR)**
- **VR Ready Indicator**
- **OVP, OCP, UVP with Flag**
- **Switching Frequency Setting**
- **Slew Rate Setting**
- **DVID Enhancement**
- **Acoustic Noise Suppression**
- **Zero Load-line**
- **Rail Disable**
- **Standard I²C Protocol Interface**
  - **Thermal Balance Adjustment**
  - **Dynamic Load Line Setting**
  - **Voltage Offset Setting**
  - **Fixed VID Setting**
  - **Protection Report and Protection Disable**
  - **Current/PSYS/Temperature Report**
- **Soldering Good Detection**
- **Small 60-Lead WQFN Package**

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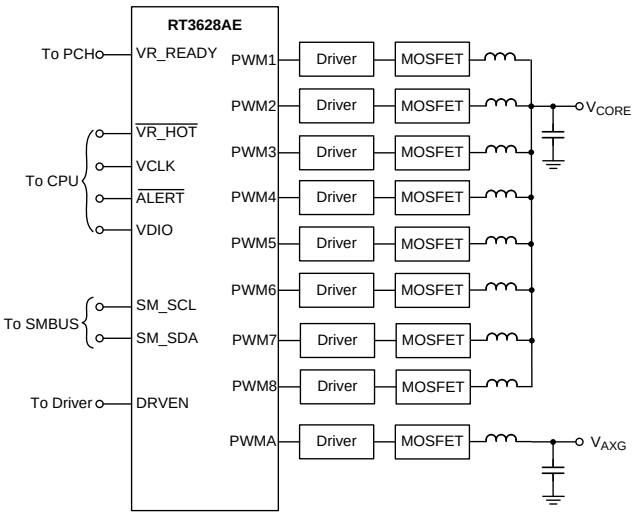
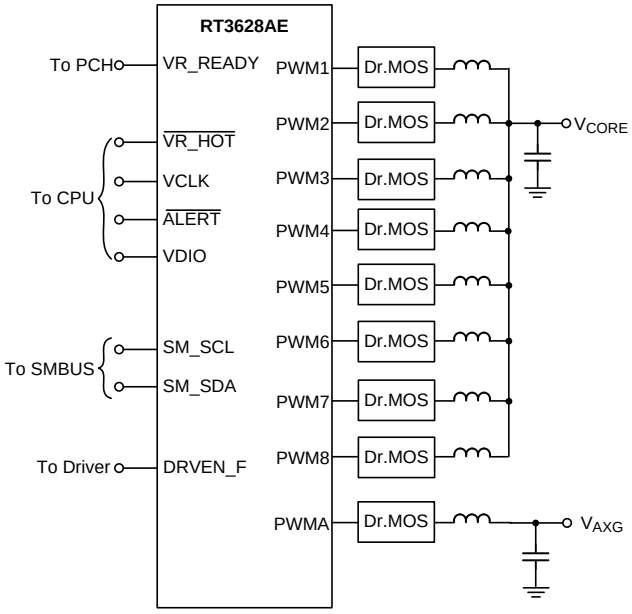
Simplified Application Circuit





Ordering Information

RT3628AE □□

- Package Type
  QW : WQFN-60L 7x7 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

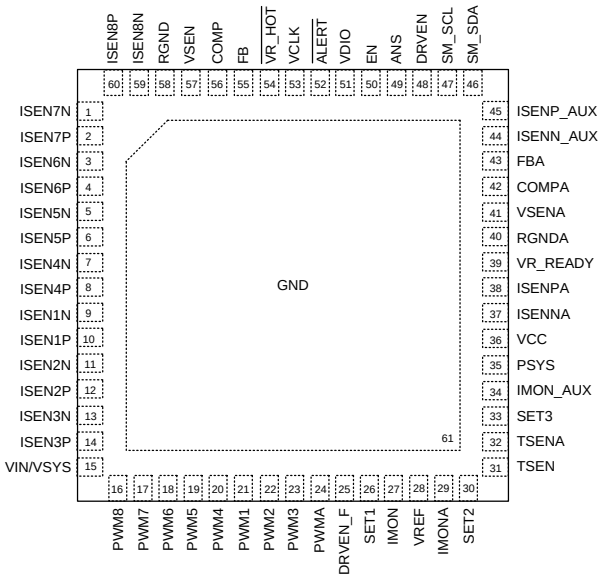
- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT3628AEGQW : Product Number
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



WQFN-60L 7x7

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Functional Pin Description

Pin No.	Pin Name	Pin Function
9, 11, 13, 7, 5, 3, 1, 59	ISEN[1:8]N	Negative inputs of current-sense amplifier of multi-phase CORE rail VR channel 1, 2, 3, 4, 5, 6, 7 and 8.
10, 12, 14, 8, 6, 4, 2, 60	ISEN[1:8]P	Positive inputs of current-sense amplifier of multi-phase CORE rail VR channel 1, 2, 3, 4, 5, 6, 7 and 8.
15	VIN/VSYS	Input voltage pin. Connect a low pass filter which time constant is at the switching frequency to this pin for setting on-time.
21, 22, 23, 20, 19, 18, 17, 16	PWM[1:8]	PWM output for CORE rail VR channel 1, 2, 3, 4, 5, 6, 7 and 8. The tri-state window = 1.6V to 2.2V.
24	PWMA	PWM output for AXG rail VR. The tri-state window = 1.6V to 2.2V.
25	DRVEN_F	External driver mode control and the output high level is VCC. As received PS4 command, this pin is in floating state. For discrete power MOSFET driver application, connecting 100kΩ resister to GND is required.
26	SET1	Function setting for DVID slew rate, I^2C address, CORE rail on-time (switch frequency), $\overline{VR\_HOT}$ assertion during DVID current limiting, and AUX rail ICCMAX. Connect the SET1 to 5V and turn on the EN pin, if the soldering is good, both rails outputs are VBOOT.
27	IMON	CORE rail VR current monitor output for controller. This pin outputs a current proportional to the output current.
28	VREF	Voltage source output. During Controller internal setting period, it outputs 3.2V. In normal operation, it outputs 0.6V to offset IMON, IMONA and IMON_AUX signal. While controller shuts down or sets all rail in PS4, voltage source shuts down. An exact 0.47μF capacitor and 3.9Ω resistor from this pin to GND are required for stability.
29	IMONA	AXG rail VR current monitor output for controller. This pin outputs a current proportional to the output current.
30	SET2	Function setting for CORE rail adaptive ramp trigger level, ICCMAX of AXG rail, dual phases function and AXG rail on-time (switch frequency).
31	TSEN	Thermal sense input for CORE rail. Function setting for CORE rail ZCD threshold, CORE and AXG rail current gain (Ai).
32	TSENA	Thermal sense input for AXG rail. Function setting for CORE and AXG rail sum-OC threshold, AXG rail ZCD threshold and CORE rail adaptive quick response threshold.
33	SET3	Function setting for CORE and AXG rail DAC step, CORE rail ICCMAX, CORE and AXG rail VBOOT (boot voltage depends on SET3 VID table setting), and AXG rail adaptive ramp trigger level.
34	IMON_AUX	AUX rail VR current monitor output for controller. This pin outputs a current proportional to the output current.
35	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. The input power domain (SVID Address 0x0Dh) rail can be disabled by pulling the voltage at the PSYS pin > (VCC – 0.5V). RT3628AE will reject any commands to the input power domain rail. If the platform doesn't support PSYS function, It is recommended to connect PSYS pin to GND to avoid affecting system performance.
36	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, R = 1Ω and C = 2.2μF. The decoupling capacitor should be placed as close to PWM controller as possible. The R is recommended as 0603 size.

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Pin No.	Pin Name	Pin Function
37	ISENNA	Negative inputs of current-sense amplifier of AXG rail VR.
38	ISENPA	Positive inputs of current-sense amplifier of AXG rail VR.
39	VR_READY	VR ready indicator.
40	RGNDA	Return ground for AXG rail VR. This pin is the negative node of the differential remote sense.
41	VSENA	AXG rail VR voltage sense input. This pin is connected to the terminal of AXG rail VR output voltage.
42	COMPA	AXG rail VR error amplifier output pin.
43	FBA	Negative input of the error amplifier. This pin is for AXG rail VR output voltage feedback to controller.
44	ISENN_AUX	Negative inputs of current-sense amplifier of AUX rail VR.
45	ISENP_AUX	Positive inputs of current-sense amplifier of AUX rail VR.
46	SM_SDA	Data line for the I^2C interface.
47	SM_SCL	Clock input for the I^2C interface.
48	DRVEN	External driver mode control and the output high level is VCC. As the PS4 command is received, this pin is in low state.
49	ANS	Acoustic noise suppression function setting. When pulling to VCC, this function can be enabled. This pin is not allowed to be floating.
50	EN	Controller enable pin. A logic high signal enables the controller. Don't drive this pin voltage higher than V_{CC} – 1.2V at any time.
51	VDIO	VR and CPU data transmission interface.
52	$\overline{\text{ALERT}}$	SVID alert. (Active low)
53	VCLK	Synchronous clock from the CPU.
54	$\overline{\text{VR\_HOT}}$	Thermal monitor output. (Active low).
55	FB	Negative input of the error amplifier. This pin is for CORE rail VR output voltage feedback to controller.
56	COMP	CORE rail VR error amplifier output pin.
57	VSEN	CORE rail VR voltage sense input. This pin is connected to the terminal of CORE rail VR output voltage.
58	RGND	Return ground for CORE rail VR. This pin is the negative node of the differential remote sense.
61 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough VIA numbers for maximum power dissipation.

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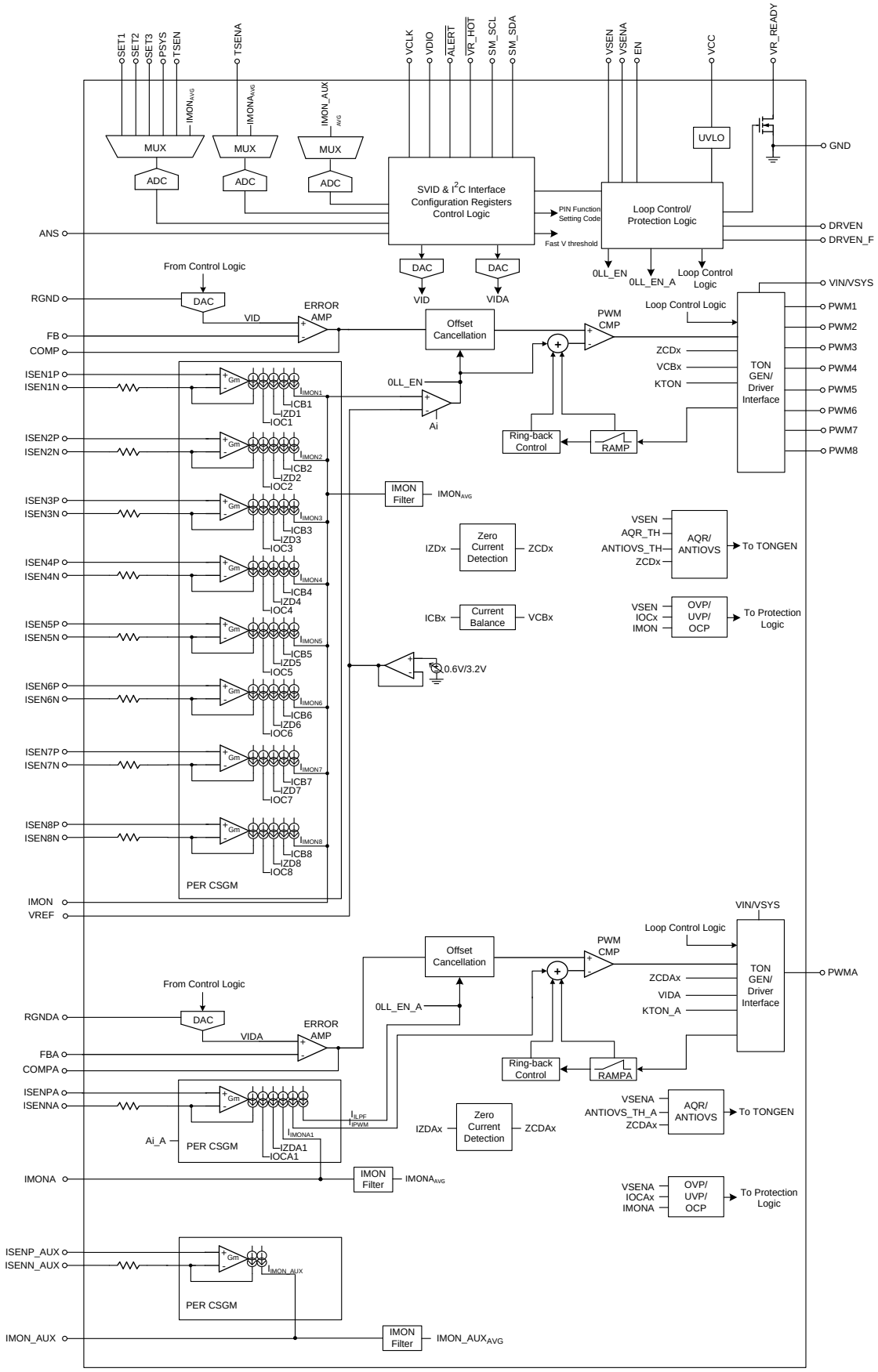
Functional Block Diagram



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Operation

G-NAVP™ Control Mode

The RT3628AE adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3628AE generates a PWM pulse to achieve loop modulation. The left part of Figure 1 shows the basic G-NAVP™ behavior waveforms. The COMP signal is the sensed voltage, that is inverted and amplified signal of output voltage. While current loading is increasing, referring to the right part of Figure 1, the CCOMP rises due to output voltage droop. Then, the rising COMP forces PWM to turn-on earlier and closer. While inductor current reaches loading current, the COMP enters another steady state of higher voltage and the corresponding output voltage is in the steady state of lower voltage. The loadline, voltage drooping which is proportional to loading current, is achieved.

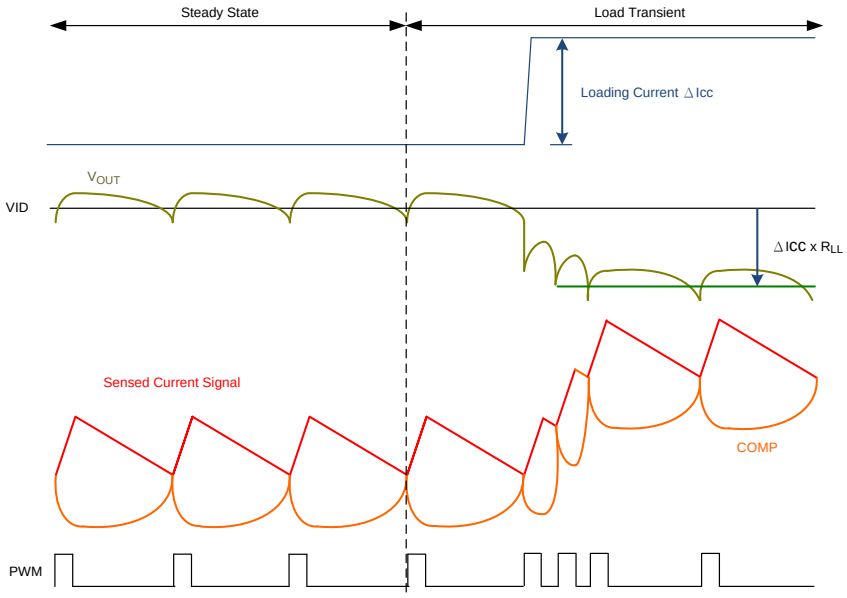

Figure 1. G-NAVP™ Behavior Waveform

I²C and SVID Interface/Control Logic/Configuration Registers

The SVID Interface receives or transmits SVID signal with CPU. The I²C Interface receives or transmits I²C signal with SMBus. The control logic executes command (Read/Write registers, SetVID, SetPS) and sends related signals to control VR. The configuration registers include function setting registers and CPU required registers.

IMON Filter

The IMON Filter is used to average current signal by analog low-pass filter. It outputs $IMON_{AVG}$, $IMONA_{AVG}$ and $IMON\_AUX_{AVG}$ to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs for SET1, SET2, SET3, TSEN, TSENA , PSYS, $IMON_{AVG}$, $IMONA_{AVG}$ and $IMON\_AUX_{AVG}$. The ADC converts these analog signals to digital codes for reporting or function settings.

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UVLO

The UVLO Detects the VCC voltage. As VCC exceeds the threshold, the controller issues POR = high and waits EN. After both POR and for EN are ready, the controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to SetVID command, Control Logic dynamically changes VID voltage to the target voltage with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM triggers.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and over-current protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by PIN-SETTING(Ai/Ai_A). It helps wide application range of DCR and load-line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal and sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation cancels the current signal/comp voltage ripple issue to control output voltage accuracy.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

Zero Current Detection

The Zero Current Detection detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (anti-overshoot function).

AQR/ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWMs to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by PIN-SETTING. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWMs in tri-state until the zero current is detected.

TONGEN/Driver Interface

The PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWMs to turn on at the same time. Driver interface provides high/low/tri-state to drive external driver. In power saving mode, driver interface force PWM in tri-state to turn off high-side and low-side power MOSFETs according to zero current detection output. In addition, the PWM state is controlled by protection logic. Different protections force required PWM state.

OVP/UVP/OCP

Over-voltage protection / under-voltage protection / over-current protection.

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Absolute Maximum Ratings (Note 1)

- VIN/VSYS to GND ---------- –0.3V to 28V
- VCC to GND ---------- –0.3V to 6.5V
- RGND to GND ---------- –0.3V to 0.3V
- Other Pins ---------- –0.3V to 6.8V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-60L 7x7 ---------- 3.92W
- Package Thermal Resistance (Note 2)

  WQFN-60L 7x7, θ_{JA} ---------- 25.5°C/W

  WQFN-60L 7x7, θ_{JC} ---------- 6.5°C/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature---------- 150°C
- Storage Temperature Range---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VIN/VSYS to GND ---------- 4.5V to 24V
- Supply Input Voltage, VCC ---------- 4.75V to 5.25V
- Junction Temperature Range ---------- –10°C to 105°C

Electrical Characteristics

(VCC = 5V, typical values are referenced to T_J = 25°C, Min and Max values are referenced to T_J from –10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Controller Supply Current	I_{VCC}	VCC = 5V, EN = H, no switching	--	13	--	mA
Controller Supply Current under PS4 all call	I_{VCC_PS4}	VCC = 5V, EN = H, PS4 all call	--	85	--	μA
VR Shutdown Current	I_{SHDN}	VCC = 5V, EN = L	--	--	15	μA
Per Phase Current Sense Amplifier						
Recommended Input Voltage Range for High Accuracy	V_{IN_PCS}	Recommend Input Voltage Range for High Accuracy	–10	--	80	mV
Current Sense Gain	GAIN_PCS		0.97	1	1.03	V/V
Current Sense Resistor	R_{INT}		--	1	--	kΩ
TON Setting						
ON-Time Setting	T_{ON}	VIN = 12V, VID = 1.8V, freq. = 350kHz	--	428	--	ns

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Protections							
VCC POR		V_{POR}		--	--	4.45	V
VCC Under-Voltage Lockout (UVLO)		V_{UVLO}		--	--	4.3	V
Over-Voltage Production Threshold		V_{ROVP}	Respect to VID voltage VID > 1V	VID + 300	VID + 350	VID + 400	mV
		V_{AOVP}	VID ≤ 1V	1.325	1.35	1.375	V
Pre-Over Voltage Protection Threshold (PRE-OVP)	for DAC = VID1	$V_{PRE-OVP}$	Active while VRON recycle or PS4 exit and until PWM turn-on	2.42	2.45	2.48	V
	for DAC = VID2			2.62	2.65	2.68	V
Debounce Time of all OVP		DT_{OVP}		--	0.5	--	µs
Under Voltage Protection Threshold (UVP)		V_{UVP}	Active while VID settle and non-DACOFF	–700	–650	–600	mV
Debounce Time of UVP		DT_{UVP}		--	3	--	µs
EN and VR_READY							
VR Enable Threshold		V_{IH_EN}		0.7	--	--	V
VR Disable Threshold		V_{IL_EN}		--	--	0.3	V
Leakage Current of EN		I_{LEAK_EN}		–1	--	1	µA
Output Voltage Low of VR_READY		$V_{OL\_VR\_READY}$	I_{VR_READY} = 10mA	--	--	0.13	V
Acoustic Noise Suppression (ANS)							
ANS Enable Threshold		$V_{TH\_H\_ANS}$	VCC-V_{ANS} < 0.5V, ANS is enabled	--	--	0.5	V
ANS Disable Threshold		$V_{TH\_L\_ANS}$	VCC-V_{ANS} > 1V, ANS is disabled	1	--	--	V
Serial VID and $\overline{VR\_HOT}$							
SVID VCLK / VDIO Logic High Threshold		V_{IH_SVID}		0.65	--	--	V
SVID VCLK / VDIO Logic Low Threshold		VI_{L_SVID}		--	--	0.45	V
Leakage Current of VCLK / VDIO / $\overline{ALERT}$ / $\overline{VR\_HOT}$		I_{LEAK_SVID}	VDIO = H, $\overline{ALERT}$ = H, $\overline{VR\_HOT}$ = H	–1	--	1	µA
Output Voltage Low of VDIO / $\overline{ALERT}$ / $\overline{VR\_HOT}$		V_{OL_VDIO}	I_{VDIO} = 10mA	0.04	--	0.13	V
		V_{OL_ALERT}	$I_{\overline{ALERT}}$ = 10mA				
		V_{OL_VRHOT}	$I_{\overline{VR\_HOT}}$ = 10mA				
I^2C Interface							
SM_SCL / SM_SDA Logic High Threshold		V_{IH_I2C}		1	--	--	V
SM_SCL / SM_SDA Logic Low Threshold		V_{IL_I2C}		--	--	0.6	V
Leakage Current of SM_SCL / SM_SDA		I_{LEAK_I2C}	SM_SDA = H	–1	--	1	µA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Active Low Voltage of SM_SDA	V_{SM_SDA}	I_{SM_SDA} = 10mA	0.04	--	0.13	V
SCL Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	$t_{HD;STA}$		0.6	--	--	µs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	µs
Data Set-Up Time	$t_{SU;DAT}$		100	--	--	µs
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	µs
Rising Time of both SDA and SCL Signals	t_R		20	--	300	µs
Falling Time of both SDA and SCL Signals	t_F		20	--	300	µs
DIMON						
Digital IMON Set	$d_{VIMON\ ICCMAX}$	VIMON – VREF = 0.4V ; VREF = 0.6V	--	255	--	Decimal
	$d_{VIMONA\ ICCMAX}$	VIMONA – VREF = 0.4V ; VREF = 0.6V	--	255	--	Decimal
	$d_{VIMON\_AUX\ ICCMAX}$	VIMON_AUX – VREF =1.6V ; VREF = 0.6V	--	255	--	Decimal
Thermal Monitor						
TSEN Voltage Threshold to Pull Low $\overline{VR\_HOT}$ (Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_L}$	Within the range, $\overline{VR\_HOT}$ = L. (R 1% variation is considered)	--	0.600	0.620	V
TSEN Voltage Threshold to Pull High $\overline{VR\_HOT}$ (De-Asserts $\overline{VR\_HOT}$)	$V_{TSEN\_\overline{VR\_HOT}\_H}$	Within the range, $\overline{VR\_HOT}$ = H (R 1% variation is considered)	0.608	0.628	0.649	V
TSEN Rises to Pull Low $\overline{ALERT}$	$V_{TSEN\_Status\_H}$	$\overline{ALERT}$ = L	0.608	0.628	0.649	V
TSEN Down to Pull Low $\overline{ALERT}$	$V_{TSEN\_Status\_L}$	$\overline{ALERT}$ = L	0.637	0.658	0.680	V
I_{TSEN}						
Current Source from TSEN	I_{TSEN}	V_{TSEN} = 1.6V	78.8	80	81.2	µA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PSYS						
Digital IMON Reporting Code for PMAX	D_{PSYS_PMAX}	V_{PSYS} = 1.6V	--	255	--	Decimal
VSYS						
VSYS Input Voltage	V_{SYS_TH}	As V_{IN} = 24V	--	255	--	Decimal
		As V_{IN} = 12V	--	128	--	
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}		--	30	--	Ω
PWM Sink Resistance	R_{PWM_SNK}		--	10	--	Ω
OSC						
Oscillator Frequency 20kHz			–5	--	5	%
V_{REF}						
VREF Voltage	V_{VREF}	Normal operation	0.59	0.6	0.61	V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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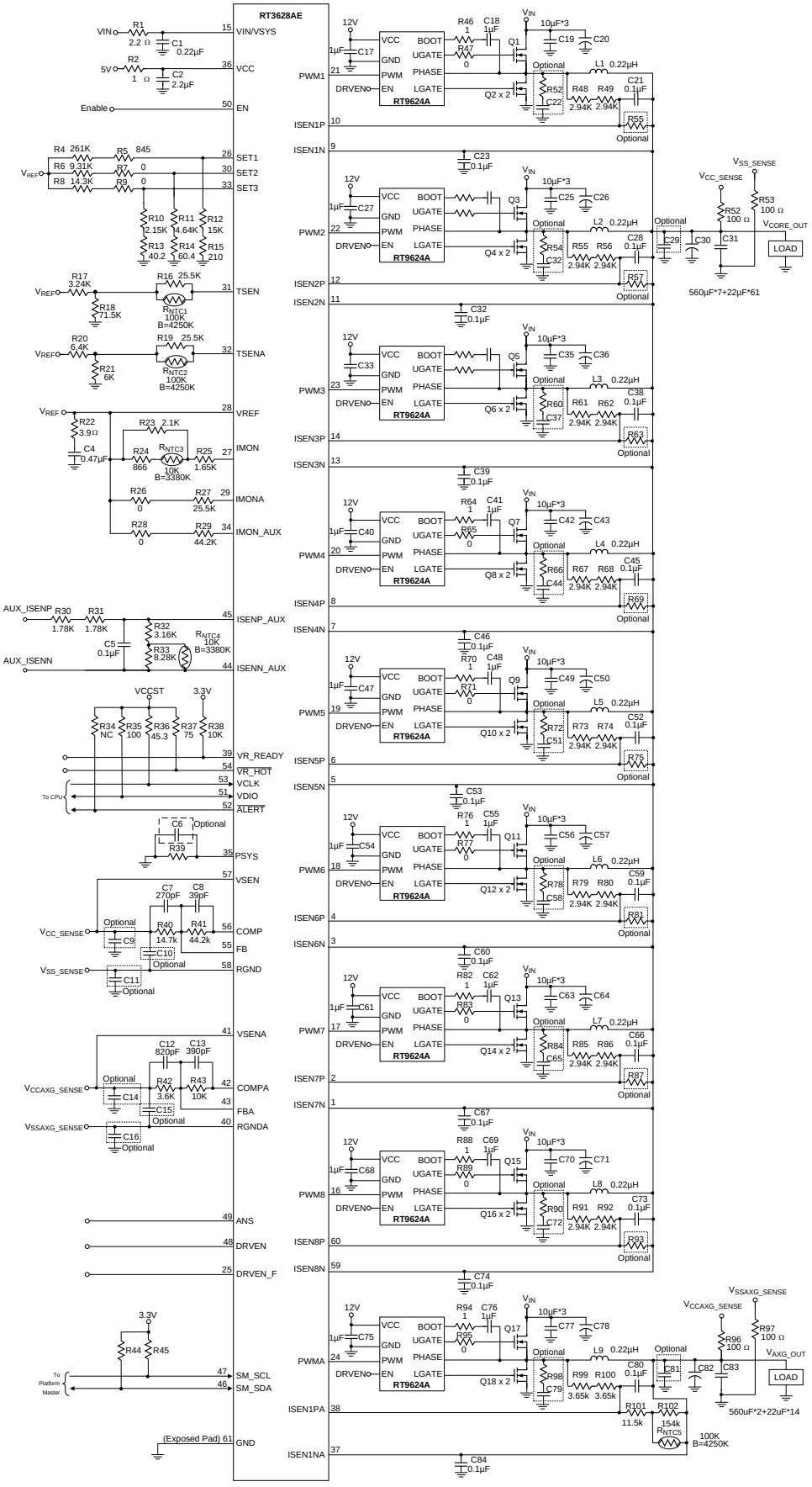
Typical Application Circuit



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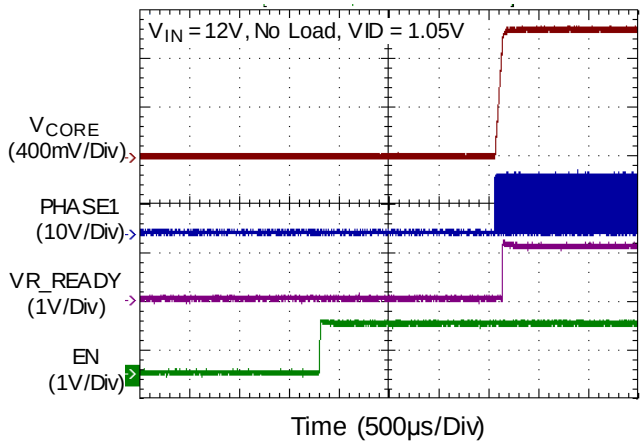
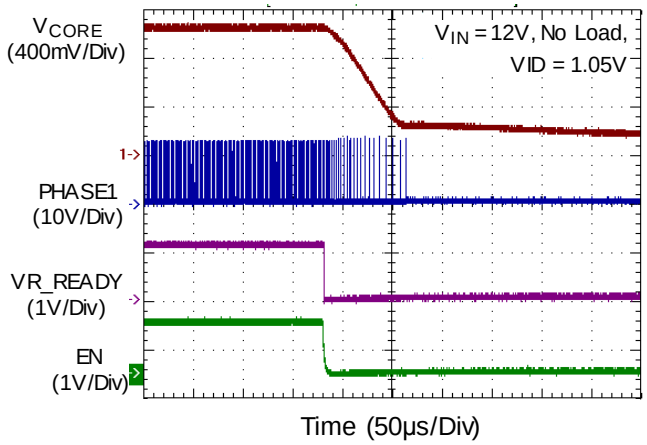
Typical Operating Characteristics

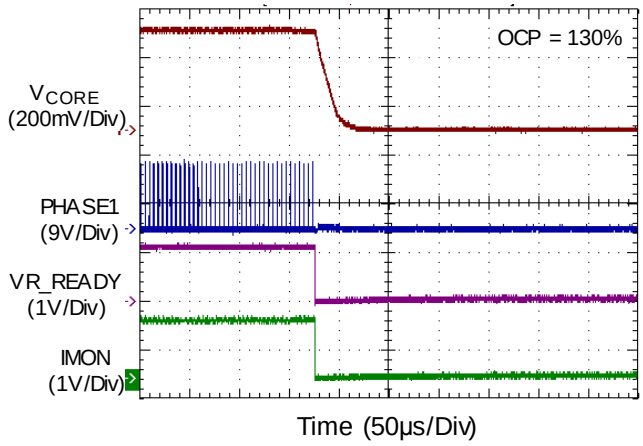
CORE VR Power On from EN



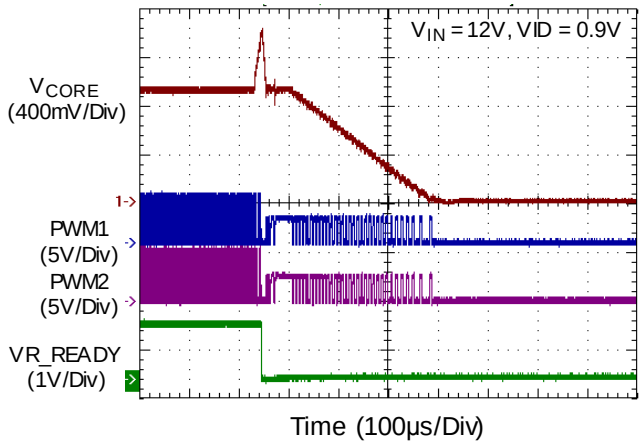
CORE VR Power Off from EN



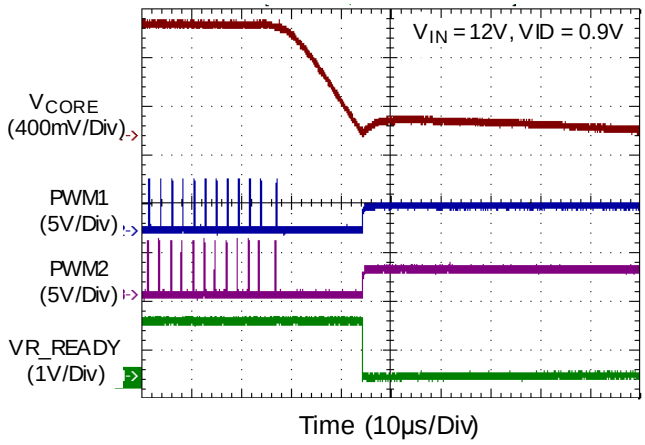
CORE VR OCP



CORE VR OVP



CORE VR UVP



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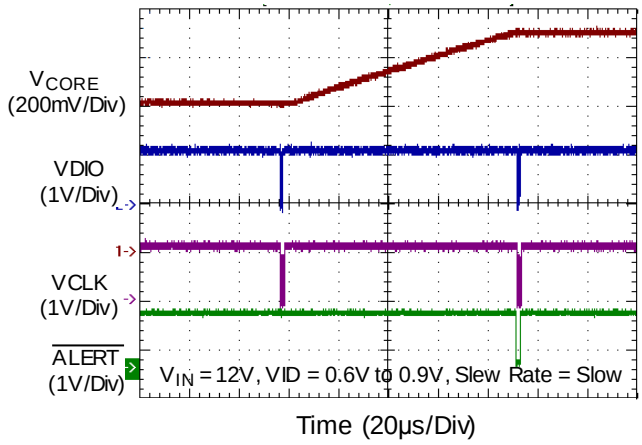

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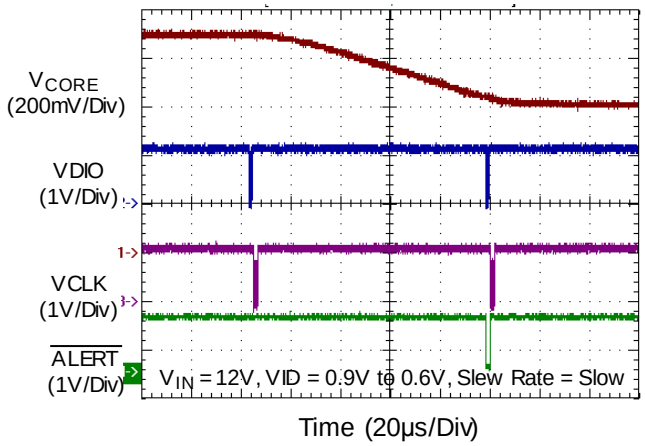
CORE VR Dynamic VID Down



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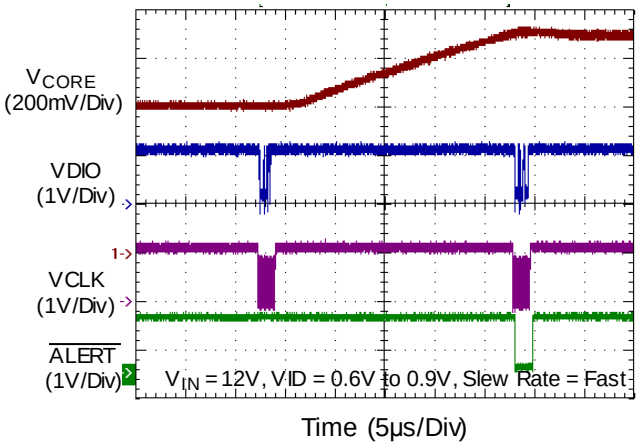

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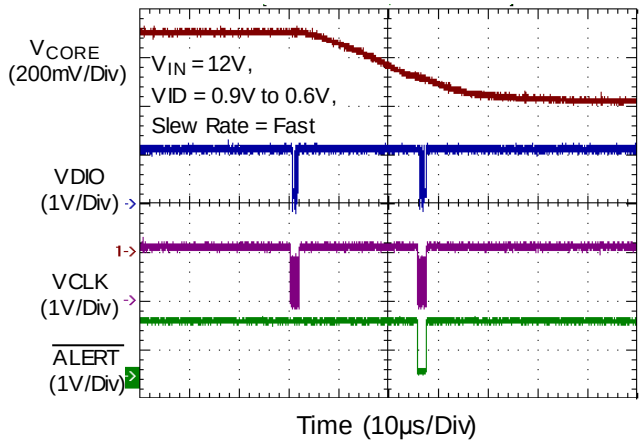

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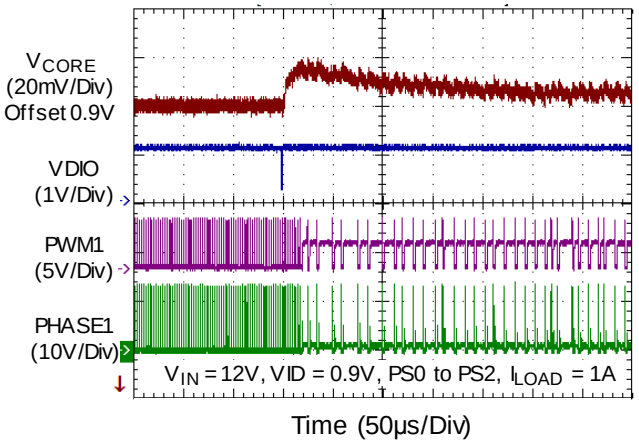

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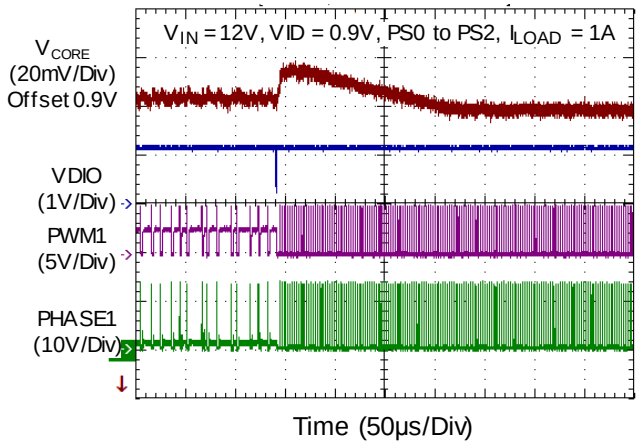
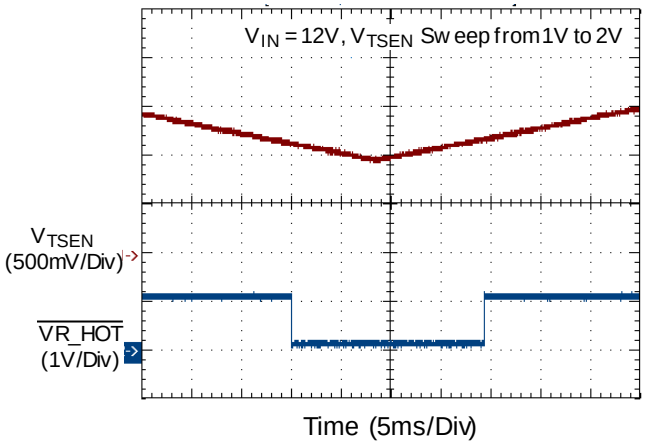


CORE VR Thermal Monitioring



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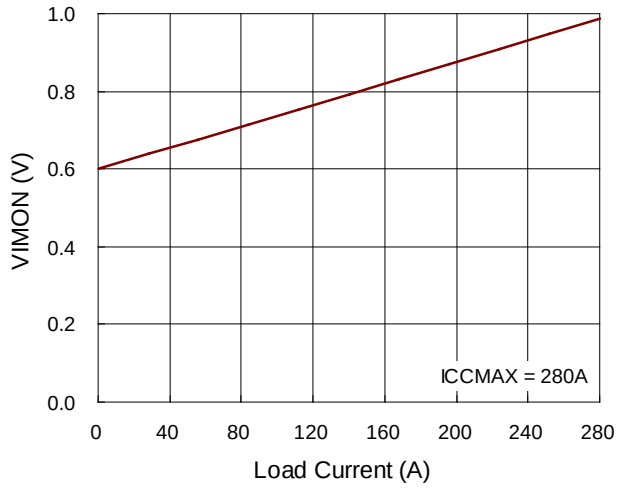
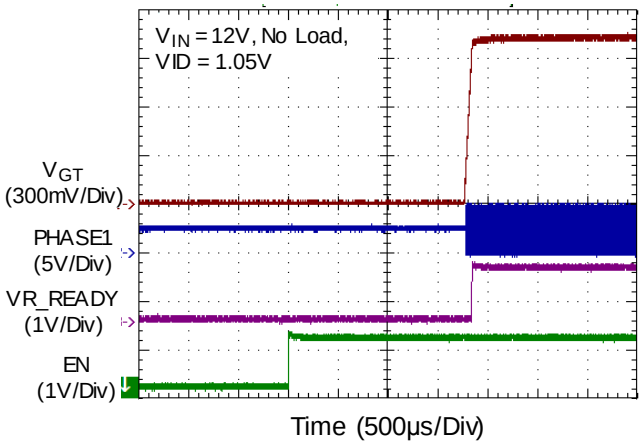
VIMON vs. Load Current



GT VR Power On from EN



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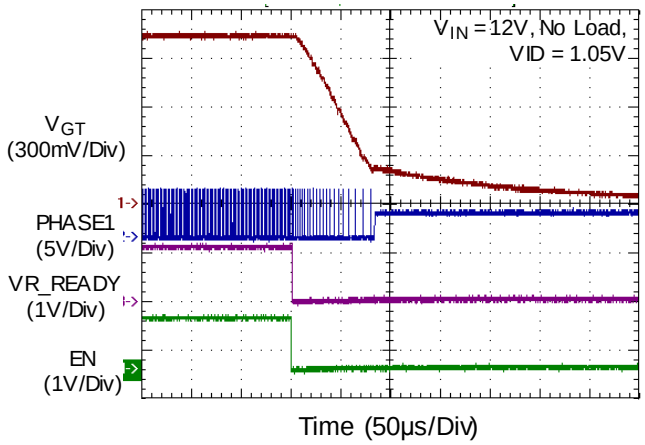

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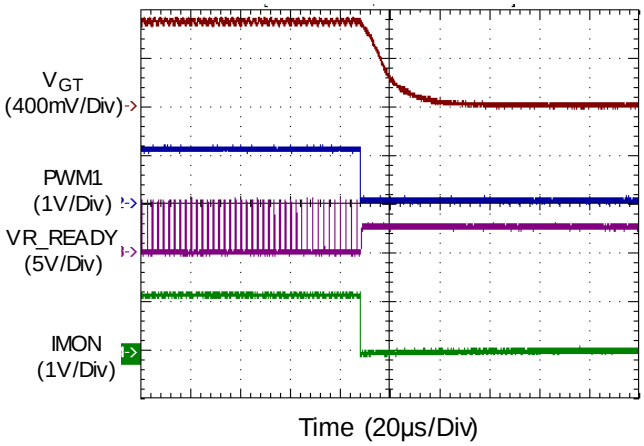

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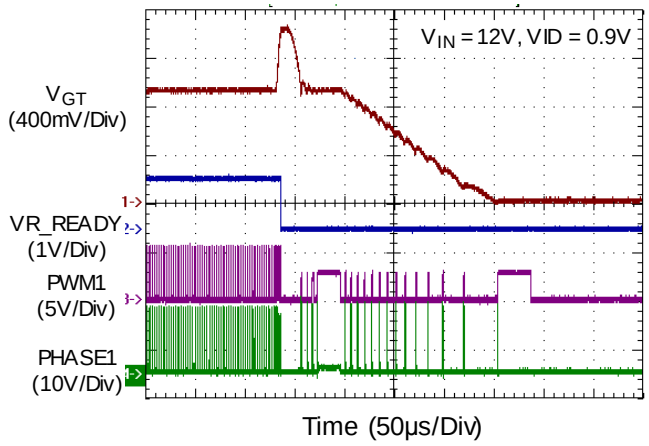

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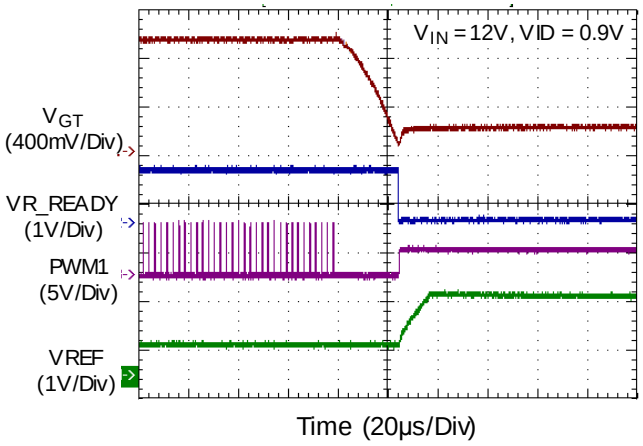

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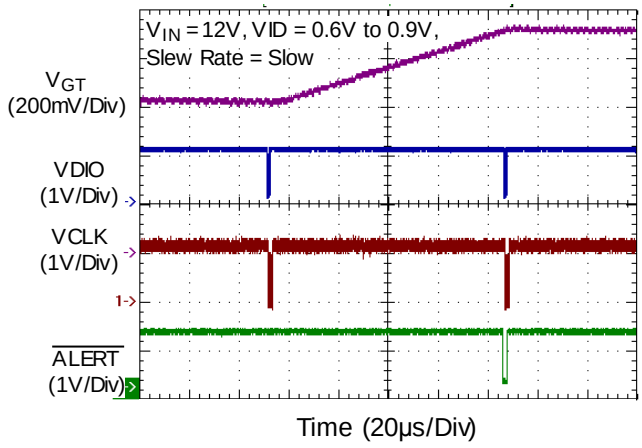
GT VR Dynamic VID Up



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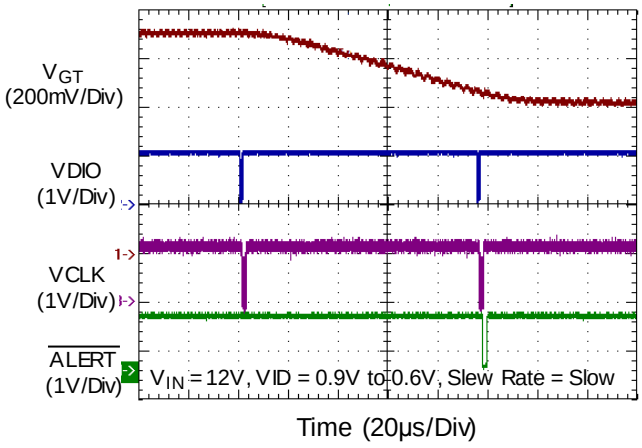

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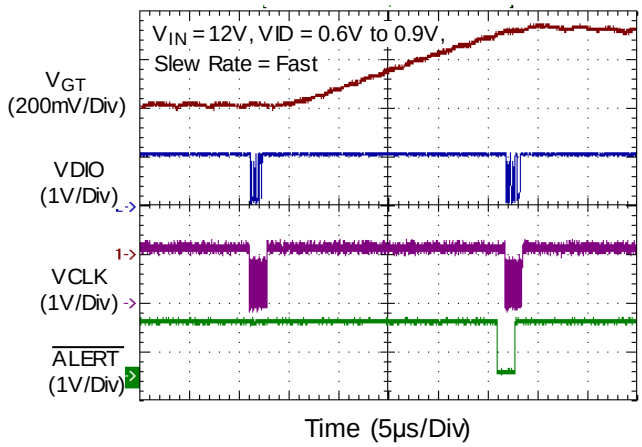

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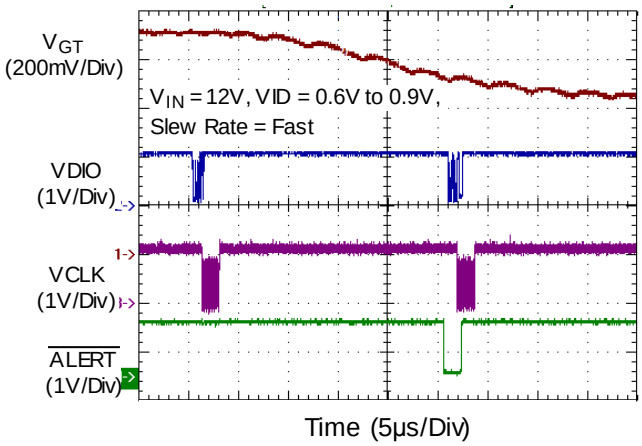
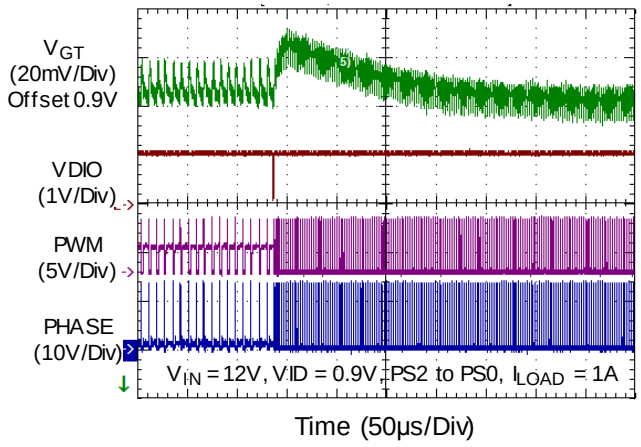


GT VR Mode Transient



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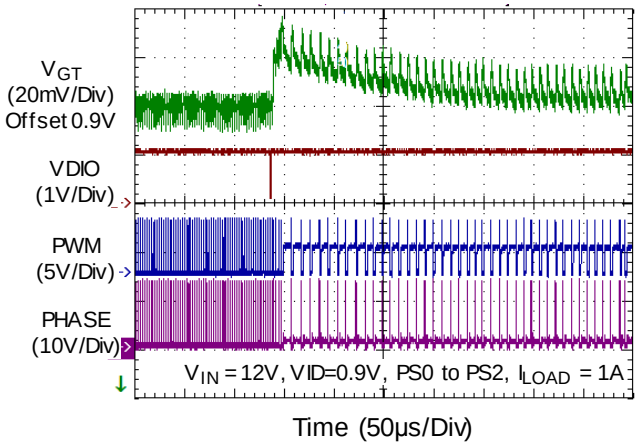

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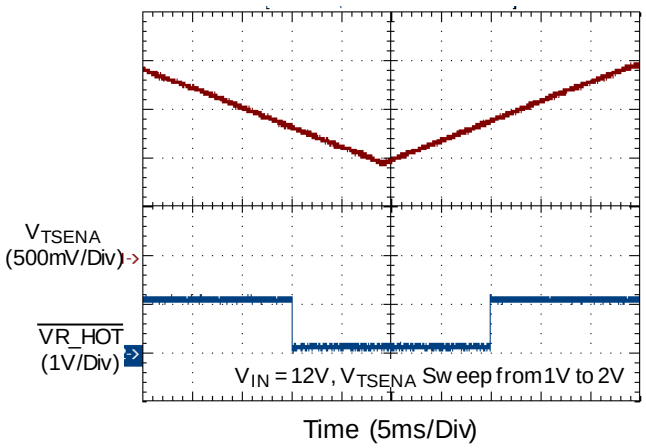
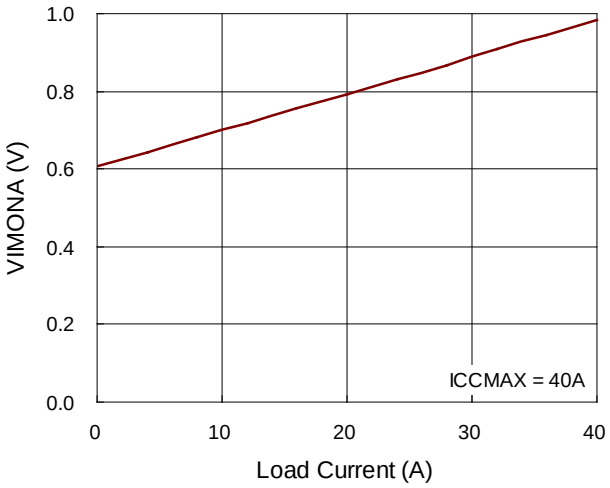
GT VR Thermal Monitoring



VIMONA vs. Load Current



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Application Information

The RT3628AE includes two voltage rails: an 8/7/6/5/4 phase synchronous buck controller, the CORE VR and a 1 phase synchronous buck controller, the AXG VR, designed to meet Intel IMVP9.1compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save total pin number for easy use and increasing PCB space utilization. The RT3628AE is used in desktop computers or notebook computers.

Power-ON Sequence

In order to confirm sufficient power supply for proper operation, the VR triggers UVLO if VCC voltage drops below 4.3V (max). The UVLO protection shuts down controller and forces high-side MOSFET and low-side MOSFET off. When VCC > 4.45, the RT3628AE issues POR=high and waits for EN signal. After POR = high and EN > 0.7V, the controller powers on (Chip Enable = H) and starts VR internal settings, which include internal circuit offset correction and function settings (PIN-SETTING). Users can set multi-functions through SETx, TSEN and TSENA pins. Figure 2 shows the typical timing of controller power-on. The pull-high power of EN pin is recommended as 1.05V, the same power as SVID interface. That can ensure the SVID power is ready while EN=H. Driver power (PVCC) is strongly suggested to be ready after VCC. This can prevent current flow back to VCC from PVCC through PWMx pin or DRVEN pin.

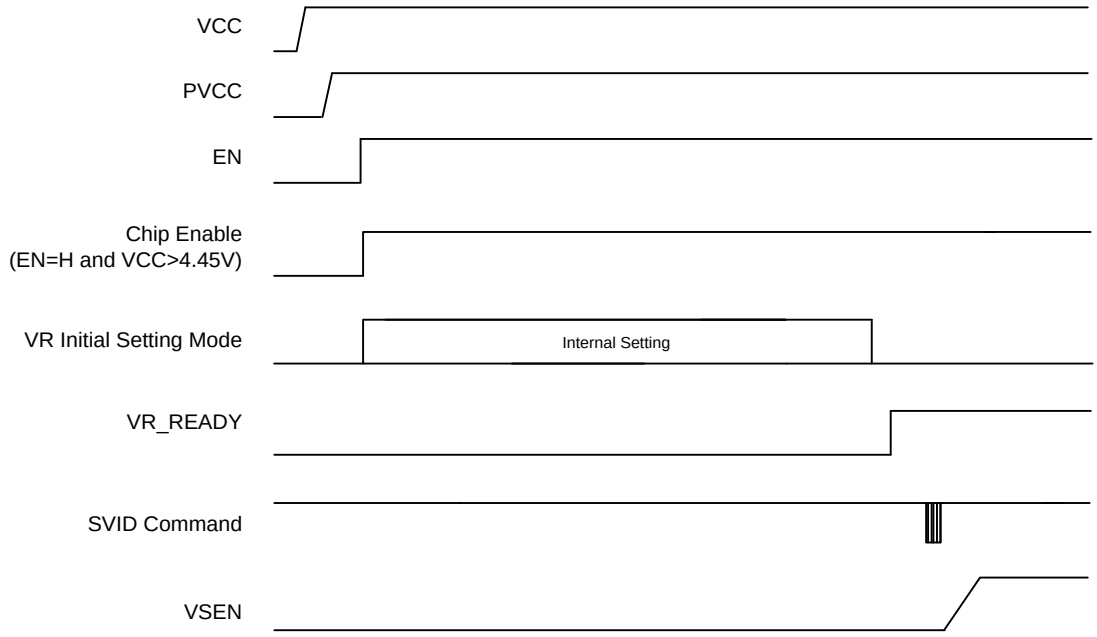

Figure 2. Typical Timing of Controller Power-ON

Maximum Active Phases Number Setting

The number of active phases is determined by the ISENxP voltages. The detection is only active and latched at Chip Enable rising edge (EN = H and VCC > 4.45V). While Voltage at ISENxP > (VCC – 0.5V), maximum active phase number is (x-1). For example, pulling ISEN8P to VCC programs a 7-phase operation, while pulling ISEN8P and ISEN7P to VCC programs a 6-phase operation. The unused ISENxN pins are recommended to connect to VCC and the unused PWM pins can be floating. Figure 3 is a 7-phase operation example, the pull-up voltage of ISEN8P/ISEN8N should be connected together with VCC of RT3628AE and the pull-up resistor should be 10kΩ.

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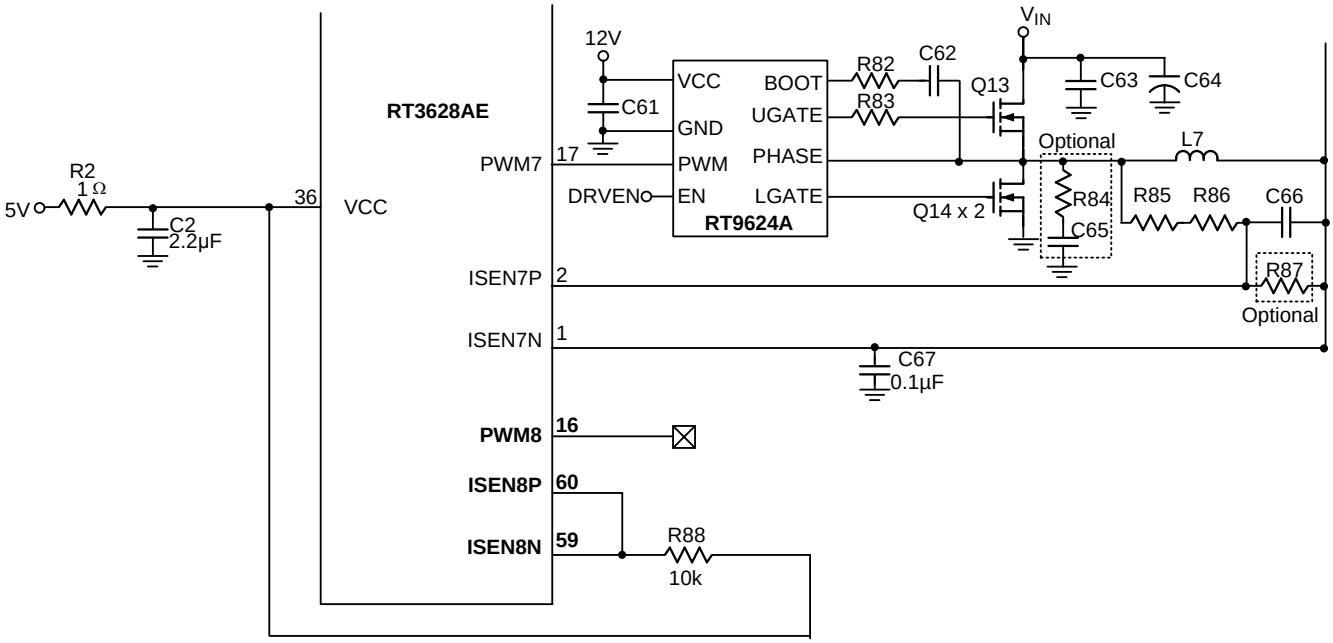

Figure 3. 7-Phase Operation Setting

Rail Disable

Pulling ISEN1P > (VCC – 0.5V) to programs CORE rail disabled. The unused ISENxN pins are recommended to connect to VCC and the unused PWM pins can be floating. Pulling ISENPA > (VCC – 0.5V) to programs AXG rail disabled. The unused ISENNA pins are recommended to connect to VCC and the unused PWMA pins can be floating. Pulling the PSYS pin to VCC programs input power domain rail disable. The RT3628AE will reject any commands to the input power domain rail. The unused ISENP_AUX pin and ISENN_AUX pin are recommended to connect to GND.

Acoustic Noise Suppression

The RT3628AE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band and the noise level is related to the output voltage transition amplitude ΔV. Therefore, the RT3628AE adapts acoustic noise suppression function which is enabled by pulling ANS pin to VCC to reduce ΔV when SetVID down and SetVID Decay down in DEM mode.

PIN-SETTING Mechanism

The RT3628AE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through SETx and TSEN pins. The RT3628AE adopts two-step PIN-SETTING mechanism to maximize IC pin utilization. Figure 4 illustrates this operating mechanism for SETx.

The Vdivider and V_{IXR} can be represented as follows :

$$V_{divider} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{IXR} = \frac{R2}{R1+R2} \times 3.2V + 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

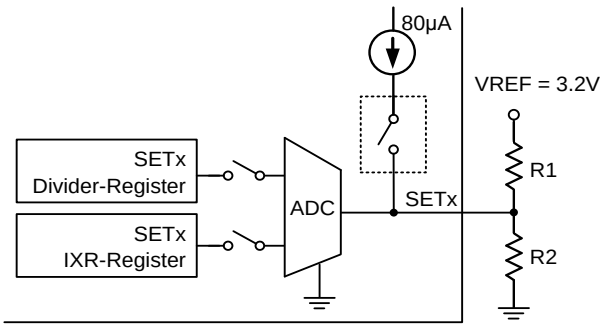

Figure 4. Operating Mechanism for SETx

The Divider-Register and the IXR-Register set the specified functions. All setting functions are summarized in Table 1.

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Table 1. Summary of Pin Setting Functions

Pin	Register	Function Setting	Symbol	Description
SET1	Divider Register[4]	DVID Fast slew rate	DVID fast_SR[4]	DVID fast_SR[4] = 0 : Fast_S DVID fast_SR[4] = 1 : Fast_P
	Divider Register[3]	I²C Address setting	I2C_ADDR[3]	I2C_ADDR[3] = 0 : 0x20h I2C_ADDR[3] = 1 : 0x21h
	Divider Register[2:0]	CORE VR TON width setting (Switching frequency)	KTON[2:0]	According to required frequency, select adaptive KTON parameter.
	IXR Register[4]	$\overline{\text{VR\_HOT}}$ assertion during DVID current limit	$\overline{\text{VR\_HOT}}$ _DVID[4]	$\overline{\text{VR\_HOT}}$ _DVID[4] = 0, Disable $\overline{\text{VR\_HOT}}$ _DVID[4] = 1, Enable
	IXR Register[3:1]	AUX VR ICCMAX	ICCMAX_AUX[3:1]	According to Platform, set AUX VR's corrsponding ICCMAX
SET2	Divider Register[4:3]	CORE VR Adaptive RAMP(AR) Trigger level in PS1	AR_TH[4:3]	AR for loop response speed-up of loading rising edge, set trigger level in PS1.
	Divider Register[2:0]	AXG VR ICCMAX	ICCMAX_A[2:0]	According to Platform, set AXG VR's corrsponding ICCMAX
	IXR Register[4]	Dual phases function	Dual_Phases[4]	Dual_Phases[4] = 0 : Each PWM output drives one phase. Dual_Phases[4] = 1 : Each PWM output drives two phases.
	IXR Register[3:1]	AXG VR TON width setting (switching frequency)	KTON_A[3:1]	According to required frequency, select adaptive KTON_A parameter.
SET3	Divider Register[4]	Selectable VID table	VIDT[4]	VIDT[4] = 0 : VID1 (0V ~ 1.52V) VIDT[4] = 1 : VID2 (0V ~ 2.74V)
	Divider Register[3:0]	Core VR ICCMAX	ICCMAX[3:0]	According to Platform, set CORE VR's corresponding ICCMAX
	IXR Register[4]	Setting VBOOT of CORE rail	VBOOT[4]	VBOOT[4] = 0 : 0V VBOOT[4] = 1 : non-zero
	IXR Register[3]	Setting VBOOT of AXG rail	VBOOT_A[3]	VBOOT_A[3] = 0 : 0V VBOOT_A[3] = 1 : non-zero
	IXR Register[2:1]	AXG VR Adaptive RAMP(AR) Trigger level	AR_TH_A[2:1]	AR for loop response speed-up of loading rising edge, set trigger level.
TSEN	Divider Register[5]	CORE VR Zero Current Detection Threshold	ZCD_TH[5]	Detect whether each phase current crosses zero current. Set trigger level.
	Divider Register[4:3]	AXG VR Current Gain	Ai_A[4:3]	Current gain setting
	Divider Register[2:1]	CORE VR Current Gain	Ai[2:1]	Current gain setting
TSENA	Divider Register[5]	Core & AXG VR sum OCP ratio	SUM_OC[5]	SUM_OC[5] = 0 : 130% x ICCMAX SUM_OC[5] = 1 : 150% x ICCMAX
	Divider Register[4]	AXG VR Zero Current Detection Threshold	ZCD_TH_A[4]	Detect whether each phase current crosses zero current. Set trigger level.
	Divider Register[3:1]	CORE VR Adaptive Quick Response(AQR) trigger level	AQR_TH[3:1]	AQR for loop response speed-up of loading rising edge. Set trigger level.

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Referring to PIN-SETTING tables Table 2 to 6, users can search corresponding Vdivider or V_{IXR} according to the desired function setting combinations. Then SETx external resistors can be calculated as follows:

$$R1 = \frac{3.2V \times V_{IXR}}{80\mu A \times V_{divider}}$$

$$R2 = \frac{R1 \times V_{divider}}{3.2V - V_{divider}}$$

Richtek provides a Microsoft Excel-based design tool to calculate the desired PIN-SETTING resisters.

The TSEN and TSENA pin also have function settings except for thermal monitoring function. It only utilizes divider part of PIN-SETTING mechanism. The detailed operation is described in Thermal Monitoring and Indicator section.

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Table 2. SET1 Pin Setting for DVID Fast SR, I2C ADDR, KTON, VR_HOT_DVID and ICCMAX_AUX

$V_{divider\_SET1}$ (mV)	DVID Fast SR	I2C ADDR	KTON	V_{IXR_SET1} (mV)	VR_HOT_DVID	ICCMAX_AUX
25	Fast_S	0x20h	0.50	50	Disable	25A
75			0.60	150		30A
125			0.70	250		35A
175			0.80	350		40A
225			0.90	450		45A
275			1.00	550		50A
325			1.10	650		55A
375			1.20	750		60A
425		0x21h	0.50	850	Enable	25A
475			0.60	950		30A
525			0.70	1050		35A
575			0.80	1150		40A
625			0.90	1250		45A
675			1.00	1350		50A
725			1.10	1450		55A
775			1.20	1550		60A
825	Fast_P	0x20h	0.50	50	Disable	25A
875			0.60	150		30A
925			0.70	250		35A
975			0.80	350		40A
1025			0.90	450		45A
1075			1.00	550		50A
1125			1.10	650		55A
1175			1.20	750		60A
1225		0x21h	0.50	850	Enable	25A
1275			0.60	950		30A
1325			0.70	1050		35A
1375			0.80	1150		40A
1425			0.90	1250		45A
1475			1.00	1350		50A
1525			1.10	1450		55A
1575			1.20	1550		60A

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Table 3. SET2 Pin Setting for AR_TH, ICCMAX_A, Dual Phases Function and KTON_A

$V_{divider\_SET2}$ (mV)	AR_TH	ICCMAX_A	SSOCP_A	V_{IXR_SET2} (mV)	Dual Phases	KTON_A
25	175mV	22A	ICCMAX*3	50	Disable	0.82
75		26A		150		0.91
125		30A	ICCMAX*2.5	250		1.00
175		34A		350		1.09
225		38A	ICCMAX*2	450		1.18
275		42A		550		1.27
325		46A	ICCMAX*1.6	650		1.36
375		50A		750		1.55
425	150mV	22A	ICCMAX*3	850	Enable	0.82
475		26A		950		0.91
525		30A	ICCMAX*2.5	1050		1.00
575		34A		1150		1.09
625		38A	ICCMAX*2	1250		1.18
675		42A		1350		1.27
725		46A	ICCMAX*1.6	1450		1.36
775		50A		1550		1.55
825	125mV	22A	ICCMAX*3	50	Disable	0.82
875		26A		150		0.91
925		30A	ICCMAX*2.5	250		1.00
975		34A		350		1.09
1025		38A	ICCMAX*2	450		1.18
1075		42A		550		1.27
1125		46A	ICCMAX*1.6	650		1.36
1175		50A		750		1.55
1225	Disable	22A	ICCMAX*3	850	Enable	0.82
1275		26A		950		0.91
1325		30A	ICCMAX*2.5	1050		1.00
1375		34A		1150		1.09
1425		38A	ICCMAX*2	1250		1.18
1475		42A		1350		1.27
1525		46A	ICCMAX*1.6	1450		1.36
1575		50A		1550		1.55

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Table 4. SET3 Pin Setting for VBOOT, VBOOT_A and AR_TH_A

V_{IXR_SET3} (mV)	VBOOT	VBOOT_A	AR_TH_A
50	0.0V	0.0V	Disable
150			125mV
250			175mV
350			225mV
450		non-zero	Disable
550			125mV
650			175mV
750			225mV
850	non-zero	0.0V	Disable
950			125mV
1050			175mV
1150			225mV
1250		non-zero	Disable
1350			125mV
1450			175mV
1550			225mV

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Table 5. SET3 Pin Setting for VIDT and ICCMAX

$V_{divider\_SET3}$ (mV)	VIDT	ICCMAX							SSOCP
		83[4]= 0 Each PWM output drives one phase.					83[4] = 1 Each PWM output drives two phases.		
		4 phase	5 phase	6 phase	7 phase	8 phase	8 phase	10/12/14/16 phase	
25	VID1	93A	134A	170A	206A	232A	232A	233A	ICCMAX*2.5
75		100A	140A	176A	212A	238A	238A	240A	
125		107A	146A	182A	218A	244A	244A	247A	
175		114A	152A	188A	224A	250A	250A	254A	
225		121A	158A	194A	230A	256A	256A	260A	ICCMAX*2.25
275		128A	164A	200A	236A	262A	262A	268A	
325		135A	170A	206A	242A	268A	268A	274A	
375		142A	176A	212A	248A	274A	274A	282A	
425		149A	182A	218A	254A	280A	280A	288A	ICCMAX*2
475		156A	188A	224A	260A	286A	286A	296A	
525		163A	194A	230A	266A	292A	292A	302A	
575		170A	200A	236A	272A	298A	298A	310A	
625		177A	206A	242A	278A	304A	304A	316A	ICCMAX*1.75
675		184A	212A	248A	284A	310A	310A	324A	
725		191A	218A	254A	290A	316A	316A	330A	
775		198A	224A	260A	296A	322A	322A	338A	
825	VID2	93A	134A	170A	206A	232A	232A	233A	ICCMAX*2.5
875		100A	140A	176A	212A	238A	238A	240A	
925		107A	146A	182A	218A	244A	244A	247A	
975		114A	152A	188A	224A	250A	250A	254A	
1025		121A	158A	194A	230A	256A	256A	260A	ICCMAX*2.25
1075		128A	164A	200A	236A	262A	262A	268A	
1125		135A	170A	206A	242A	268A	268A	274A	
1175		142A	176A	212A	248A	274A	274A	282A	
1225		149A	182A	218A	254A	280A	280A	288A	ICCMAX*2
1275		156A	188A	224A	260A	286A	286A	296A	
1325		163A	194A	230A	266A	292A	292A	302A	
1375		170A	200A	236A	272A	298A	298A	310A	
1425		177A	206A	242A	278A	304A	304A	316A	ICCMAX*1.75
1475		184A	212A	248A	284A	310A	310A	324A	
1525		191A	218A	254A	290A	316A	316A	330A	
1575		198A	224A	260A	296A	322A	322A	338A	

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Table 6. TSEN Pin Setting for ZCD_TH, Ai_A and Ai

V_{TSEN} (mV)	ZCD_TH	Ai_A	Ai
50	0.417mV	0.75	0.25
150			0.50
250			0.75
350			1.00
450		1.13	0.25
550			0.50
650			0.75
750			1.00
850		1.50	0.25
950			0.50
1050			0.75
1150			1.00
1250		1.88	0.25
1350			0.50
1450			0.75
1550			1.00
1650	0.208mV	0.75	0.25
1750			0.50
1850			0.75
1950			1.00
2050		1.13	0.25
2150			0.50
2250			0.75
2350			1.00
2450		1.50	0.25
2550			0.50
2650			0.75
2750			1.00
2850		1.88	0.25
2950			0.50
3050			0.75
3150			1.00

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Table 7. TSENA Pin Setting for SUM_OC, ZCD_TH_A and AQR_TH

V_{TSENA} (mV)	SUM_OC	ZCD_TH_A	AQR_TH
50	130%	0.063mV	240mV
150			400mV
250			560mV
350			800mV
450			880mV
550			1040mV
650			1200mV
750			Disable
850		0.188mV	240mV
950			400mV
1050			560mV
1150			800mV
1250			880mV
1350			1040mV
1450			1200mV
1550			Disable
1650	150%	0.063mV	240mV
1750			400mV
1850			560mV
1950			800mV
2050			880mV
2150			1040mV
2250			1200mV
2350			Disable
2450		0.188mV	240mV
2550			400mV
2650			560mV
2750			800mV
2850			880mV
2950			1040mV
3050			1200mV
3150			Disable

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Thermal Monitoring and Indicator

The TSEN pin processes two functions of PIN-SETTING (function setting) and thermal monitoring. After power on, TSEN has three operation modes: PIN-SETTING, Pre-Thermal Sense and Thermal Sense Mode. The corresponding function blocks of the three modes are shown in Figure 5. In PIN-SETTING Mode, the TSEN pin voltage = 3.2V x R2 / (R1+R2) with VREF = 3.2V and is coded by ADC and stored in PIN-SETTING register. In Pre-Thermal Sense Mode, the TSEN pin voltage = 0.6V x R2 / (R1+R2) with VREF = 0.6V and is coded and stored in Pre-Thermal Register. This part helps Thermal Sense Mode calculation. In Thermal Sense Mode, the TSEN pin voltage = 0.6V x R2 / (R1+R2) + 80μA x [(R1//R2)+R3] with VREF = 0.6V and is coded. Subtracting Pre-Thermal Register code, the result is stored in Thermal Register (The corresponding TSEN voltage = 80uA x [(R1//R2)+R3] which is defined as Thermal Voltage. The R3 is the NTC thermistor network to sense temperature.) The NTC thermistor is recommended to be placed near the MOSFET, the hottest area in the PCB. Higher temperature causes smaller R3 and lower TSEN. According to NTC thermistor temperature curve, design Thermal Voltage vs Temperature with proper R3 network to meet Table 8. The R_{NTC} = 100kΩ with Beta = 4250 is recommended. The 100°C Thermal Voltage = 80μA x [(R1//R2)+R3(100°C)] = 0.6V must be meet. The controller processes the TSEN pin voltage to report temperature zone register. While the TSEN pin voltage is less than 0.6V, the $\overline{VR\_HOT}$ is pulled low. The Thermal Register data is update every 75us and the averaging interval is 600μs. The resistance accuracy of TSEN network is recommended to be less than 1% error.

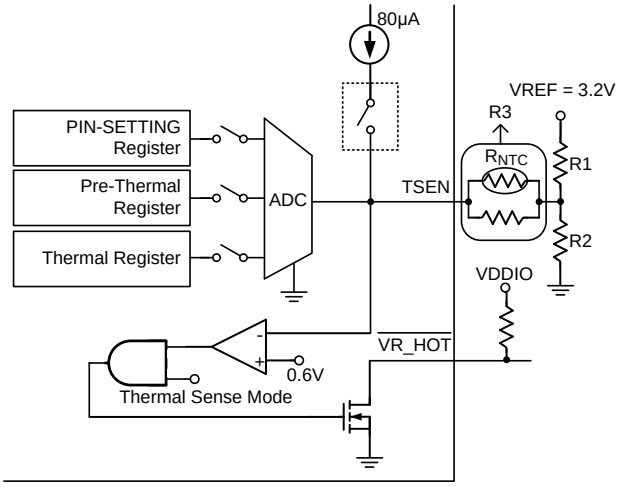

Figure 5. Multi-Function Pin Setting Mechanism for TSEN

Table 8. Thermal Zone and Detection Encoding with R_{NTC} = 100kΩ, Beta = 4250K

Temperature	Thermal Voltage 80uA x [(R1//R2)+R3]	Temperature Zone Register
100℃	0.600V	FFh
97℃	0.628V	7Fh
94℃	0.658V	3Fh
91℃	0.690V	1Fh
88℃	0.725V	0Fh
85℃	0.761V	07h
82℃	0.800V	03h
75℃	0.900V	01h

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System Input Power Monitoring (PSYS)

The RT3628AE provides PSYS function to monitor total platform system power and report to the CPU via SVID interface. The PSYS function can be illustrated as in Figure 6. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. The R_{PSYS} is designed for the PSYS voltage = 1.6V with maximum I_{PSYS} for 100% system input power. 1.6V is a full-scale analog signal for FFh digitized code.

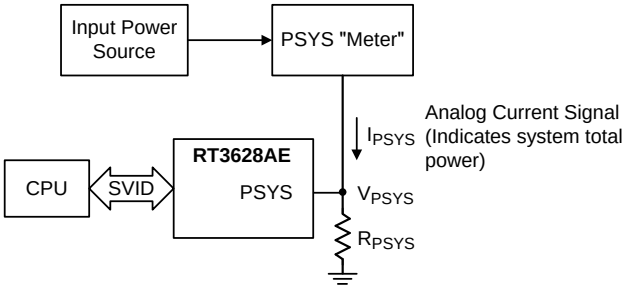

Figure 6. PSYS Function Block Diagram

System Input Voltage Monitoring (VSYS)

The RT3628AE provides optional VSYS function to monitor system input voltage. The threshold can be set through SVID interface and FFh digitized code indicates for 24V input voltage (24V/255 per code). As if input voltage lower than critical threshold, controller will assertion $\overline{VR\_HOT}$.

Zero Load-line

The RT3628AE also can support enable zero loadline function. When zero loadline function is enabled, the output voltage is determined only by VID and does not vary with the loading current like loadline system behavior. The RT3628AE adopts a new feature, i.e. AC-droop, to effectively suppress load transient ring back and to control overshoot for zero loadline application. Figure 7 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring back $\Delta V2$ due to C area charge. Figure 8 shows the condition with AC-droop control. While loading occurs, the controller changes VID target to short-term voltage target temporarily. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as following :

$$Short\_Term\_Voltage\_Target = VID - \Delta I_{CC} \times R_{LL}$$

The setting method of R_{LL} is the same as load-line system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can help inductor current not to exceed loading current too much and then the ring back $\Delta V2$ can be suppressed. The overshoot amplitude is reduced to only $\Delta V3$.

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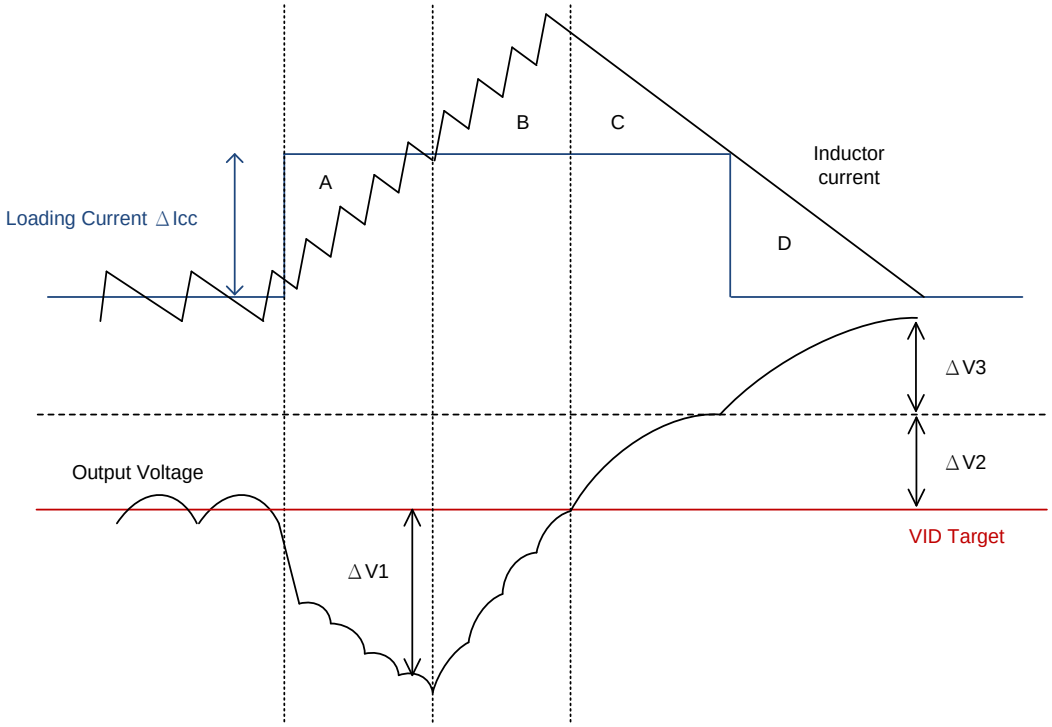

Figure 7. Zero Load-line without AC-droop Control

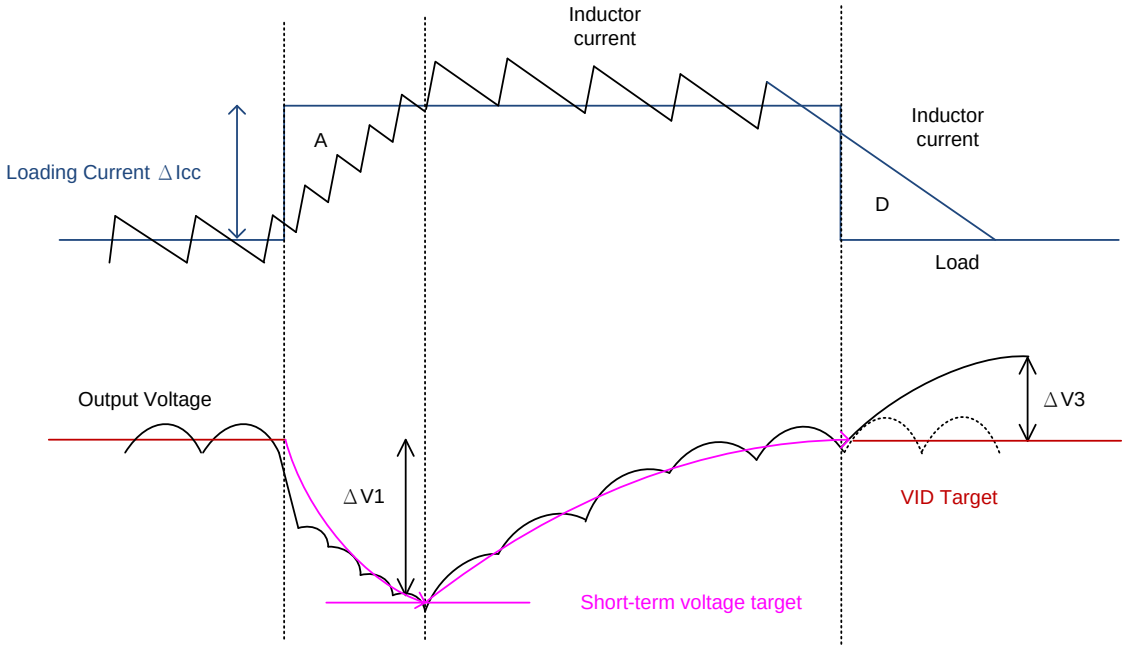

Figure 8. Zero Loadline with AC-droop Control

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PS4 Quiescent Current

To achieve PS4 power consumption requirement for notebook, the I²C function can be disable to save more power consumption by tying SM_SCL and SM_SDA to GND. The judgment mechanism is illustrated in Figure 9. The RT3628AE disables I²C I/O if SM_SCL and SM_SDA remain low state within 2.2ms after asserting VR_READY, and does not enable I²C I/O even SM_SCL and SM_SDA are pulled high after 2.2ms. Note: For I²C application, the SM_SCL & SM_SDA pull high voltage must be ready before asserting VR_READY, otherwise, the I²C function is disabled.

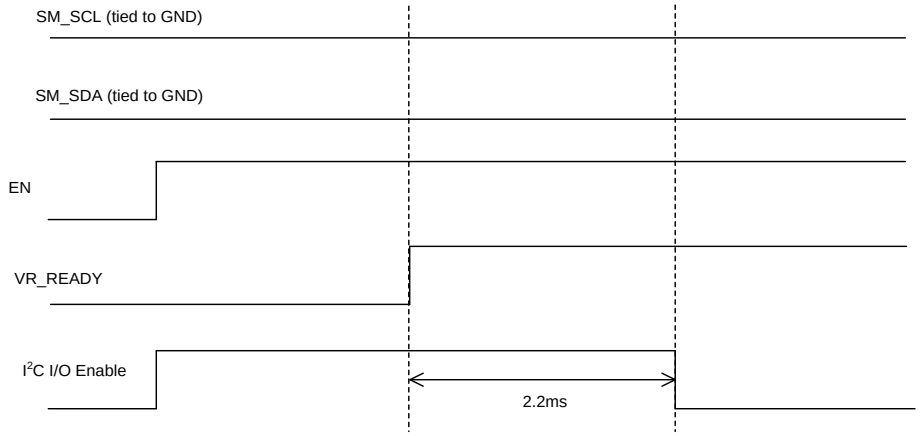

Figure 9. Disable I²C Function Judgment Mechanism

Soft-Start OC Protection (SSOCP)

The RT3628AE supports soft-start OC protection (SSOCP) to prevent output terminal short-circuit during soft-start period. During soft-start + 60μs period, the RT3628AE will sense IMON voltage to prevent large current damage power MOSFET. Once SSOCP is triggered, controller will de-assert VR_READY and latch PWM in tri-state to turn off high-side and low-side power MOSFET. SSOCP threshold depends on ICCMAX value that can be referenced in Table 3 and Table 5.

CORE VR

Per Phase Current Sense

To achieve higher efficiency, the RT3628AE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 10. An external low-pass filter R_{X1} and C_X, reconstructs the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant $\frac{L_X}{DCR}$ of Inductance and DCR. It's necessary to fine tune RX1 and CX for transient performance and current reporting. If RC network time constant matches inductor time constant $\frac{L_X}{DCR}$, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L_X}{DCR}$, VCORE waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant $\frac{L_X}{DCR}$, VCORE waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP). Figure 11 shows the output waveforms according to the RC network time constant.

The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the I_{OUT} reporting accuracy. The C_X is suggested to be 0.1μF X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{INT.}} = \frac{I_{Lx} \times DCR}{R_{INT.}}$$

The R_{X2} is optional for prevent V_{CSIN} exceeding current sense amplifier input range. The time constant of $(R_{X1}//R_{X2}) \times C_X$ should match $\frac{L_X}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{INT.}} = \frac{I_{Lx} \times DCR}{R_{INT.}} \times \frac{R_{X2}}{R_{X1}+R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero

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current. The mirrored current to IMON pin is 1.25 time of $I_{CS,PER}$

($I_{IMON}=A_{MIRROR}\times I_{CS,PERx}$, $A_{MIRROR}=1.25$)

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

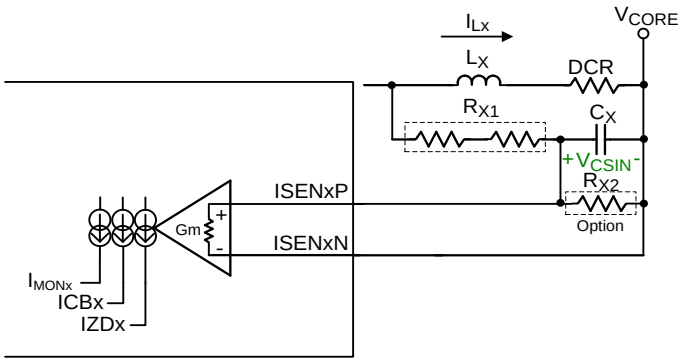

Figure 10. Inductor DCR Current Sensing Method

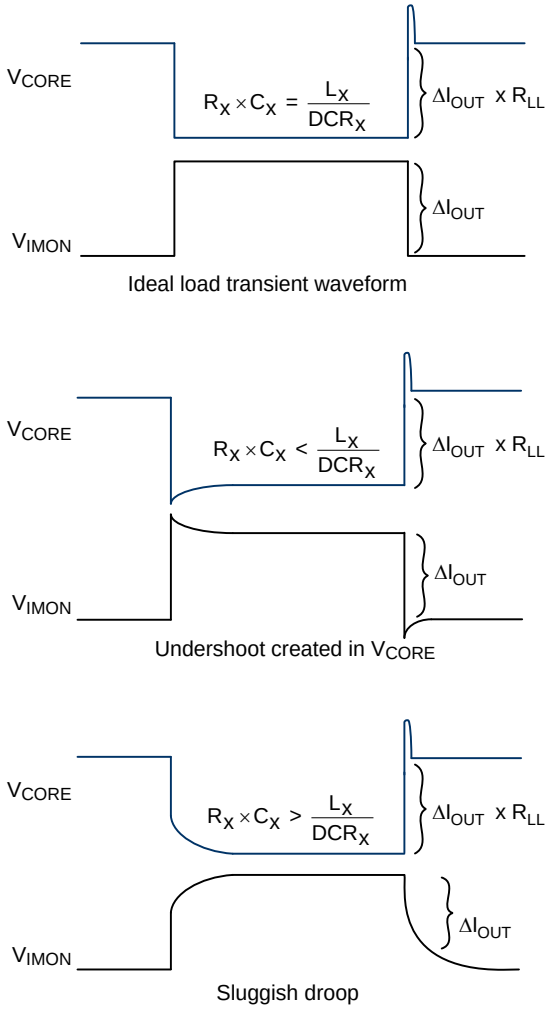

Figure 11. All Kinds of RC Network Time Constant

Total Current Sense/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3628AE adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within IMON resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase. Figure 12 shows the configuration. All phase current signals are gathered to IMON pin and converted to a voltage signal V_{IMON} by $R_{IMON,EQ}$ based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as V_{VREF}) while normal operation. The relationship between V_{IMON} and inductor current I_{Lx} is:

$$V_{IMON}-V_{VREF}=(I_{L1}+I_{L2}+I_{L3}+I_{L4}+I_{L5}+I_{L6}+I_{L7}+I_{L8})\times\frac{DCR}{R_{INT.}}$$

$$\times 1.25\times R_{IMON,EQ}$$

V_{IMON}-V_{VREF} is proportional to output current. V_{IMON}-V_{VREF} is used for output current reporting and load-line loop-control and Sum over-current protection. For the former, V_{IMON}-V_{VREF} is averaged by analog low-pass filter and then outputs to 8-bit ADC. The digitized reporting value is scaled such that FFh = ICCMAX. The RT3628AE provides several ICCMAX selections through PIN-SETTING of ICCMAX[3:0]. The setting value determines Intel ICCMAX register value. $R_{IMON,EQ}$ should be designed according to ICCMAX value, that is $V_{IMON} – V_{VREF}$ = 0.4 while (I_{L1} + I_{L2} + I_{L3} + I_{L4} + I_{L5} + I_{L6} + I_{L7} + I_{L8}) = ICCMAX = ICCMAX register. For load-line loop-control, V_{IMON}-V_{VREF} is scaled by Ai, that can be selected by PIN-SETTING of Ai[2:1]. The detailed application is described in the load-line setting section.

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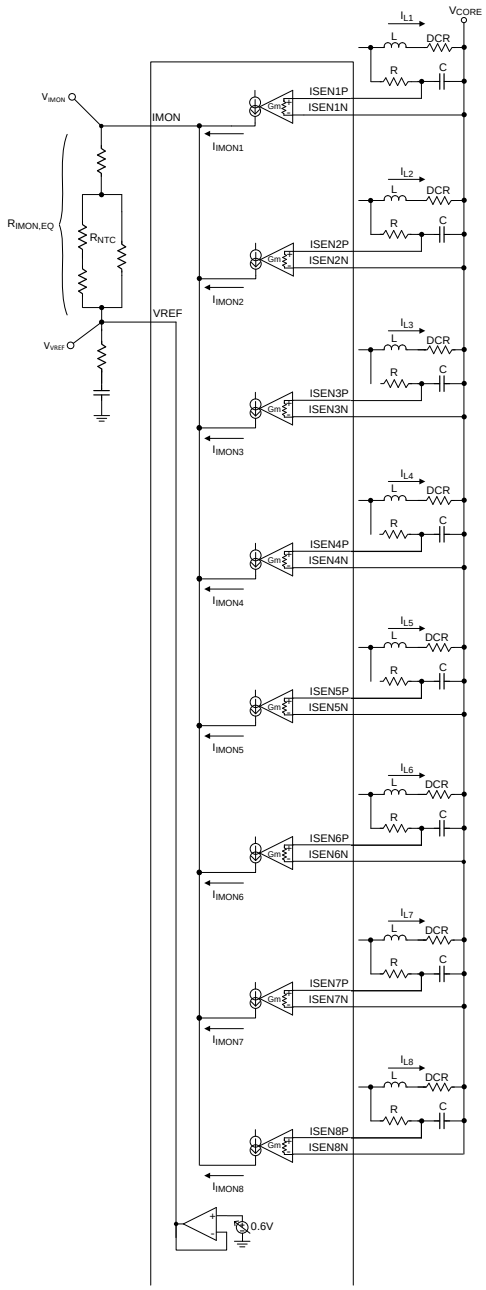

Figure 12. Total Current Sense Method

Load-line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount which is proportional to the increasing loading current. The slope between output voltage and loading current (R_{LL}) is shown in Figure 13. Figure 14 shows how the voltage and current loop parameters of RT3628AE to achieve load-line. The detailed equation is described as following :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{INT.}} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times \frac{15}{4}$$

Ai is current gain. $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and is suggested within 2.5~3.5 for better transient response. RLL can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by PIN-SETTING of Ai[2:1] as listed in Table 9.

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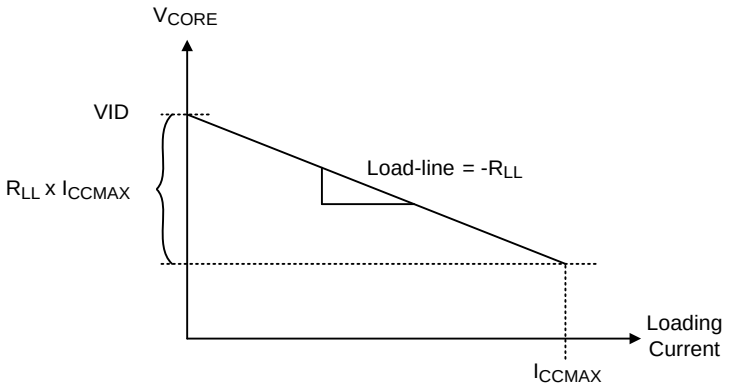

Figure 13. Load-Line (Droop)

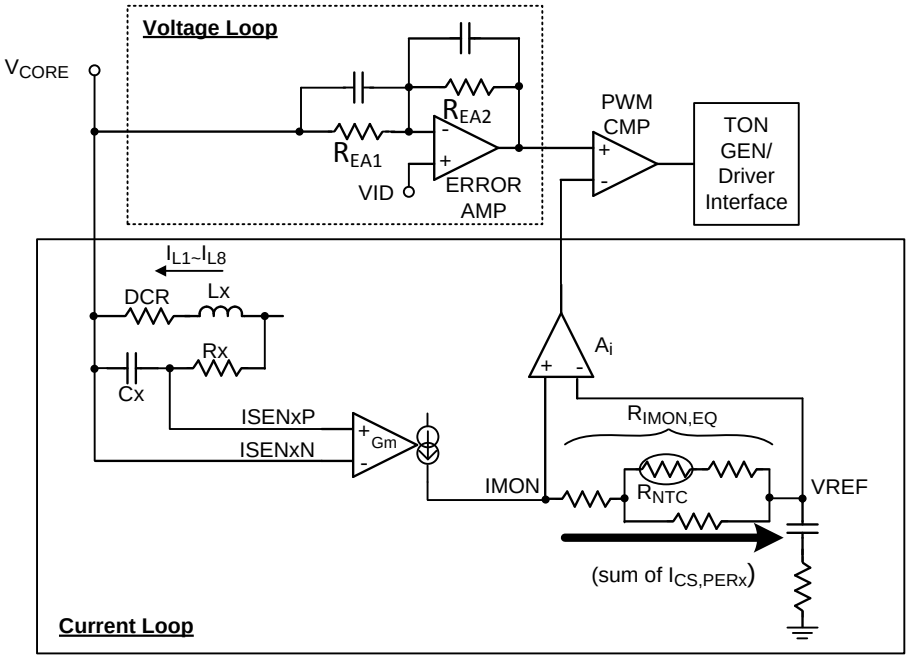

Figure 14. Voltage Loop and Current Loop for Load-line

Table 9. PIN-SETTING of Ai[2:1]

Ai[2:1]	Current Gain Setting
00	0.25
01	0.50
10	0.75
11	1.00

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Dynamic VID (DVID) Compensation

During DVID transition, an extra current is required to charge output capacitor for increasing voltage. The charging current approximates to the product of the DVID slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to DVID Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, Ω). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 15. The RT3628AE provides one DVID compensation function as shown in Figure 16. An internal current IDVID_LIFT sinks internally from FB pin to generate DVID compensation $I_{DVID\_LIFT} \times R_{EA1}$. The I_{DVID_LIFT} for fast DVID SR is 5μA for Core rail, 20μA for AXG rail. For different scale of DVID SR, the I_{DVID_LIFT} is internally adjusted. Compensating magnitude can also be adjusted by R_{EA1}. When DAC output reaches the target ($\overline{ALERT}$ issue timing), inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitance (The magnitude is related with inductor, capacitance and VID). Thus DVID compensation current can be less than DVID Slew Rate x Output Capacitance (Capacitance degeneration should be considered). While output capacitance is so larger that DVID compensation cannot cover, adding resistor and capacitance from FB to GND also can provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects DVID behavior. The final setting should be based on actual measurement.

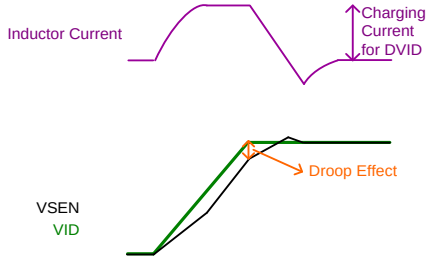

Figure 15. Droop Effect in VID Transition

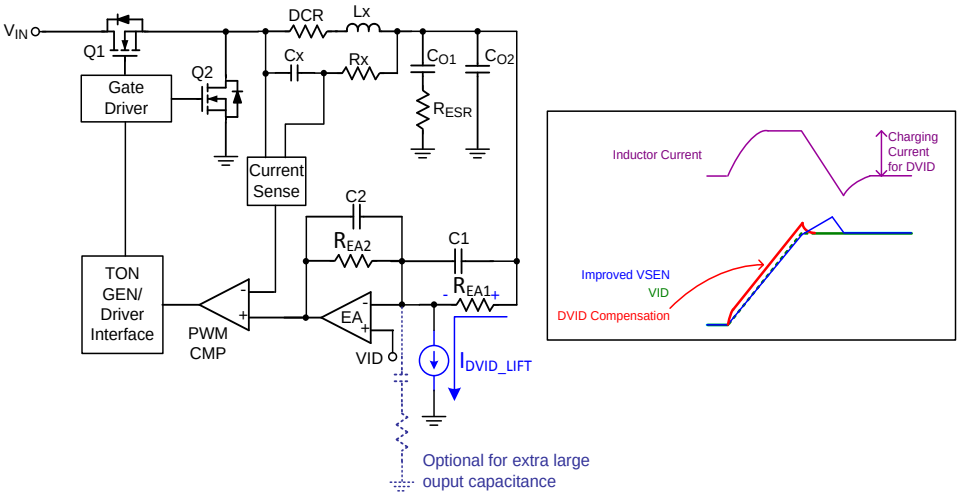

Figure 16. DVID Compensation

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Compensator Design

The RT3628AE doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 17. For IMVP9.1 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Refer to the design tool for default compensator values.

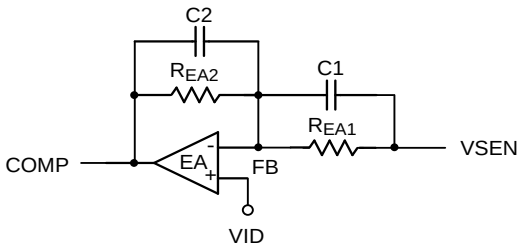

Figure 17. Type I Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, VCC_SENSE and VSS_SENSE. The related connection is shown in Figure 18. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

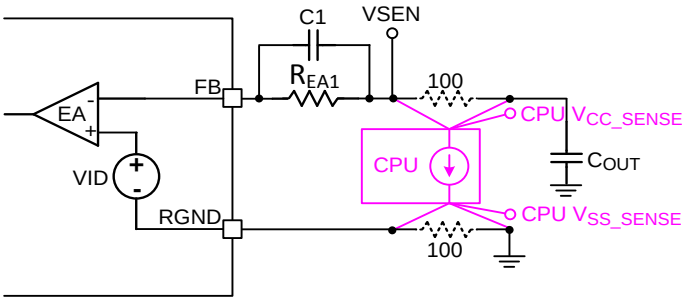

Figure 18. Remote Sensing Circuit

Switching Frequency Setting

The G-NAVP^{TM} (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive TON (PWM) with input voltage (VIN) for better line regulation. The TON is also adaptive to VID voltage to achieve constant frequency concept. The constant switching frequency operation makes the thermal estimation easy. The RT3628AE provides a parameter setting of k_{TON} to design TON width. The k_{TON} is set by PIN-SETTING of KTON[2:0]. The related setting table is listed in Table 10.

The equations of TON are listed as below :

VID>0.9V,

$$T_{ON}=2u\times\frac{VID}{k_{TON}\times V_{IN}}$$

VID≤0.9V,

$$T_{ON}=2u\times\frac{0.9V}{k_{TON}\times V_{IN}}$$

Table 10. PIN-SETTING of KTON

KTON[2:0]	k_{TON}
000	0.50
001	0.60
010	0.70
011	0.80
100	0.90
101	1.00
110	1.10
111	1.20

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The switching frequency can be derived from T_{ON} as shown below. The losses in the main power stage and driver characteristics are considered.

$$Freq=\frac{VID+\frac{I_{CC}}{N}\times(DCR+\frac{R_{ON_{LS,max}}}{n_{LS}}-N\times R_{LL})}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ON_{LS,max}}}{n_{LS}}-\frac{R_{ON_{HS,max}}}{n_{HS}}\right)\right]\times(T_{ON}-T_D+T_{ON,\,VAR})+\frac{I_{CC}}{N}\times\frac{R_{ON_{LS,max}}}{n_{LS}}\times T_D}$$

VID: VID voltage

V_{IN}: input voltage

I_{CC}: loading current

N: total phase number

$R_{ON_{HS,max}}$: maximum equivalent of the high-side $R_{DS(ON)}$

n_{HS}: number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent of the low-side $R_{DS(ON)}$

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

$T_{ON,\,VAR}$: on-time variation value

DCR: inductor DCR

R_{LL}: load-line setting (Ω)

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Adaptive Quick Response (AQR)

The RT3628AE provides Adaptive Quick Response (AQR) to optimize transient response. The mechanism concept is illustrated in Figure 19. Controller detects output voltage drop slew rate. While the slew rate exceeds the AQR threshold, all PWMs turn on until output voltage slew rate significantly slows down. The output voltage slew rate transition also indicates that inductor current almost reaches the loading current. Under such mechanism, AQR PWM width is adaptive to variable loading step. The RT3628AE provides various AQR threshold through PIN-SETTING of AQR_TH[3:1]. The following equation can initially decide the AQR starting trigger threshold. Smaller threshold indicates larger AQR PWM. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid triggering AQR abnormally.

$$\text{AQR Starting Trigger Threshold} = -4\mu \times \frac{dVSEN}{dt}$$

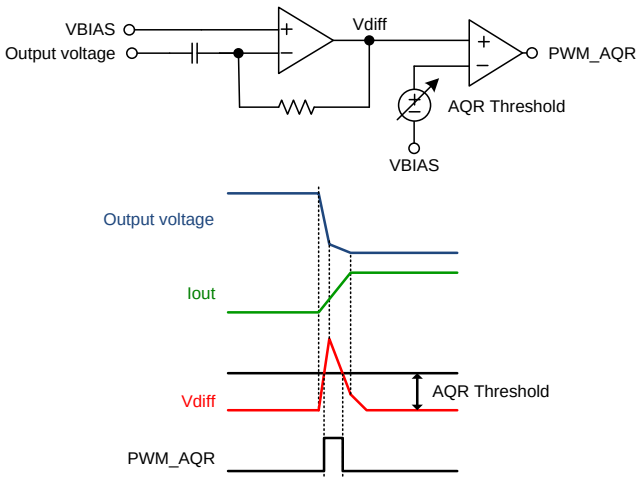

Figure 19. Adaptive Quick Response Mechanism

Table 11. PIN-SETTING of AQR_TH

AQR_TH[3:1]	AQR Starting Trigger Threshold (mV)
000	240
001	400
010	560
011	800
100	880
101	1040
110	1200
111	Disable

Anti-overshoot (ANTI-OVS)

The RT3628AE provides Anti-overshoot function to suppress output voltage overshoot. Controller detects overshoot by signals relating to output voltage. The overshoot trigger level can be adjusted by I2C Reg0x7C[2:0]. The main detecting signal comes from COMP. However, COMP varies with compensation. Initial trigger level setting can be based on the following equation :

$$\Delta COMP \times \frac{4}{3} = \Delta VSEN \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{ANTI-OVS Threshold}$$

The final setting depends on the actual Error AMP compensator design and measurement.

While overshoot exceeds the trigger level setting, all PWMs keep in tri-state until the zero current is detected or VSEN back to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

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ACLL Performance Enhancement

The RT3628AE provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. Controller detects COMP signal and compares it with steady state. While VCOMP variation exceeds a threshold, an additional positive offset is added to the output voltage. The threshold can be set through PIN-SETTING AR_TH[4:3], as listed in Table 12. The smaller index indicates that the detection is triggered easily. Figure 20 shows undershoot suppression behavior in PS1. For different platform, the optimized setting is different. The final setting must be based on actual measurement.

Table 12. PIN-SETTING of Undershoot Suppression

AR_TH[4:3]	Adaptive RAMP Trigger Level (mV)
00	175
01	150
10	125
11	Disable

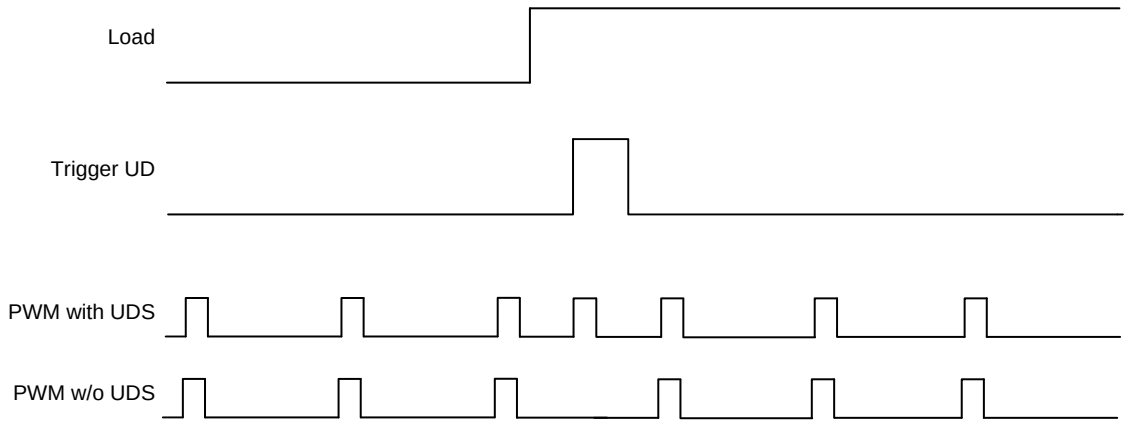

Figure 20. Undershoot Suppression Behavior in PS1

Over-current Protection (OCP)

The RT3628AE has sum OCP mechanisms and the threshold of sum OCP for PS0 is defined as

$$I_{SUM\_OC,PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}\times\frac{1}{1.25}$$

The PS1/2/3 sum OCP threshold is defined as

$$I_{SUM\_OC,nonPS0}=\frac{1}{3}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}\times\frac{1}{1.25};\ \text{when } 110A\le ICCMAX<145A$$

$$I_{SUM\_OC,nonPS0}=\frac{1}{4}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}\times\frac{1}{1.25};\ \text{when } 145A\le ICCMAX<215A$$

$$I_{SUM\_OC,nonPS0}=\frac{1}{5}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}\times\frac{1}{1.25};\ \text{when } 215A\le ICCMAX\le 300A$$

While $R_{IMON,EQ}$ is designed exactly for

$$VIMON_{ICCMAX}=\text{ICCMAX register value}\times\frac{DCR}{R_{INT.}}\times 1.25\times R_{IMON,EQ},$$

ICCMAX register value = ICCMAX, and $VIMON_{ICCMAX}$ = 0.4V.

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The KSOCP is sum OCP ratio which value is 0.6~1.6 and it is set by Pin Setting Function of TSENA & I2C register 0x73h[2:0]. The sum OCP threshold can be simplified as $I_{SUM\_OC,PS0}=K_{SOCP}\times ICCMAX$ and $I_{SUM\_OC,nonPS0}=\frac{1}{K}\times ICCMAX$. Note that the modification of ICCMAX register value cannot change sum OCP threshold. While inductor current above sum OCP threshold lasts 20μs / 40μs (set by I2C register 0x73h[7].) controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs. Sum OCP is masked during DVID period and 80μs after VID settles. They are also masked while VID = 0V condition.

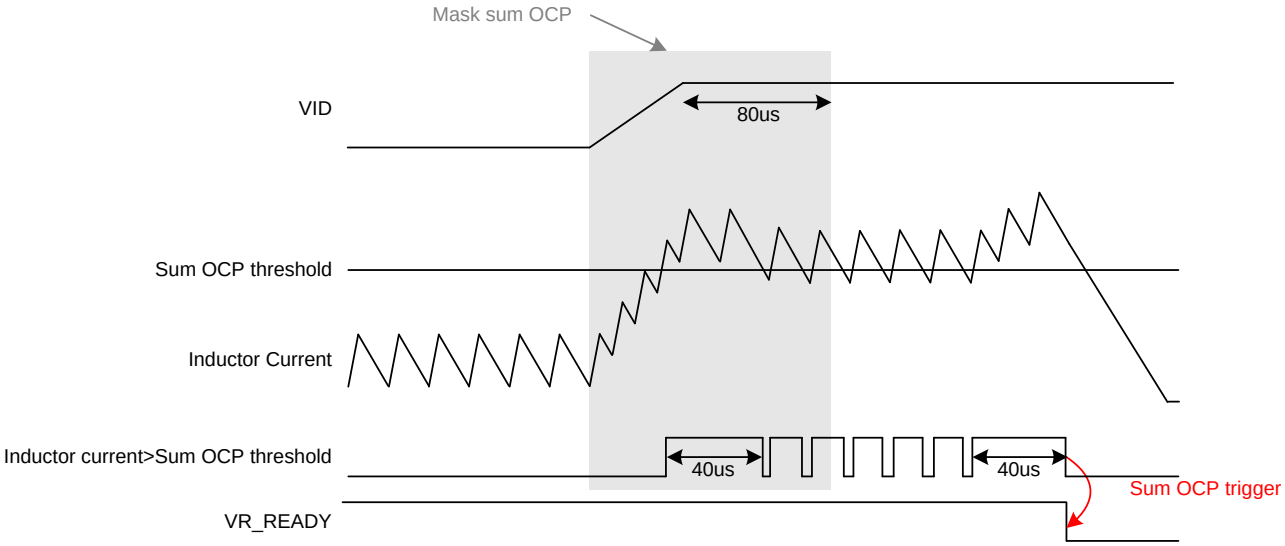

Figure 21. SUM OC Protection Mechanism

Over-Voltage Protection (OVP)

The OVP threshold is linked to VID. The classification table is illustrated in Table 13. While VID = 0V, in case of VR internal setting mode, DACOFF or PS4, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, the OVP threshold is 2.45V or 2.65V which depends on VID table to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID ≤ 1.0V, the OVP threshold is limited at 1.35V.

.

The OV protection mechanism is illustrated in Figure 22. When OVP is triggered with 0.5μs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. The PWM remains low until the output voltage is pulled down below VID. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. Controller controls PWM to be low or tri-state to pull down the output voltage along with VID

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Table 13. Summary of Over Voltage Protection

VID Condition	OVP Threshold	Example	Protection Flag	Protection Action	Protection Reset
VID=0 (EN=L or VR internal setting mode or DACOFF or PS4)	OVP is masked.		VREF=1V		VCC/EN Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	Threshold is set by 0x75h. Default is 2.45V or 2.65V which depends on VID table.			VR_READY latched low. The output voltage is pulled down to below SSOVP-0.35V and then ramps down to 0V.	
DVID period from non-zero VID	VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.		VR_READY latched low. The output voltage is pulled down to below VID and then ramps down to 0V.	
VID≠0	VID+350mV if VID >1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.			

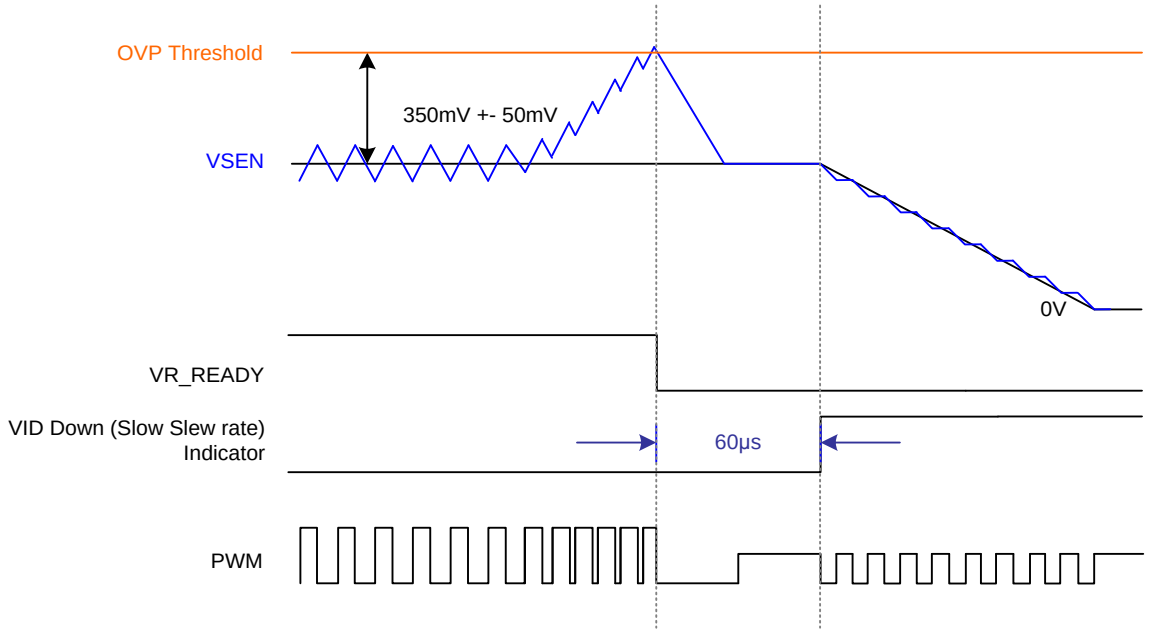

Figure 22. Over Voltage Protection Mechanism

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Under Voltage Protection

When the output voltage is lower than VID-650mV with 3μs filter time, the UVP is triggered and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. The UVP is masked during DVID period and 80us after VID settles. The mechanism is illustrated in Figure 23.

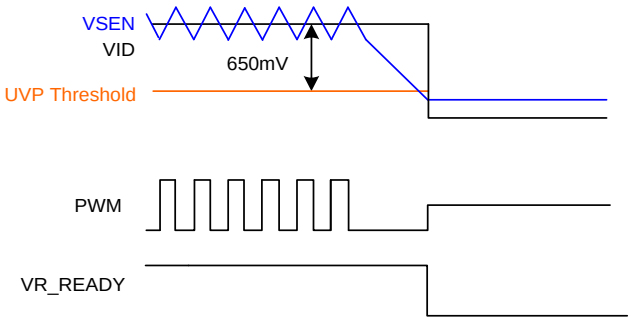

Figure 23. Under Voltage Mechanism

All protections are reset only by VCC/EN toggle. The UVP and OCP protections are listed in Table 14. Note that the real filter time also depends on the magnitude of detected signal. The signal magnitude will affect analog comparator's overdrive voltage and output slew rate. For user friendly operation, the RT3628AE provides protection flag to promptly determine which kind of protections is triggered. As protection happens, the VREF is pulled to 1V/1.5625V/2V for OVP/UVP/SUM_OCP respectively.

Table 14. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Flag	Protection Action	DVID mask time	Protection Reset
Sum OCP for PS0	$I_{SUM\_OC,PS0}=K_{SOCP}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}$	VREF=2V	PWM tri-state, VR_READY latched low	DVID + 80us	VCC/EN Toggle
Sum OCP for non PS0	$I_{SUM\_OC,nonPS0}=\frac{1}{K}\times VIMON_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMON,EQ}}$	VREF=2V			
UVP	VID-650mV	VREF=1.5625 V			

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AXG VR

Per Phase Current Sense

To achieve higher efficiency, the RT3628AE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 24. An external low-pass filter R_{AX1} , R_{AX2}_eq and C_{AX} reconstructs the current signal. Where R_{AX2} is necessary for DCR temperature compensation. The time constant of (R_{AX1}//R_{AX2}) x C_{AX} should match $\frac{L_{AX}}{DCR}$. If RC network time constant matches inductor time constant, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant, V_{CORE} waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant, V_{CORE} waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP). Figure 25 shows the output waveforms according to the RC network time constant.

$$I_{CSA,PERx}=\frac{V_{CSIN}}{R_{INT.}}=\frac{I_{LAx}\times DCR}{R_{INT.}}\times\frac{R_{AX2\_eq}}{R_{AX1}+R_{AX2\_eq}}$$

The current signal $I_{CSA,PERx}$ is mirrored for load-line control/current reporting, current balance, and zero current detection. The mirrored current to IMONA pin is 1.25 time of $I_{CSA,PER}$

($I_{IMONA}=A_{MIRROR}\times I_{CSA,PERx}$, $A_{MIRROR}=1.25$)

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

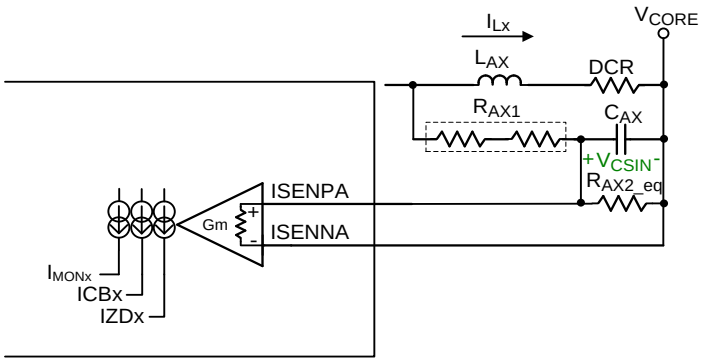

Figure 24. Inductor DCR Current Sensing Method

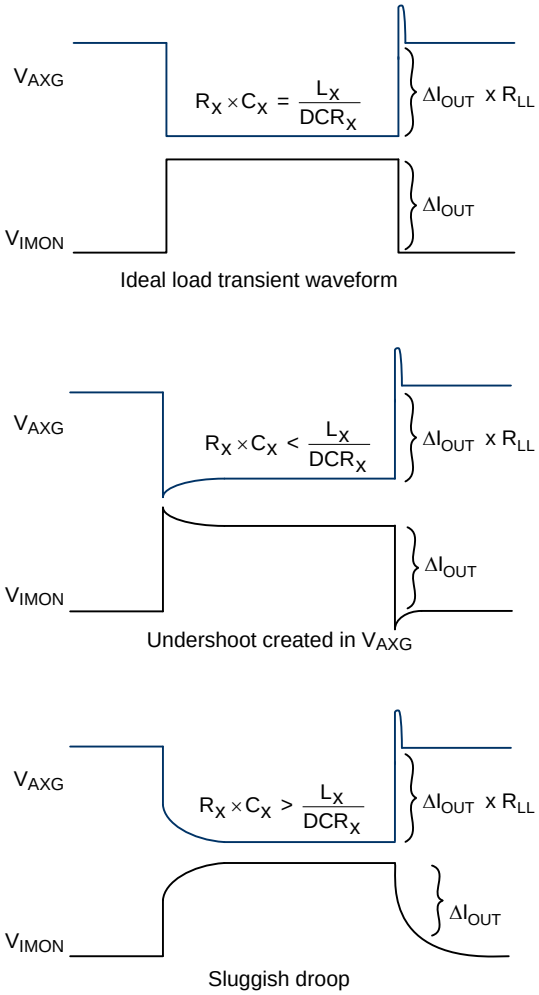

Figure 25. All Kinds of RC Network Time Constant

Total Current Sense/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The NTC resistor is designed within DCR current sense network. It is suggested to be placed near the inductor of the first phase. Figure 26 shows the configuration. Current signals are gathered to IMONA pin and converted to a voltage signal V_{IMONA} by R_{IMONA} based on VREF pin. VREF pin provides 0.6V voltage source (as presented as V_{VREF}) while normal operation. The relationship between VIMONA and inductor current I_{LAx} is:

$$V_{IMONA}-V_{VREF}=(I_{LA1})\times\frac{DCR}{R_{INT.}}\times\frac{R_{AX2\_eq}}{R_{AX1}+R_{AX2\_eq}}\times1.25\times R_{IMONA}$$

$V_{IMONA}-V_{VREF}$ is proportional to output current. $V_{IMONA}-V_{VREF}$ is used for output current reporting and

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load-line loop-control. V_{IMONA}-V_{VREF} is averaged by analog low-pass filter and then outputs to 8-bit ADC. The digitized reporting value is scaled such that FFh = ICCMAX. The RT3628AE provides several ICCMAX selections through PIN-SETTING of ICCMAX_A[2:0]. The setting value determines Intel ICCMAX register value. The R_{IMONA} should be designed according to ICCMAX register value, that is V_{IMONA} - V_{VREF} = 0.4V while I_{LA1} = ICCMAX register value.

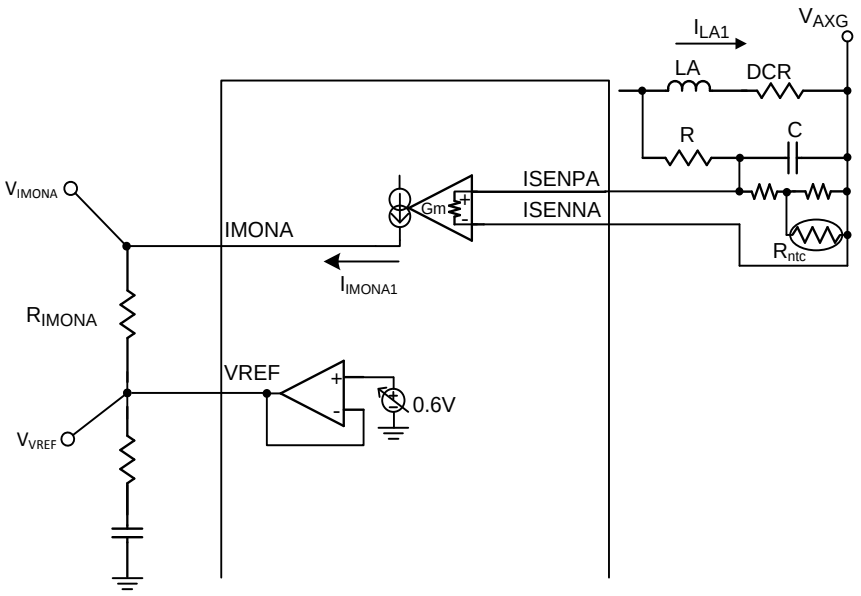

Figure 26. Total Current Sense Method

Load-line Setting (R_{LL})

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount which is proportional to the increasing loading current, i.e. the slope between output voltage and loading current (R_{LL}) is shown in Figure 27. Figure 28 shows how the voltage and current loop parameters of RT3628AE to achieve load-line. The detailed equation is described as below :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{R_{INT}} \times \frac{R_{EQ}}{R_{X1} + R_{EQ}} \times \frac{A_i\_A}{\frac{RA_{EA2}}{RA_{EA1}}} \times 20$$

Ai_A is current gain, $\frac{RA_{EA2}}{RA_{EA1}}$ is ERROR AMP gain and suggested within 2.5~3.5 for better transient response.

R_{LL} can be programmed by Ai_A and $\frac{RA_{EA2}}{RA_{EA1}}$. Ai_A can be selected by PIN-SETTING of Ai_A [4:3] as listed in Table 15.

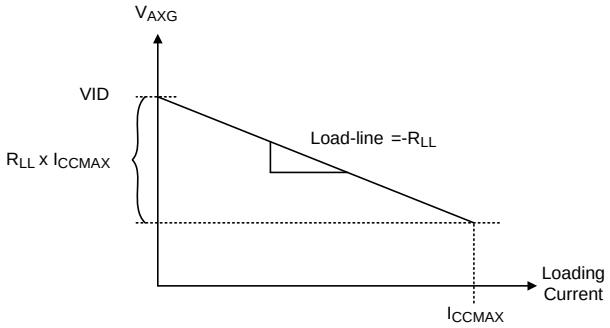

Figure 27. Load-Line (Droop)

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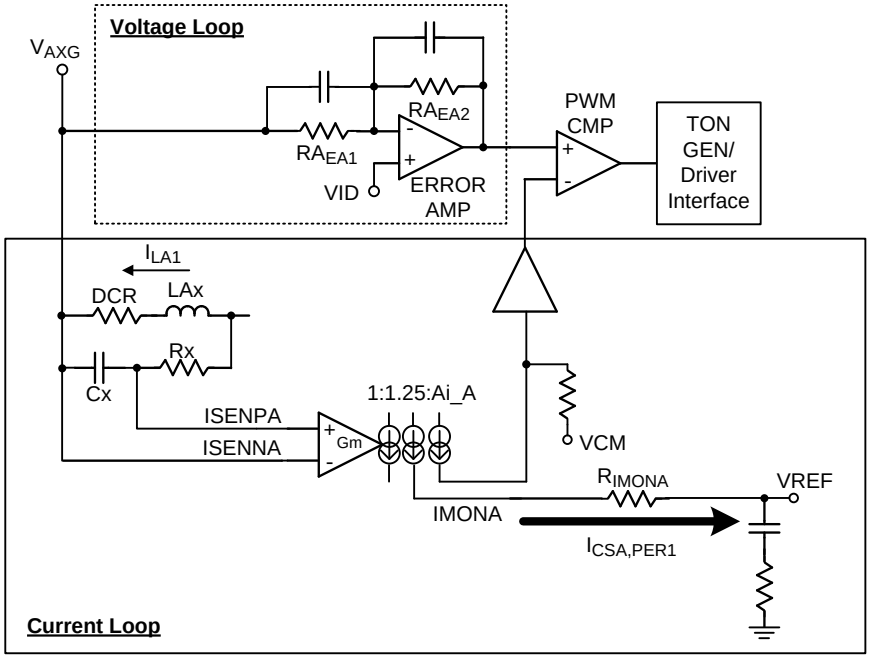

Figure 28. Voltage Loop and Current Loop for Loadline

Table 15. PIN-SETTING of Ai_A[4:3]

Ai_A[4:3]	Current Gain Setting
00	0.75
01	1.13
10	1.5
11	1.88

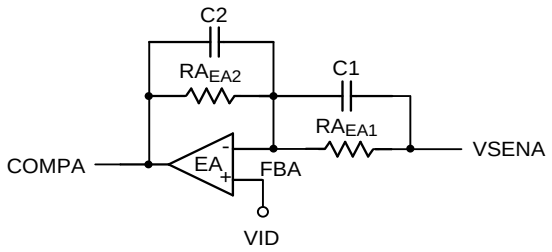

Figure 29. Type I Compensator

Compensator Design

The RT3628AE doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP^{TM} topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 29. For IMVP9.1 ACLL specification, it is recommended to adjust compensator according to load transient ring back level. Refer to the design tool for default compensator values.

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, VCCAXG_SENSE and VSSAXG_SENSE. The related connection is shown in Figure 30. The VID voltage (DAC) is referred to RGNDA to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

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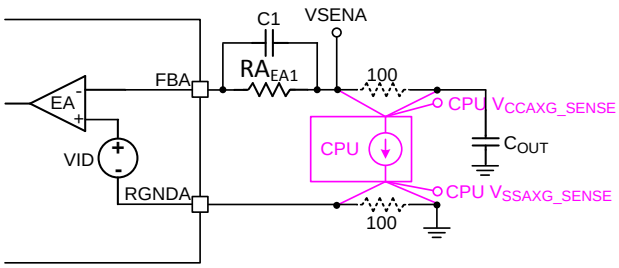

Figure 30. Remote Sensing Circuit

Switching Frequency Setting

The G-NAVP™ (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive T_{ON} (PWM) with input voltage (V_{IN}) for better line regulation. The T_{ON} is also adaptive to VID voltage. The adaptive T_{ON} is based on constant current ripple concept for better output voltage ripple size control. The adaptive T_{ON} is based on constant frequency concept for better efficiency performance. Figure 31 is the conceptual chart showing the relationships between switching frequency vs VID and current ripple vs VID. The RT3628AE provides a parameter setting of k_{TON_A} to design T_{ON} width. The k_{TON_A} is set by PIN-SETTING of KTON_A[3:1]. The related setting table is listed in Table 16.

The equations of T_{ON} with different VID table setting are listed as below (k_{TON_A} should be referred to Table 16)

For VID1 :

VID ≥ 0.9V,

$$T_{ON}=2.206\mu\times\frac{VID}{k_{TON\_A}\times(V_{IN}-0.9V)}+15ns$$

0.3V < VID < 0.9V,

$$T_{ON}=1.9854\mu\times\frac{1}{k_{TON\_A}\times(V_{IN}-VID)}+15ns$$

VID ≤ 0.3V,

$$T_{ON}=1.9854\mu\times\frac{1}{k_{TON\_A}\times(V_{IN}-0.3V)}+15ns$$

For VID2 :

VID ≥ 1.8V,

$$T_{ON}=2.206\mu\times\frac{VID}{k_{TON\_A}\times(V_{IN}-1.8V)}+15ns$$

0.3V < VID < 1.8V,

$$T_{ON}=1.9854\mu\times\frac{2}{k_{TON\_A}\times(V_{IN}-VID)}+15ns$$

VID ≤ 0.3V,

$$T_{ON}=1.9854\mu\times\frac{2}{k_{TON\_A}\times(V_{IN}-0.3V)}+15ns$$

Table 16. PIN-SETTING of KTON_A

KTON_A[3:1]	k_{TON_A}
000	0.82
001	0.91
010	1.00
011	1.09
100	1.18
101	1.27
110	1.36
111	1.55

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The switching frequency can be derived from T_{ON} as shown as below. The losses in the main power stage and driver characteristics are considered.

$$Freq=\frac{VID+\frac{I_{CC}}{N}\times(DCR+\frac{R_{ON_{LS,max}}}{n_{LS}}-N\times R_{LL})}{\left[V_{IN}+\frac{I_{CC}}{N}\times\left(\frac{R_{ON_{LS,max}}}{n_{LS}}-\frac{R_{ON_{HS,max}}}{n_{HS}}\right)\right]\times(T_{ON}-T_D+T_{ON,\,VAR})+\frac{I_{CC}}{N}\times\frac{R_{ON_{LS,max}}}{n_{LS}}\times T_D}$$

VID: VID voltage

V_{IN}: input voltage

I_{CC}: loading current

N: total phase number

$R_{ON_{HS,max}}$: maximum equivalent of the high-side RDS(ON)

n_{HS}: number of high-side MOSFETs

$R_{ON_{LS,max}}$: maximum equivalent of the low-side RDS(ON)

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

$T_{ON,\,VAR}$: on-time variation value

DCR: inductor DCR

R_{LL}: loadline setting (Ω).

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Although TON is designed for constant frequency target while VID ≥ 0.9V, the actual frequency is still impacted by main power stage's loss and driver dead time. The switching frequency rises as loading current increases. It's recommend to design the switching frequency based on the optimized efficiency and thermal performance at thermal design current (ICCTDC). For example, at ICC = ICCTDC, VID = 0.9V and VIN = 12V, the switching frequency is 400kHz in S-Line application. Then substitute these values into equations to get TON and relative k_{TON_A}.

Richtek provides a Microsoft Excel-based design tool to help design k_{TON_A} setting for the desired switching frequency at TDC.

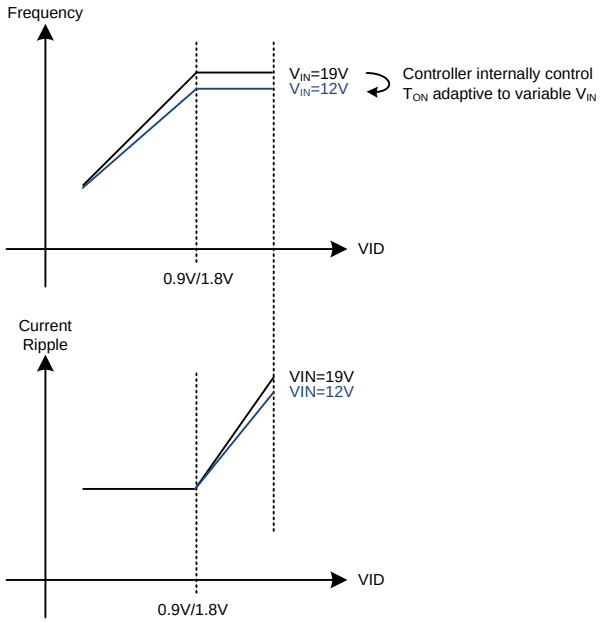

Figure 31. Switching Frequency and Current with Different VID

Anti-overshoot (ANTI-OVS)

The RT3628AE provides Anti-overshoot function to depress output voltage overshoot. Controller detects overshoot by signals relating to output voltage. The overshoot trigger level can be adjusted by I2C Reg0x7C[5:3]. The main detecting signal comes from COMPA. However, COMPA varies with compensation. Initial trigger level setting can be based on the following equation :

$$\Delta COMPA \times \frac{4}{3} = \Delta VSENA \times \frac{RA_{EA2}}{RA_{EA1}} \times \frac{4}{3}$$

>Antiovershoot Threshold of I2C Reg0x7C[5:3]

The final setting depends on the actual Error AMP compensator design and measurement.

While overshoot exceeds the setting trigger level, all PWMs keep in tri-state until the zero current is detected or VSENA back to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

ACLL Performance Enhancement

The RT3628AE provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. Controller detects COMPA signal and compares it with steady state. While VCOMPA variation exceeds a threshold, an additional positive offset will be applied to the output voltage. The threshold can be set through PIN-SETTING AR_TH_A[2:1], as listed in Table 17. The smaller index indicates the easier detection being triggered. The positive offset is related to the compensation. Figure 32 show undershoot suppression behavior. For different platform, the optimized setting is different. The final setting must be based on actual measurement.

Table 17. PIN-SETTING of Undershoot Suppression

AR_TH_A[2:1]	Adaptive RAMP Trigger level (mV)
00	Disable
01	125
00	175
01	225

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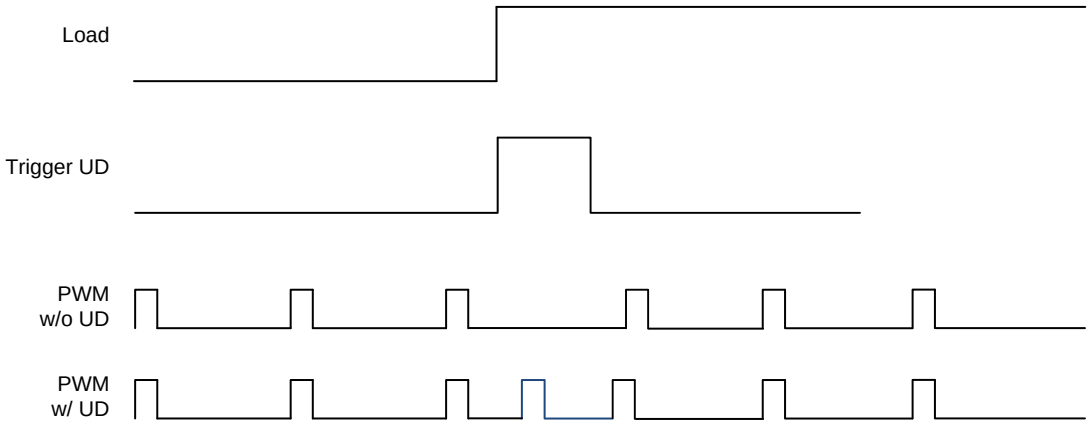

Figure 32. Undershoot Suppression Behavior in PS0/PS1

Over-current Protection (OCP)

The RT3628AE has sum OCP mechanisms.

Sum OCP

The threshold of sum OCP for PS0 is defined as

$$I_{SUM\_OC\_A,PS0}=K_{SOCPA}\times VIMONA_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{1.25}\times\frac{1}{R_{IMONA}}$$

PS1/2/3 sum OCP is defined as

$$I_{SUM\_OC\_A,nonPS0}=K_{SOCPA}\times VIMONA_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{1.25}\times\frac{1}{R_{IMONA}}$$

While $R_{IMONA,EQ}$ is designed exactly for

$$VIMONA_{ICCMAX}=\text{ICCMAX register value}\times\frac{DCR}{R_{INT.}}\times 1.25\times R_{IMONA},$$

ICCMAX register value=ICCMAX, and $VIMONA_{ICCMAX}=0.4V$

The KSOCPA is sum OCP ratio whose value is 0.6~1.6 and it is set by Pin Setting Function of TSENA & I2C register 0x73h[5:3]. Sum OCP threshold can be simplified as $I_{SUM\_OC\_A,PS0}=K_{SOCPA}\times ICCMAX$. Note that the modification of ICCMAX register value cannot change sum OCP threshold. While inductor current above sum OCP threshold lasts 20μs / 40μs(set by I2C register 0x73h[6].), controller de-asserts VR_READY and latches PWM in tri-state to turn off high-side and low-side power MOSFETs.

Sum OCP is masked during DVID period and 80us after VID settles. They are also masked while VID = 0V condition.

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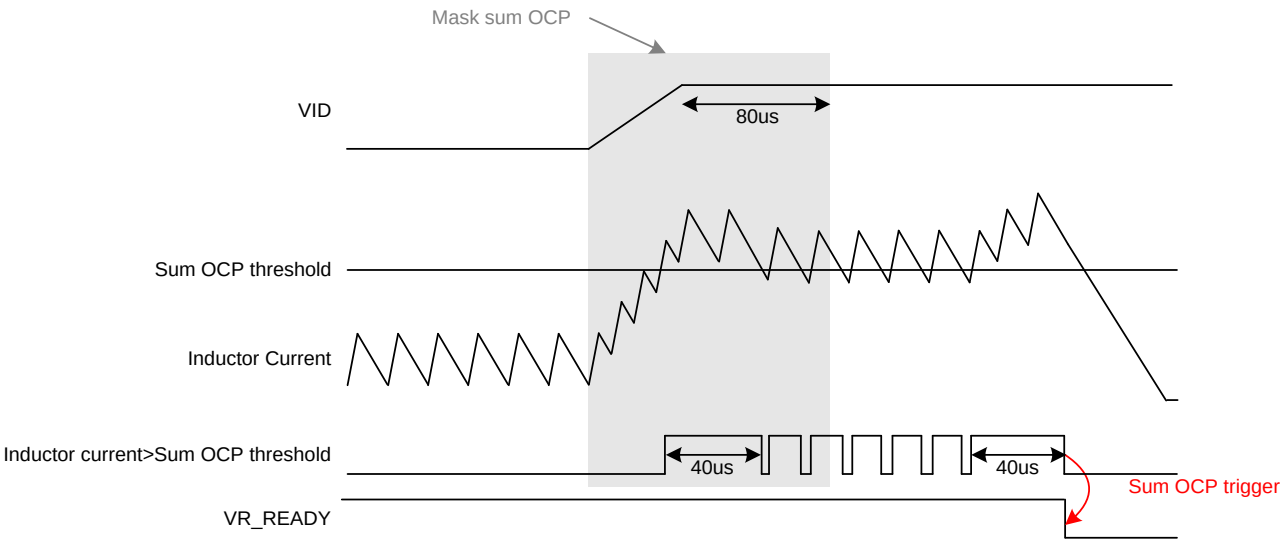

Figure 33. SUM OC Protection Mechanism

Over-Voltage Protection (OVP)

The OVP threshold is linked with to VID. The classification table is illustrated in Table 18. While VID = 0V, in case of VR internal setting mode, DACOFF or PS4, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, the OVP threshold is 2.45V or 2.65V which depends on VID table to allow not-fully-discharged VSEN. Otherwise, the OVP threshold is relative to VID and equals to VID+350mV with minimum limit = 1.35V. While VID ≤ 1V, the OVP threshold is limited at 1.35V.

The OV protection mechanism is illustrated in Figure 34. When OVP is triggered with 0.5μs filter time, controller de-asserts VR_READY and forces all PWMs low to turn on low-side power MOSFETs. The PWM remains low until the output voltage is pulled down below VID. After 60μs from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, the PWM is not allowed to turn on. Controller controls the PWM to be low or tri-state to pull down the output voltage along with VID.

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Table 18. Summary of Over Voltage Protection

VID Condition	OVP Threshold	Example	Protection Flag	Protection Action	Protection Reset
VID=0 (EN=L or VR internal setting mode or DACOFF or PS4)	OVP is masked.		VREF=1V		VCC/EN Toggle
DVID up period from 0V to 1st PWM pulse after VID settles	Threshold is set by 0x75h. Default is 2.45V or 2.65V which depends on VID table.			VR_READY latched low. The output voltage is pulled down to below SSOVP-0.35V and then ramps down to 0V.	
DVID period from non-zero VID	VID+350mV if VID > 1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.		VR_READY latched low. The output voltage is pulled down to below VID and then ramps down to 0V.	
VID≠0	VID+350mV if VID >1.0V, 1.35V if VID ≤ 1.0V	VID = 1.2V, OVP threshold = 1.55V. VID = 0.9V, OVP threshold = 1.35V.			

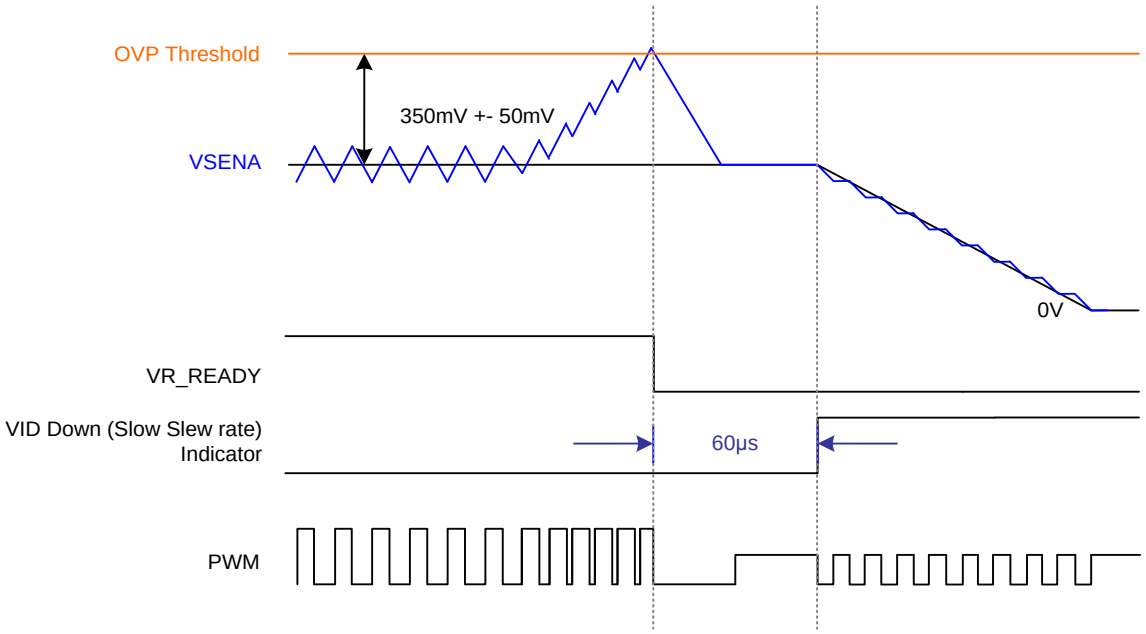

Figure 34. Over Voltage Protection Mechanism

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Under-Voltage Protection

When the output voltage is lower than VID-650mV with 3μs filter time, the UVP is triggered and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. The UVP is masked during DVID period and 80us after VID settles. The mechanism is illustrated in Figure 35.

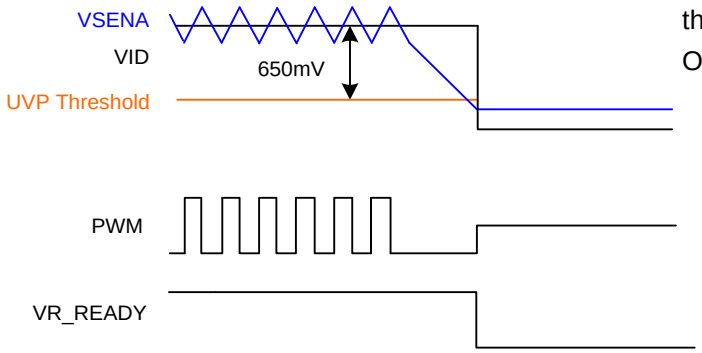

Figure 35. Under Voltage Mechanism

All protections are reset only by VCC/EN toggle. The UVP and OCP protections are listed in Table 19. Note that the real filter time also depends on the magnitude of detected signal. The signal magnitude will affect analog comparator's overdrive voltage and output slew rate. For user friendly operation, the RT3628AE provides protection flag to promptly determine which kind of protections is triggered. As protection happens, the VREF is pulled to 1V/1.5625V/2V for OVP/UVP/SUM_OCP respectively.

Table 19. Summary of UVP and OCP Protection

Protection Type	Protection Threshold	Protection Flag	Protection Action	DVID mask time	Protection Reset
Sum OCP for PS0	$I_{SUM\_OC\_A,PS0}=K_{SOCPA}\times VIMONA_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMONA}}$	VREF=2V	PWM tri-state, VR_READY latched low	DVID+ 80μs	VCC/EN Toggle
Sum OCP for non PS0	$I_{SUM\_OC\_A,nonPS0}=K_{SOCPA}\times VIMONA_{ICCMAX}\times\frac{R_{INT.}}{DCR}\times\frac{1}{R_{IMONA}}$	VREF=2V			
UVP	VID-650mV	VREF=1.5625 V			

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Current Reporting of AUX

Current Sense

AUX rail support DCR and Smart Power Stage (SPS) current sensing report. Figure X1 shows the DCR application diagram. As illustrated in Figure 36, an external low-pass filter R_{AUX1} , R_{AUX2} and C_{AUX} reconstruct the current signal, where R_{AX2} is necessary for DCR temperature compensation. The low-pass filter time constant $(R_{AUX1}//R_{AUX2})\times C_{AUX}$ should match time constant $\frac{L_{AUX}}{DCR}$ of inductance and DCR. If RC network time constant matched inductor time constant, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant, V_{AUX} waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant, V_{AUX} waveform sags to create an undershooting to fail the specification.

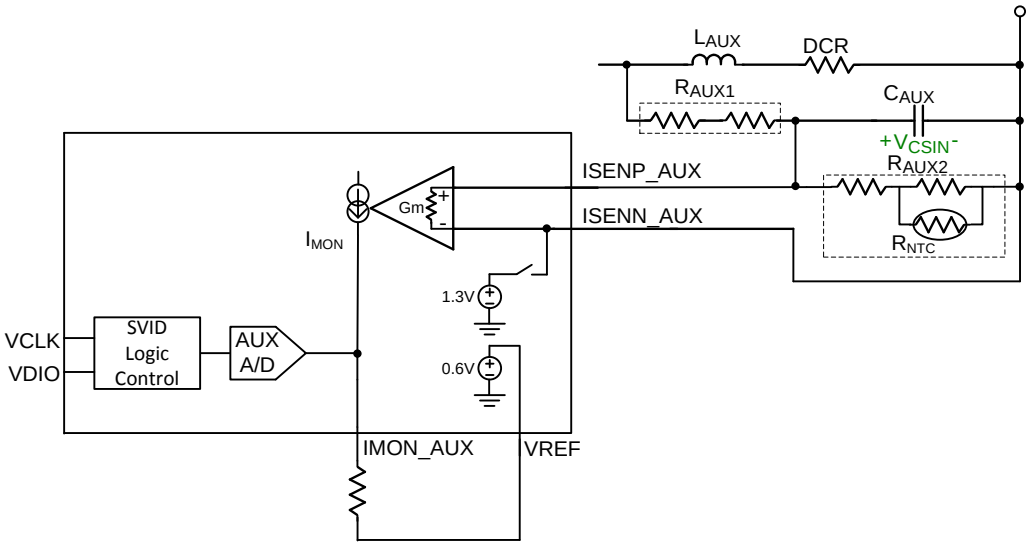

Figure 36. AUX Rail use DCR Current Sense

$$I_{CSA,PERx}=\frac{V_{CSIN}}{R_{INT.}}=\frac{I_{LAx}\times DCR}{R_{INT.}}\times\frac{R_{AUX2}}{R_{AUX1}+R_{AUX2}}$$

The current signal $I_{CSA,PERx}$ is mirrored for current reporting. The mirrored current to IMON_AUX pin is 1.25 time of $I_{CSA,PER}$

($I_{IMONA}=A_{MIRROR}\times I_{CSA,PERx}$, $A_{MIRROR}=1.25$)

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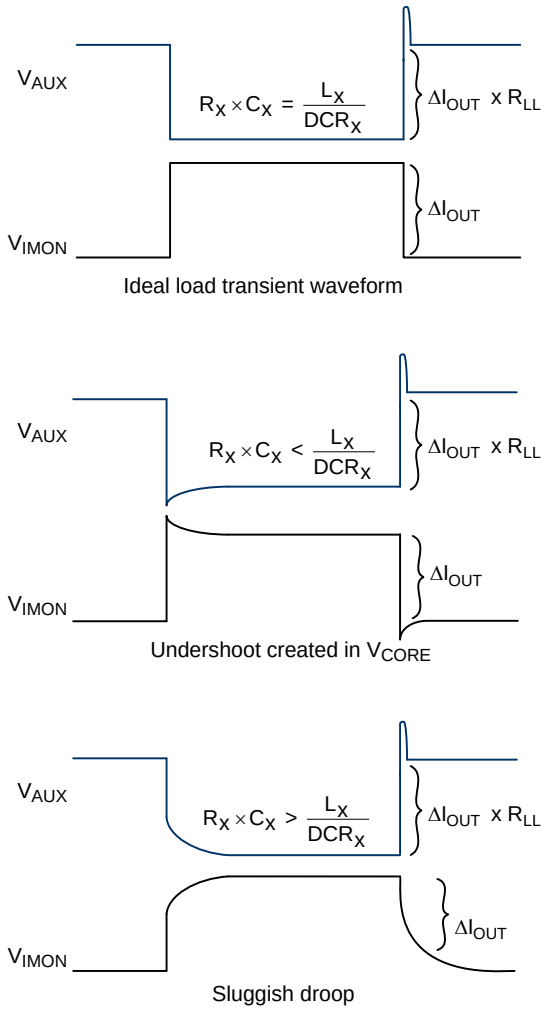

Figure 37. All Kinds of RC Network Time Constant

Total Current Sense/ICCMAX Setting/Current Monitoring

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The NTC resistor is designed within DCR current sense network. It is suggested to be placed near the inductor of the first phase. Current signals are gathered to IMON_AUX pin and converted to a voltage signal V_{IMON_AUX} by R_{IMON_AUX} based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as VVREF) while normal operation. The relationship between V_{IMONA} and inductor current I_{L_AUX} is:

$$V_{IMON\_AUX}-V_{VREF}=(I_{L\_AUX})\times\frac{DCR}{R_{INT.}}\times\frac{R_{AUX2}}{R_{AUX1}+R_{AUX2}}$$

$$\times 1.25\times R_{IMON\_AUX}$$

$V_{IMON\_AUX}-V_{VREF}$ is proportional to output current. $V_{IMON\_AUX}-V_{VREF}$ is used for output current reporting. $V_{IMON\_AUX}-V_{VREF}$ is averaged by analog low-pass filter and then outputs to 8-bit ADC. The digitized reporting value is scaled such that FFh = ICCMAX, and the ICCMAX is set by SET1, R_{IMON_AUX} can be designed through above equation, where $V_{IMON\_AUX} - V_{VREF}$ = 1.6V while I_{L_AUX} = ICCMAX register value.

Figure 38 shows the SPS(current type) application diagram. While ISENP_AUX is connected to 5V, ISENN_AUX will by pass a 1.3V reference voltage for SPS, and the SPS output current is directly injected to the IMON_AUX pin. The relationship between V_{IMONA} and inductor current I_{L_AUX} is:

$$V_{IMON\_AUX}-V_{REFIN}=(I_{L\_AUX})\times SPS\_gain\times R_{IMON\_AUX}$$

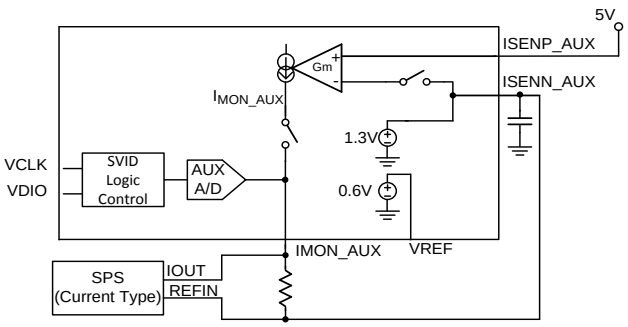

Figure 38. AUX Rail Use SPS Current Sense

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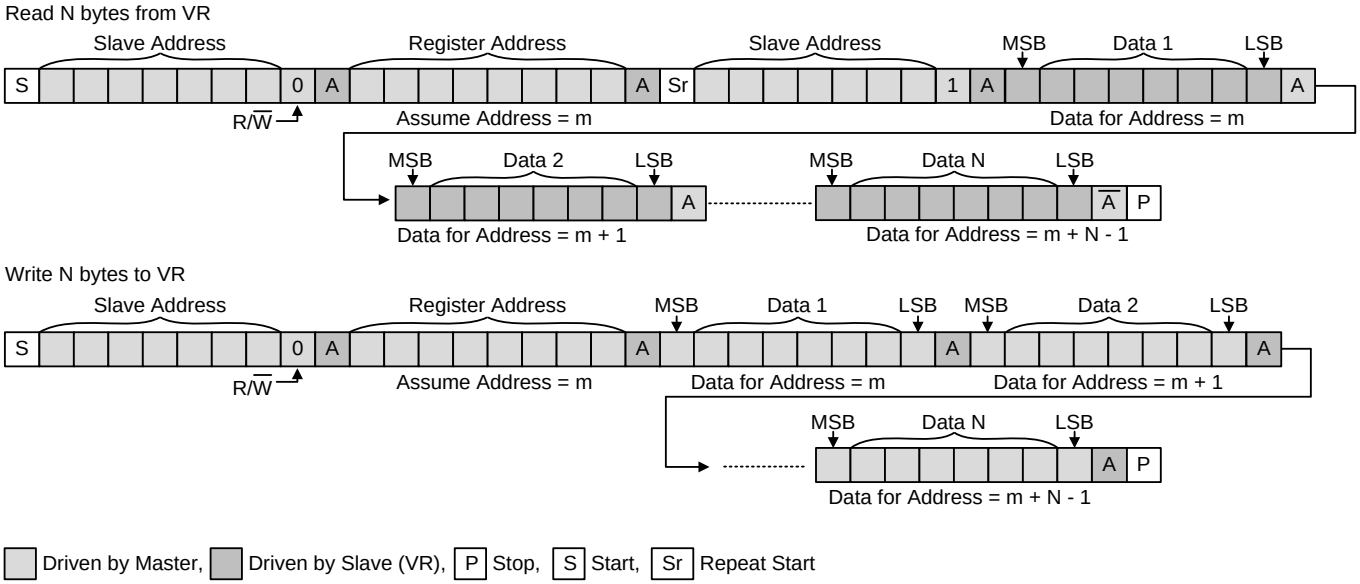
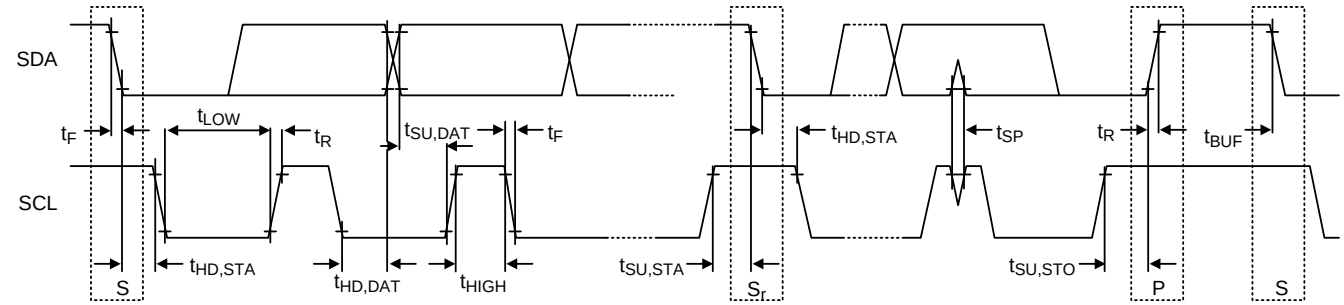
I²C Interface

The I²C slave address = 0x20h or 0x21h by SET1 pin setting.

This I²C does not have a stretch function.

The I²C interface supports standard slave mode (100 kbps), and fast mode (400kbps). The write or read bit stream (N>1) is shown below :





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Register Map

Register Address	NAME	Type	Register Reset
0x00h	CBG1_CORE	RW	0x04h
0x01h	CBG2_CORE	RW	0x04h
0x02h	CBG3_CORE	RW	0x04h
0x03h	CBG4_CORE	RW	0x04h
0x04h	CBG5_CORE	RW	0x04h
0x05h	CBG6_CORE	RW	0x04h
0x06h	CBC7_CORE	RW	0x04h
0x07h	CBC8_CORE	RW	0x04h
0x22h	LL_SEL_CORE	RW	0x07h
0x23h	VOFS_CORE	RW	0x00h
0x24h	EN_VFIX_CORE	RW	0x00h
0x25h	VFIX_LSB_CORE	RW	0x83h(VID1) 0xA1h(VID2))
0x26h	VFIX_MSB_CORE	RW	0x00h
0x27h	EN_PRT_CORE	RW	--
0x28h	PRT_FLAG_CORE	R	0x00h
0x2Ah	FORCE_PS0_CORE	RW	0x00h
0x30h	ILOAD_RPT_CORE	R	--
0x31h	PSYS_RPT	R	--
0x32h	TEMP_RPT_CORE	R	--
0x42h	LL_SEL_AXG	RW	0x07h
0x43h	VOFS_AXG	RW	0x00h
0x44h	EN_VFIX_AXG	RW	0x00h
0x45h	VFIX_LSB_AXG	RW	0x83h(VID1) 0xA1h(VID2)
0x46h	VFIX_MSB_AXG	RW	0x00h
0x47h	EN_PRT_AXG	RW	--
0x48h	PRT_FLAG_AXG	R	0x00h
0x4Ah	FORCE_PS0_AXG	RW	0x00h
0x50h	CORE_ACLL_MISC1	RW	0x06h
0x51h	CORE_ACLL_ MISC2	RW	0xE3h
0x52h	CORE_ACLL_ MISC3	RW	0x5Bh
0x53h	CORE_ACLL_ MISC4	RW	0x91h
0x54h	CORE_ACLL_ MISC5	RW	0xCAh
0x55h	CORE_ACLL_ MISC6	RW	0x1Fh
0x60h	AXG _ACLL_MISC1	RW	0x1Fh
0x61h	AXG _ACLL_MISC2	RW	0x79h
0x62h	AXG _ACLL_MISC3	RW	0xC7
0x63h	AXG _ACLL_MISC4	RW	0x11h
0x70h	ILOAD_RPT_AXG	R	--
0x72h	TEMP_RPT_AXG	R	--
0x73h	SUMOCP_DLY	RW	0xF6h
0x75h	OVP_SS	RW	0x00h

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Register Address	NAME	Type	Register Reset
0x76h	WDR	RW	0x00h
0x77h	WDR_ST	R	--
0x78h	ILOAD_RPT_Ratio	RW	0x00h
0x79h	ILOAD_RPT_AUX	R	--
0x7Ah	CORE_ZCD_TH	RW	--
0x7Bh	AXG_ZCD_TH	RW	--
0x7Ch	ANTIOVS_TH	RW	0x3Fh
0x80h	MISC1	RW	--
0x81h	FASTV_VRHOT_ICCMAX_AUX	RW	--
0x82h	AR_TH_CORE_ICCMAX_AXG	RW	--
0x83h	EN_DBLR_KTON_AXG	RW	--
0x84h	DAC_SEL_ICCMAX	RW	--
0x85h	MISC2	RW	--
0x86h	MISC3	RW	--
0x87h	SUMOCP_ZCD_TH_AXG	RW	--

Register Address: 0x00h
Description: Adjustment phase1 current balance gain of CORE rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG1_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Register Address: 0x01h
Description: Adjustment phase2 current balance gain of CORE rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG2_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

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Register Address: 0x02h **Description**: Adjustment phase3 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG3_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Register Address: 0x03h **Description**: Adjustment phase4 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG4_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Register Address: 0x04h **Description**: Adjustment phase5 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG5_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

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Register Address: 0x05h **Description**: Adjustment phase6 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG6_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Register Address: 0x06h **Description**: Adjustment phase7 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG77_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

Register Address: 0x07h **Description**: Adjustment phase8 current balance gain of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG8_CORE							
Reset Value	0x04h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	CBG	[2:0] = 000 : 69.2%, [2:0] = 001 : 76.9%, [2:0] = 010 : 84.6%, [2:0] = 011 : 92.3%, [2:0] = 100 : 100% (default), [2:0] = 101 : 107.69%, [2:0] = 110 : 115.38%, [2:0] = 111 : 123.08%

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Register Address: 0x22h **Description**: Selection load-line of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LL_SEL_CORE							
Reset Value	0x07h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	SEL_LL	[2:0] = 000 : 0% (0mΩ LL), [2:0] = 001 : 12.5%, [2:0] = 010 : 25%, [2:0] = 011 : 37.5%, [2:0] = 100 : 50%, [2:0] = 101 : 62.5%, [2:0] = 110 : 75%, [2:0] = 111 : 100%(default)

Register Address: 0x23h **Description**: Setting offset voltage of CORE rail. For VID1 the final voltage limiting range 0.25V ~ 2.17V. (i.e. 0.25V ≤ VID setting ± SVID offset voltage ± I^2C offset voltage ≤ 2.17V) For VID2 the final voltage limiting range 0.2V~3.04V. The offset slew rate is 1/2 of the fast slew rate. While setting voltage offset, the VR should return to power state PS0. After VSEN settles at the target offset voltage, the power state(PS) goes back to the original PS. If CPU sends SetPS1/2/3 command, the controller follows PS and the voltage offset still exists. If CPU sends SetVID off code command (VID setting ± SVID offset voltage ± I2C offset voltage), the controller sets output voltage to 0V.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOFS_CORE							
Reset Value	0x00h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OFS	[7:0] = 00h : no offset [7] : sign bit (as part of two's complement) [6:0] : 5mV/step (DAC_SEL=0) or 10mV/step (DAC_SEL=1) [e.g.] 0000000**1** = current VID + (**1** x VID step) 0000000**11** = current VID + (**3** x VID steps) 1**1111111** = current VID - (**1** x VID step)

Register Address: 0x24h **Description**: Enable/Disable fixed VID mode of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_VFIX_CORE							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved
[0]	EN_VFIX	[0] = 0 : Disable Fixed VID Mode [0] = 1 : Enable Fixed VID Mode

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Register Address: 0x25h
Description: 9 bit fixed VID (Reg. 0x26h + Reg. 0x25h). Set voltage in fixed VID mode of CORE rail. In fixed VID mode, VR skips SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving SetVID command, while the VR output voltage stays at the fixed VID.) While Fixed VID is enabled, VR doesn't act for I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_LSB_CORE							
Reset Value	0x83h(VID1); 0xA1h(VID2)							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:0]	VFIX_LSB	Voltage of fixed VID mode = 0.0V when receives an off code (VFIX_MSB [0]=00h + VFIX_LSB[7:0]=00h) DAC_SEL=0, Voltage of fixed VID mode = 0.245V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. DAC_SEL=1, Voltage of fixed VID mode = 0.19V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V.

Register Address: 0x26h
Description: 9 bit fixed VID (Reg. 0x26h + Reg. 0x25h). Set voltage in fixed VID mode of CORE rail. In fixed VID mode, VR skips SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving SetVID command, while the VR output voltage stays at the fixed VID.) While Fixed VID is enabled, VR doesn't act for I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MSB_CORE							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	Name	Description
[7:1]	Reserved	Reserved
[0]	VFIX_MSB	Voltage of fixed VID mode = 0.0V when receives an off code (VFIX_MSB [0]=00h + VFIX_LSB[7:0]=00h) DAC_SEL=0, Voltage of fixed VID mode = 0.245V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. DAC_SEL=1, Voltage of fixed VID mode = 0.19V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V.

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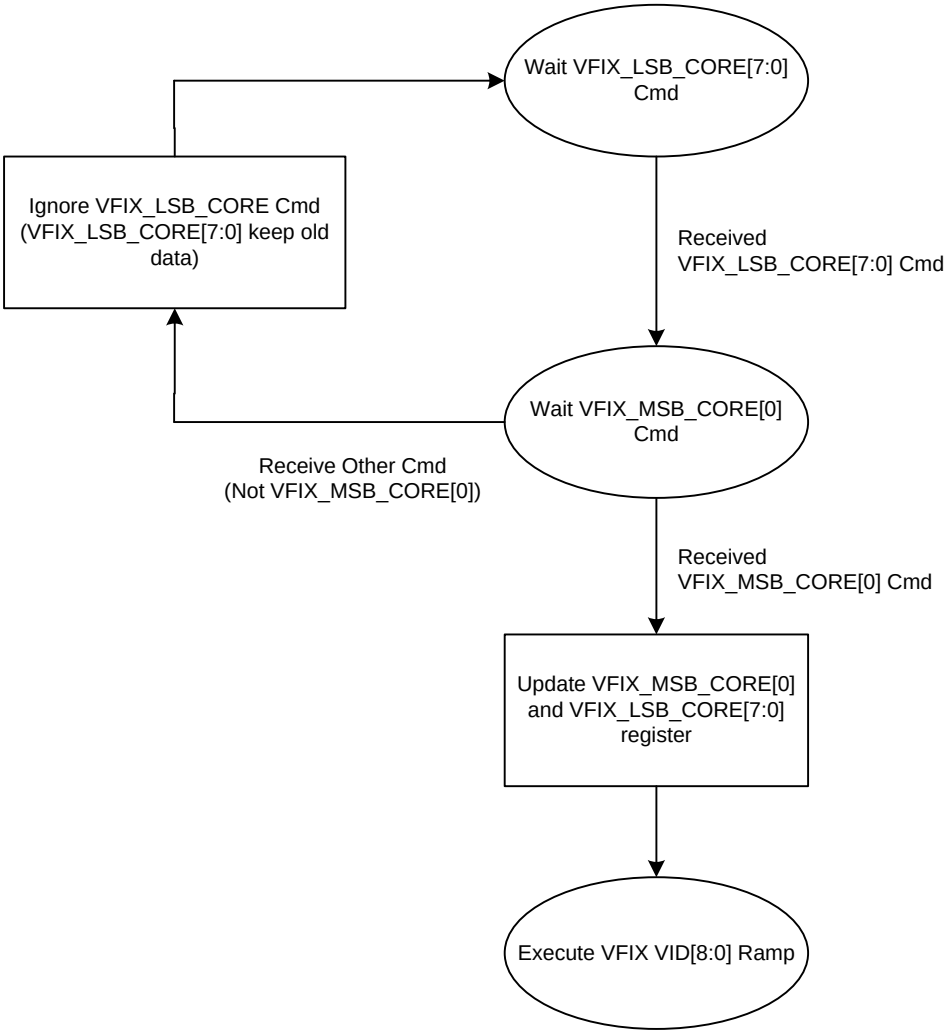

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Register Address: 0x27h **Description**: Enable/Disable protection function of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_PRT_CORE							
Reset Value	--							
Read/Write	R	RW	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved
[6]	EN_Non-PS0_OC_SUM	[6] = 0 : Disable PS1/2/3 sum OC protection [6] = 1 : Enable PS1/2/3 sum OC protection (default)
[5:4]	Reserved	Reserved
[3]	EN_OC_SUM	[3] = 0 : Disable sum OC protection [3] = 1 : Enable sum OC protection (default)
[2]	EN_NV	[2] = 0 : Disable NV protection [2] = 1 : Enable NV protection (default)
[1]	EN_UV	[1] = 0 : Disable UV protection [1] = 1 : Enable UV protection (default)
[0]	EN_OV	[0] = 0 : Disable OV protection [0] = 1 : Enable OV protection (default)

Register Address: 0x28h **Description**: Protection indicator of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRT_FLAG_CORE							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:4]	Reserved	Reserved
[3]	OC_SUM	[3] = 0 : No occurrence sum OCP [3] = 1 : Occurrence sum OCP
[2]	Reserved	Reserved
[1]	UV	[1] = 0 : No occurrence UVP [1] = 1 : Occurrence UVP
[0]	OV	[0] = 0 : No occurrence OVP [0] = 1 : Occurrence OVP

Register Address: 0x2Ah **Description:** Enable/Disable force PS0 function of CORE rail, and the rail still operates in PS0 when the SetPS1/2/3 command is received.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Force_PS0_CORE							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved bits
[0]	Force_PS0	[0] = 0 : Disable [0] = 1 : Enable (Fixed in PS0)

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Register Address: 0x30h **Description:** Output current reporting of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ILOAD_RPT_CORE							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	ILOAD_RPT	Output current reporting of CORE rail.

Register Address: 0x31h **Description:** PSYS reporting.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	PSYS_RPT	PSYS reporting.

Register Address: 0x32h **Description**: Temperature reporting of CORE rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TEMP_RPT_CORE							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	TEMP_RPT	$V_{THERMAL}$ = TEMP_RPT[7:0] x 6.25mV

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Table 20. $V_{THERMAL}$ vs Temperature (based on the R_{NTC} = 100k/Beta = 4250K)

Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)	Temperature (°C)	$V_{THERMAL}$ (V)
61	1.133	81	0.814	101	0.591	121	0.453
62	1.116	82	0.800	102	0.582	122	0.447
63	1.098	83	0.787	103	0.574	123	0.442
64	1.080	84	0.774	104	0.566	124	0.437
65	1.063	85	0.761	105	0.558	125	0.432
66	1.046	86	0.749	106	0.550	126	0.428
67	1.029	87	0.737	107	0.542	127	0.423
68	1.012	88	0.725	108	0.534	128	0.419
69	0.995	89	0.713	109	0.527	129	0.414
70	0.979	90	0.702	110	0.520	130	0.410
71	0.963	91	0.690	111	0.513		
72	0.947	92	0.679	112	0.506		
73	0.931	93	0.669	113	0.500		
74	0.916	94	0.658	114	0.493		
75	0.900	95	0.648	115	0.487		
76	0.885	96	0.638	116	0.481		
77	0.871	97	0.628	117	0.475		
78	0.856	98	0.618	118	0.469		
79	0.842	99	0.609	119	0.463		
80	0.828	100	0.600	120	0.458		

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Register Address: 0x42h **Description**: Selection load-line of AXG rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LL_SEL_AXG							
Reset Value	0x07h							
Read/Write	R	R	R	R	R	RW	RW	RW

Bits	**Name**	**Description**
[7:3]	Reserved	Reserved bits
[2:0]	SEL_LL	[2:0] = 000 : 0% (0mΩ LL), [2:0] = 001 : 12.5%, [2:0] = 010 : 25%, [2:0] = 011 : 37.5%, [2:0] = 100 : 50%, [2:0] = 101 : 62.5%, [2:0] = 110 : 75%, [2:0] = 111 : 100%(default)

Register Address: 0x43h

Description: Set offset voltage of AXG rail. For VID1 the final voltage limiting range 0.25V ~ 2.17V. (i.e. 0.25V ≤ VID setting ± SVID offset voltage ± I^2C offset voltage ≤ 2.17V) For VID2 the final voltage limiting range 0.2V~3.04V. The offset slew rate is 1/2 of the fast slew rate. While setting voltage offset, the VR should return to power state PS0. After VSEN settles at the target offset voltage, the power state(PS) goes back to the original PS. If CPU sends SetPS1/2/3 command, the controller follows PS and the voltage offset still exists. If CPU sends SetVID off code command (VID setting ± SVID offset voltage ± I2C offset voltage), the controller sets output voltage to 0V.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOFS_AXG							
Reset Value	0x00h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:0]	OFS	[7:0] = 00h : no offset [7] : sign bit (as part of two's complement) [6:0] : 5mV/step(DAC_SEL=0) or 10mV/step(DAC_SEL=1) [e.g.] 0000000**1** = current VID + (**1** x VID step) 000000**11** = current VID + (**3** x VID steps) 1**1111111** = current VID - (**1** x VID step)

Register Address: 0x44h **Description**: Enable/Disable fixed VID mode of AXG rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_VFIX_AXG							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	**Name**	**Description**
[7:1]	Reserved	Reserved
[0]	EN_VFIX	[0] = 0 : Disable Fixed VID Mode [0] = 1 : Enable Fixed VID Mode

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Register Address: 0x45h
Description: 9 bit fixed VID (Reg. 0x46h + Reg. 0x45h). Set voltage in fixed VID mode of AXG rail. In fixed VID mode, VR skips SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving SetVID command, while the VR output voltage stays at the fixed VID.) While Fixed VID is enabled, VR doesn't act for I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_LSB_AXG							
Reset Value	0x83h(VID1); 0xA1(VID2)							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7:0]	VFIX_LSB	Voltage of fixed VID mode = 0.0V when receives an off code (VFIX_MSB [0]=00h + VFIX_LSB[7:0]=00h) DAC_SEL=0, Voltage of fixed VID mode = 0.245V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. DAC_SEL=1, Voltage of fixed VID mode = 0.19V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V.

Register Address: 0x46h
Description: 9 bit fixed VID (Reg. 0x46h + Reg. 0x45h). Set voltage in fixed VID mode of AXG rail. In fixed VID mode, VR skips SetVID/SetPS command. (VR has no actions but still asserts $\overline{\text{ALERT}}$ immediately after receiving SetVID command, while the VR output voltage stays at the fixed VID.) While Fixed VID is enabled, VR doesn't act for I^2C voltage offset as well. After disabling fixed VID mode, VID returns to the last SetVID target and last power state. When entering/exiting fixed VID mode, VID slew rate is 1/2 of the fast slew rate.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MSB_AXG							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	Name	Description
[7:1]	Reserved	Reserved
[0]	VFIX_MSB	Voltage of fixed VID mode = 0.0V when receives an off code (VFIX_MSB [0]=00h + VFIX_LSB[7:0]=00h) DAC_SEL=0, Voltage of fixed VID mode = 0.245V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 5mV, (VID1), voltage range from 0.25V to 2.17V. DAC_SEL=1, Voltage of fixed VID mode = 0.19V + (VFIX_MSB [0]+VFIX_LSB[7:0]) x 10mV, (VID2), voltage range from 0.2V to 3.04V.

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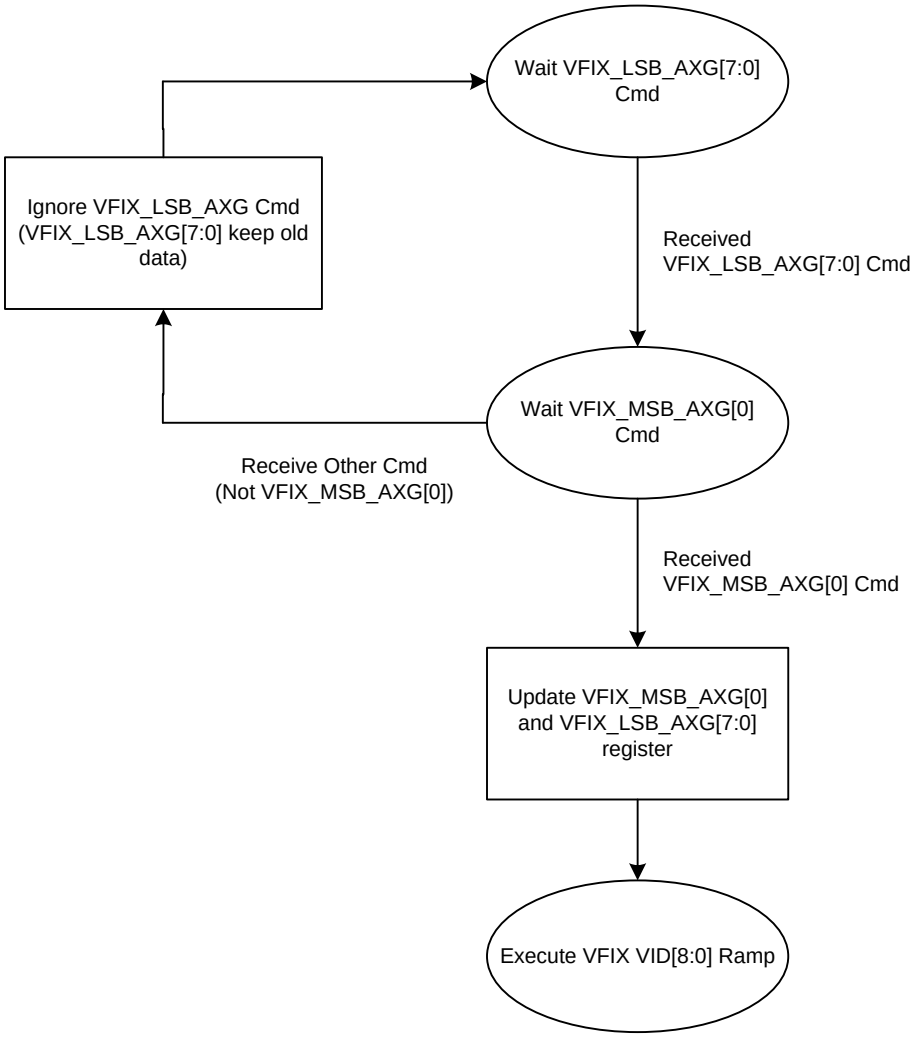

Register Address: 0x47h
Description: Enable/Disable protection function of AXG rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_PRT_AXG							
Reset Value	--							
Read/Write	R	RW	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved
[6]	Reserved	Reserved
[5:4]	Reserved	Reserved
[3]	EN_OC_SUM	[3] = 0 : Disable sum OC protection [3] = 1 : Enable sum OC protection (default)
[2]	EN_NV	[2] = 0 : Disable NV protection [2] = 1 : Enable NV protection (default)
[1]	EN_UV	[1] = 0 : Disable UV protection [1] = 1 : Enable UV protection (default)
[0]	EN_OV	[0] = 0 : Disable OV protection [0] = 1 : Enable OV protection (default)

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Register Address: 0x48h
Description: Protection indicator of AXG rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRT_FLAG_AXG							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	R

Bits	Name	Description
[7:4]	Reserved	Reserved
[3]	OC_SUM	[3] = 0 : No occurrence sum OCP [3] = 1 : Occurrence sum OCP
[2]	Reserved	Reserved
[1]	UV	[1] = 0 : No occurrence UVP [1] = 1 : Occurrence UVP
[0]	OV	[0] = 0 : No occurrence OVP [0] = 1 : Occurrence OVP

Register Address: 0x4Ah
Description: Enable/Disable force PS0 function of AXG rail, and the rail still operates in PS0 when the SetPS1/2/3 command is received.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Force_PS0_AXG							
Reset Value	0x00h							
Read/Write	R	R	R	R	R	R	R	RW

Bits	Name	Description
[7:1]	Reserved	Reserved bits
[0]	Force_PS0	[0] = 0 : Disable [0] = 1 : Enable (Fixed in PS0)

Register Address: 0x50h
Description: Selection kind of QR in PS0 or PS1 for CORE rail, setting fixed QR width in PS0 or PS1 for CORE rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC1							
Reset Value	0x06h							
Read/Write	R	RW	RW	RW	R	RW	RW	RW

Bits	Name	Description
[7]	Reserved	Reserved bit
[6]	Reserved	Reserved bit
[5:4]	Reserved	Reserved bit
[3]	Reserved	Reserved bit
[2]	ADPTV_FIX_QR_PS0	Selection kind of QR in PS0 for CORE rail [2] = 0 : Fixed QR [2] = 1 : Adaptive-QR (AQR)
[1:0]	FIX_QR_WD_PS0	Setting fixed QR width in PS0 for CORE rail [1:0] = 00 : 0.5 x Ton, [1:0] = 01 : 0.75 x Ton, [1:0] = 10 : 1.0 x Ton, [1:0] = 11 : 1.25 x Ton

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Register Address: 0x51h **Description**: Setting the extend Ton width and shrink Ton in PS1 for CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC2							
Reset Value	0xE3h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	EXTD_Ton_WD	Extend Ton width for CORE rail [7] = 0 : Disable [7] = 1 : Enable
[6]	HFACLL_STON_PS1	PWM behavior will shrink Ton and QR while ACLL frequency > STON_FREQ_PS1[5:4] for CORE rail [6] = 0 : Disable [6] = 1 : Enable
[5:4]	STON_FREQ_PS1	Select the ACLL frequency to start shrinking TON and QR in PS1 for CORE rail [5:4] = 00 : 200kHz, [5:4] = 01 : 300kHz, [5:4] = 10 : 400kHz, [5:4] = 11 : 500kHz
[3:2]	SEL_EXTD _Ton_WD	Selection extend Ton width for CORE rail [3:2] = 00 : 2.66 x Ton, [3:2] = 01 : 2.0 x Ton, [3:2] = 10 : 1.6 x Ton, [3:2] = 11 : 1.33 x Ton
[1:0]	INC_TON_TH	Setting increase Ton threshold for CORE rail [1:0] = 00 : 2.4V + 150mV, [1:0] = 01 : 2.4V + 200mV, [1:0] = 10 : 2.4V + 250mV, [1:0] = 11 : 2.4V + 300mV

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Register Address: 0x52h
Description: Set lift VID amount while QR/ RAMP_AUX be triggered for CORE rail. Set lift VID be pulled down time for QR/ RAMP_AUX be triggered for CORE rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC3							
Reset Value	0x5Bh							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	QR_LIFT_VID_PS0	The QR be triggered will lift VID in PS0 for CORE rail [7] = 0 : Disable [7] = 1 : Enable
[6]	QR_LIFT_VID_PS1	The QR be triggered will lift VID in PS1 for CORE rail [6] = 0 : Disable [6] = 1 : Enable
[5]	ADAPTIVE_RAMP _LIFT_VID_PS0	The ADAPTIVE_RAMP be triggered will lift VID in PS0 for CORE rail [5] = 0 : Disable [5] = 1 : Enable
[4]	ADAPTIVE_RAMP _LIFT_VID_PS1	The ADAPTIVE_RAMP be triggered will lift VID in PS1 for CORE rail [4] = 0 : Disable [4] = 1 : Enable
[3]	QR_LIFT_FAST_DOWN	Selection lift VID be pulled down time for QR be triggered [3] = 0 : 150us [3] = 1 : 40us
[2]	ADAPTIVE_RAMP _LIFT_FAST_DOWN	Selection lift VID be pulled down time for RAMP_AUX be triggered [2] = 0 : 150us [2] = 1 : 40us
[1]	QR_LIFT_VID	Selection lift VID amount while QR be triggered [1] = 0 : 5mV [1] = 1 : 10mV
[0]	ADAPTIVE_RAMP_LIFT_VID	Selection lift VID amount while RAMP_AUX be triggered [0] = 0 : 5mV [0] = 1 : 10mV

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Register Address: 0x53h **Description**: Set lift LPF while QR/ RAMP_AUX be triggered in PS0/1 for CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC4							
Reset Value	0x91h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	QR_LIFT_LPF_PS0	The QR be triggered will lift LPF in PS0 for CORE rail [7] = 0 : Disable [7] = 1 : Enable
[6]	QR_LIFT_LPF_PS1	The QR be triggered will lift LPF in PS1 for CORE rail [6] = 0 : Disable [6] = 1 : Enable
[5]	ADAPTIVE_RAMP_LIFT_LPF_PS0	The ADAPTIVE_RAMP be triggered will lift LPF in PS0 for CORE rail [5] = 0 : Disable [5] = 1 : Enable
[4]	ADAPTIVE_RAMP_LIFT_LPF_PS1	The ADAPTIVE_RAMP be triggered will lift LPF in PS1 for CORE rail [4] = 0 : Disable [4] = 1 : Enable
[3]	Reserved	Reserved bit
[2]	LF_LIFT_LPF_PS0	The QR or RAMP_AUX be triggered will lift LPF 10us in PS0 for CORE rail in PS0 for CORE rail [2] = 0 : Disable [2] = 1 : Enable
[1]	Reserved	Reserved bit
[0]	LF_LIFT_LPF_PS1	The QR or RAMP_AUX be triggered will lift LPF 10us in PS1 for CORE rail [0] = 0 : Disable [0] = 1 : Enable

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Register Address: 0x54h **Description**: Selection to shrink/disable QR at high frequency ACLL for CORE rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC5							
Reset Value	0xCAh							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	HF_ACLL_DISA_QR	To disable QR at high frequency ACLL, frequency can be set by HF_ACLL_DISA_QR_SEL[6:4] for CORE rail [7] = 0 : Disable [7] = 1 : Enable
[6:4]	HF_ACLL_DISA_QR_SEL	Selection to disable QR frequency at high frequency ACLL for CORE rail [6:4] = 000 : 500kHz, [6:4] = 001 : 550kHz, [6:4] = 010 : 600kHz, [6:4] = 011 : 650kHz, [6:4] = 100 : 700kHz, [6:4] = 101 : 750kHz, [6:4] = 110 : 800kHz, [6:4] = 111 : 850kHz
[3]	HF_ACLL_SQR	To shrink QR at high frequency ACLL, frequency can be set by HF_ACLL_SQR_SEL[2:0] for CORE rail [3] = 0 : Disable [3] = 1 : Enable
[2:0]	HF_ACLL_SQR_SEL	Selection to shrink QR frequency at high frequency ACLL for CORE rail [2:0] = 000 : 200kHz, [2:0] = 001 : 250kHz, [2:0] = 010 : 300kHz, [2:0] = 011 : 350kHz, [2:0] = 100 : 400kHz, [2:0] = 101 : 450kHz, [2:0] = 110 : 500kHz, [2:0] = 111 : 550kHz

Register Address: 0x55h **Description**: Selection AQR be triggered threshold in PS1 for CORE rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CORE_ACLL_MISC6							
Reset Value	0x1Fh							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved bit
[4:0]	AQR_TH_PS1	Selection AQR be triggered threshold in PS1 for CORE rail AQR_TH_PS1 = [4:0] x 40mV + 40mV; [4:0] = 11111 : Disable

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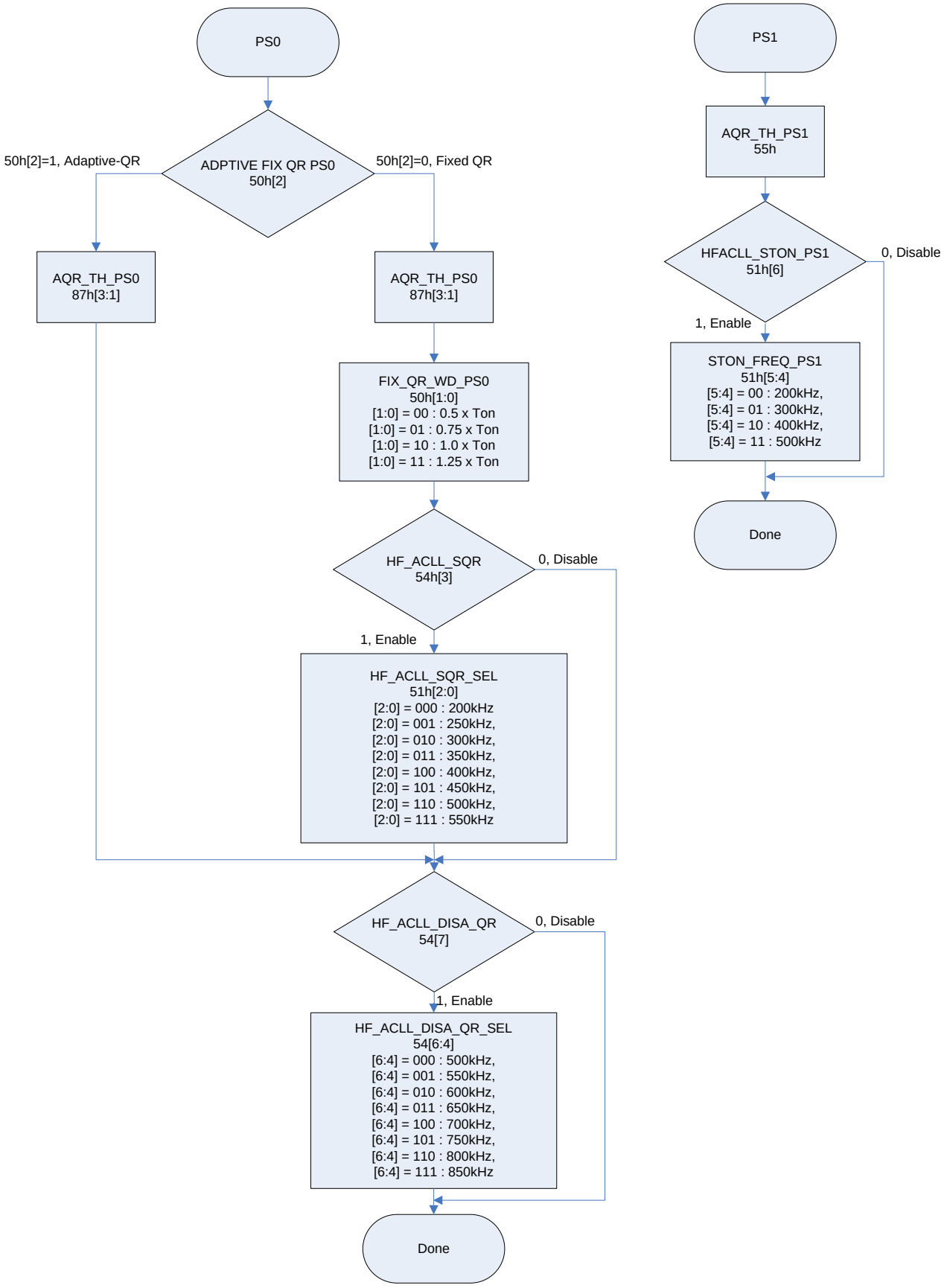

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Register Address: 0x60h **Description**: Selection AQR be triggered threshold for AXG rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AXG_ACLL_MISC1							
Reset Value	0x1Fh							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved bit
[4:0]	AQR_TH_ AXG	Selection AQR be triggered threshold for AXG rail 60H[4] = 0, AQR_TH = 240mV+[3:0]*80mV 60H[4] = 1, AQR_TH = 720mV+[3:0]*80mV [3:0] = 1110, 1111, AQR_TH = Disable

Register Address: 0x61h **Description**: Selection frequency to both the shrink Ton or the disable QR at high frequency ACLL for AXG rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AXG _ACLL_MISC2							
Reset Value	0x79h							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	Reserved	Reserved bit
[6:4]	HF_ACLL_DISA_QR_SEL	Selection to disable QR frequency at high frequency ACLL for AXG rail [6:4] = 000 : Disable, [6:4] = 001 : 475kHz, [6:4] = 010 : 517kHz, [6:4] = 011 : 559kHz, [6:4] = 100 : 601kHz, [6:4] = 101 : 642kHz, [6:4] = 110 : 682kHz, [6:4] = 111 : 724kHz
[3]	HF_ACLL_STON	To shrink Ton at high frequency ACLL for AXG rail [3] = 0 : Disable [3] = 1 : Enable
[2:0]	HF_ACLL_STON_LIFT_VID_SEL	Selection frequency to lift VID and STON at high frequency ACLL for AXG rail [2:0] = 000 : 175kHz, [2:0] = 001 : 220kHz, [2:0] = 010 : 263kHz, [2:0] = 011 : 306kHz, [2:0] = 100 : 348kHz, [2:0] = 101 : 390kHz, [2:0] = 110 : 433kHz, [2:0] = 111 : Disable SQR

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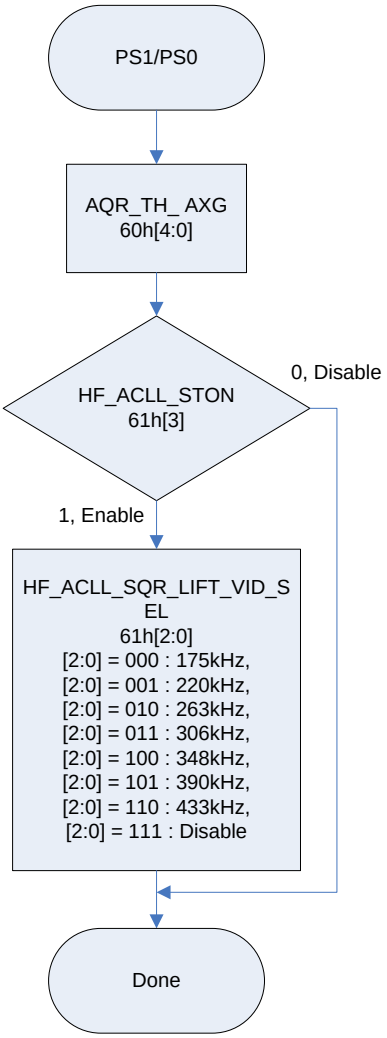

Register Address: 0x62h
Description: Set ramp_adj, ramp_clamp and floating_ramp for AXG rail

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AXG _ACLL_MISC3							
Reset Value	0xC7h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7]	RAMP_ADJ_MASK_TIME	Select mask time of ramp_adj while ramp_aux be triggered for AXG rail [7] = 0 : 20us [7] = 1 : 40us
[6]	ADAPTIVE_RAMP_MASK_ADJ	The ADAPTIVE_RAMP be triggered will mask ramp_adj for AXG rail [6] = 0 : Disable [6] = 1 : Enable
[5:4]	RAMP_CLAMP_TH	Select ramp_clamp threshold for AXG rail [5:4] = 00 : 150mV, [5:4] = 01 : 225mV, [5:4] = 10 : 300mV, [5:4] = 11 : 420mV,
[3:2]	Reserved	Reserved bit
[1:0]	SEL_FLRAMP_TH	Select floating_ramp threshold for AXG rail [1:0] = 00 : 125mV, [1:0] = 01 : 175mV, [1:0] = 10 : 225mV, [1:0] = 11 : Disable

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Register Address: 0x63h **Description**: Set extend Ton and increase Ton threshold for AXG rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AXG _ACLL_MISC4							
Reset Value	0x11h							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved bit
[4]	ACLL_EXTD_TON	Extend Ton at ACLL for AXG rail [4] = 0 : Disable [4] = 1 : Enable
[3:2]	ACLL_EXTD_TON_SET	Select extend Ton ratio at ACLL for AXG rail [3:2] = 00 : 2.66 x Ton, [3:2] = 01 : 2.00 x Ton, [3:2] = 10 : 1.60 x Ton, [3:2] = 11 : 1.33 x Ton
[1:0]	INC_TON_TH	Setting increase Ton threshold for AXG rail [1:0] = 00 : 2.4V + 150mV, [1:0] = 01 : 2.4V + 200mV, [1:0] = 10 : 2.4V + 250mV, [1:0] = 11 : 2.4V + 300mV

Register Address: 0x70h **Description**: Output current reporting of AXG rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ILOAD_RPT_AXG							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	ILOAD_RPT	Output current reporting of AXG rail.

Register Address: 0x72h **Description**: Temperature reporting of AXG rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TEMP_RPT_AXG							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	TEMP_RPT	$V_{THERMALA}$ = TEMP_RPT[7:0] x 6.25mV

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Table 21. $V_{THERMALA}$ vs Temperature (based on the R_{NTC} = 100k/Beta = 4250K)

Temperature (°C)	$V_{THERMALA}$ (V)	Temperature (°C)	$V_{THERMALA}$ (V)	Temperature (°C)	$V_{THERMALA}$ (V)	Temperature (°C)	$V_{THERMALA}$ (V)
61	1.133	81	0.814	101	0.591	121	0.453
62	1.116	82	0.800	102	0.582	122	0.447
63	1.098	83	0.787	103	0.574	123	0.442
64	1.080	84	0.774	104	0.566	124	0.437
65	1.063	85	0.761	105	0.558	125	0.432
66	1.046	86	0.749	106	0.550	126	0.428
67	1.029	87	0.737	107	0.542	127	0.423
68	1.012	88	0.725	108	0.534	128	0.419
69	0.995	89	0.713	109	0.527	129	0.414
70	0.979	90	0.702	110	0.520	130	0.410
71	0.963	91	0.690	111	0.513		
72	0.947	92	0.679	112	0.506		
73	0.931	93	0.669	113	0.500		
74	0.916	94	0.658	114	0.493		
75	0.900	95	0.648	115	0.487		
76	0.885	96	0.638	116	0.481		
77	0.871	97	0.628	117	0.475		
78	0.856	98	0.618	118	0.469		
79	0.842	99	0.609	119	0.463		
80	0.828	100	0.600	120	0.458		

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Register Address: 0x73h
Description: Setting sum OCP threshold of CORE/AXG rail and sum OCP delay time of CORE/AXG rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SUMOC_DLY							
Reset Value	0xF6h							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Description
[7]	SUMOCP_DLY_CORE	**Sum OCP delay time of CORE rail** [7] = 0 : 20us [7] = 1 : 40us
[6]	SUMOCP_DLY_AXG	**Sum OCP delay time of AXG rail** [6] = 0 : 20us [6] = 1 : 40us
[5:3]	SUMOCP_AXG	**Sum OCP threshold of AXG rail** **While Reg. Addr 0x87h[5] = 0** [5:3] = 000 : 60%, [5:3] = 001 : 60%, [5:3] = 010 : 60%, [5:3] = 011 : 60%, [5:3] = 100 : 90%, [5:3] = 101 : 100%, [5:3] = 110 : 130%, [5:3] = 111 : 140% **While Reg. Addr 0x87h[5] = 1** [5:3] = 000 : 60%, [5:3] = 001 : 60%, [5:3] = 010 : 70%, [5:3] = 011 : 80%, [5:3] = 100 : 110%, [5:3] = 101 : 120%, [5:3] = 110 : 150%, [5:3] = 111 : 160%
[2:0]	SUMOCP_CORE	**Sum OCP threshold of CORE rail** **While Reg. Addr 0x87h[5] = 0** [2:0] = 000 : 60%, [2:0] = 001 : 60%, [2:0] = 010 : 60%, [2:0] = 011 : 60%, [2:0] = 100 : 90%, [2:0] = 101 : 100%, [2:0] = 110 : 130%, [2:0] = 111 : 140% **While Reg. Addr 0x87h[5] = 1** [2:0] = 000 : 60%, [2:0] = 001 : 60%, [2:0] = 010 : 70%, [2:0] = 011 : 80%, [2:0] = 100 : 110%, [2:0] = 101 : 120%, [2:0] = 110 : 150%, [2:0] = 111 : 160%

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Register Address: 0x75h **Description**: DVID up period from 0V to 1st PWM pulse after VID settles OVP threshold of CORE/AXG rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		OVP_SS							
Reset Value		0x00h(VID1); 0x05h(VID2)							
Read/Write		R	R	R	R	RW	RW	RW	RW
Bits	**Name**			**Description**					
[7:2]	Reserved			Reserved					
[3:2]	OVP_SS_AXG			**1st PWM pulse after VID settles OVP threshold of AXG rail** [3:2] = 00 : 2.45V(VID1); [3:2] = 01 : 2.65V(VID2); [3:2] = 10 : 2.85V; [3:2] = 11 : 3.05V					
[1:0]	OVP_SS_CORE			**1st PWM pulse after VID settles OVP threshold of CORE rail** [1:0] = 00 : 2.45V(VID1); [1:0] = 01 : 2.65V(VID2); [1:0] = 10 : 2.85V; [1:0] = 11 : 3.05V					

Register Address: 0x76h **Description**: Enable/Disable watchdog function and setting watchdog-Reset period.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		WDR							
Reset Value		0x00h							
Read/Write		R	R	R	R	R	R	RW	RW
Bits	**Name**			**Description**					
[7:2]	Reserved			Reserved					
[1]	EN_WATCHDOG_RESET			**Enable/Disable watchdog function** [1] = 0 : Disable Watchdog-Reset (If SMBus transition hanging exceed 30ms, VR I^2C interface state machine is reset but all register keeps the latest value.) [1] = 1 : Enable Watchdog-Reset (Watchdog period is based on WDR[0] setting. While SMBus transmission hanging exceeds the setting, all I^2C register except for protection flag and 0x80h to 0x8Bh, will be reset to the default value.					
[0]	WATCHDOG_RESET_PERIOD			**Watchdog-Reset period** [0] = 0 : 800ms [0] = 1 : 1600ms					

Register Address: 0x77h **Description:** Watchdog-reset status, being reset after SMBus read this bit or VCC recycle.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		WDR_ST							
Reset Value		--							
Read/Write		R	R	R	R	R	R	R	R
Bits	Name			Description					
[7:1]	Reserved			Reserved					
[0]	WATCHDOG_STATUS			Watchdog-Reset Status [0] = 0 : SMBus transmission normal [0] = 1 : SMBus transmission hanging had ever exceeded watchdog-reset period					

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Register Address: 0x78h **Description**: Output current reporting ratio adjustment of CORE/AXG rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ILOAD_RPT_Ratio							
Reset Value	0x00h							
Read/Write	R	R	R	R	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:4]	Reserved	Reserved
[3:2]	ILOAD_RPT_Ratio_AXG	**Output current reporting ratio adjustment of AXG rail** [3:2] = 00 : 100%, [3:2] = 01 : 87.5%, [3:2] = 10 : 75%, [3:2] = 11 : 50%
[1:0]	ILOAD_RPT_Ratio_CORE	**Output current reporting ratio adjustment of CORE rail** [1:0] = 00 : 100%, [1:0] = 01 : 87.5%, [1:0] = 10 : 75%, [1:0] = 11 : 50%

Register Address: 0x79h **Description**: Output current reporting of AUX rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ILOAD_RPT_AUX							
Reset Value	--							
Read/Write	R	R	R	R	R	R	R	R

Bits	**Name**	**Description**
[7:0]	ILOAD_RPT	Output current reporting of AUX rail.

Register Address: 0x7Ah **Description**: Setting ZCD threshold of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	ZCD_TH_CORE							
Reset Value	--							
Read/Write	R	R	RW	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved
[5:0]	ZCD_TH_CORE	[5] = 0 : Positive ZCD threshold [5] = 1 : Negative ZCD threshold [4:0]: ([4:0]*0.208mV)+0.833 mV **Ex.** ZCD_TH_CORE[5:0] = **0**11010 ZCD_{th_CORE} = (26*0.208mV)+0.833mV **Ex.** ZCD_TH_CORE[5:0] = **1**10010 ZCD_{th_CPRE} = [18*(-0.208mV)]+0.833mV

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Register Address: 0x7Bh **Description**: Setting ZCD threshold of AXG rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		ZCD_TH_AXG							
Reset Value		--							
Read/Write		R	R	RW	RW	RW	RW	RW	RW
Bits	**Name**			**Description**					
[7:6]	Reserved			Reserved					
[5:0]	ZCD_TH_AXG			ZCD_{th_AXG} = (7B[5:0]*0.0625mV)-1.75 mV **Ex.** ZCD_TH_AXG[5:0] = 011010 ZCD_{th_AXG} = (26*0.0625mV)-1.75 mV **Ex.** ZCD_TH_ AXG[5:0] = 110010 ZCD_{th_AXG} = (50*0.0625mV)-1.75 mV					

Register Address: 0x7Ch **Description**: Setting ANTIOVS threshold of CORE/AXG rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		ANTIOVS_TH							
Reset Value		0X3Fh							
Read/Write		R	R	RW	RW	RW	RW	RW	RW
Bits	**Name**			**Description**					
[7:6]	Reserved			Reserved					
[5:3]	AXG_ANTIOVS_TH			**Setting ANTIOVS threshold of AXG rail** [5:3] = 000 : 90mV, [5:3] = 001 : 120mV, [5:3] = 010 : 150mV, [5:3] = 011 : 180mV, [5:3] = 100 : 210mV, [5:3] = 101 : 240mV, [5:3] = 110 : Disable, [5:3] = 111 : Disable					
[2:0]	CORE_ANTIOVS_TH			**Setting ANTIOVS threshold of CORE rail** [2:0] = 000 : 180mV, [2:0] = 001 : 240mV, [2:0] = 010 : 300mV, [2:0] = 011 : 360mV, [2:0] = 100 : 420mV, [2:0] = 101 : 480mV, [2:0] = 110 : Disable, [2:0] = 111 : Disable					

Register Address: 0x80h **Description**: SET1 pin setting ($V_{divider}$) for DVID fast slew rate, I^2C address and K_{TON} (TONSET) of CORE rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MISC1							
Reset Value		--							
Read/Write		R	R	R	RW	RW	RW	RW	RW
Bits	**Name**			**Description**					
[7:5]	Reserved			Reserved					
[4]	DVID_Fast_SR			[4] = 0 : fast_S [4] = 1 : fast_P					
[3]	I2C_ADDS			**I^2C address** [3] = 0 : 0x20h [3] = 1 : 0x21h					
[2:0]	K_{TON}			**On-time (TON) K Factor Setting of CORE rail** [2:0] = 000 : 0.50, [2:0] = 001 : 0.60, [2:0] = 010 : 0.70, [2:0] = 011 : 0.80, [2:0] = 100 : 0.90, [2:0] = 101 : 1.00, [2:0] = 110 : 1.10, [2:0] = 111 : 1.20					

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Register Address: 0x81h
Description: SET1 pin setting (V_{IXR}) for $\overline{VR\_HOT}$ assertion during DVID current limit and ICCMAX of VCCIN_AUX rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	FASTV_VRHOT_SEL_ ICCMAX_AUX							
Reset Value	--							
Read/Write	R	R	R	RW	RW	RW	RW	R

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved
[4]	$\overline{VR\_HOT}$ _DVID	$\overline{VR\_HOT}$ assertion during DVID current limit. $\overline{VR\_HOT}$ _DVID[4] = 0, Disable $\overline{VR\_HOT}$ _DVID[4] = 1, Enable
[3:1]	ICCMAX_AUX	ICCMAX_AUX = 25A + ICCMAX_AUX [3:1] x 5A
[0]	Reserved	Reserved

Register Address: 0x82h
Description: SET2 pin setting ($V_{divider}$) for adaptive ramp trigger threshold in PS1 of CORE rail and ICCMAX of AXG rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AR_TH_CORE_ICCMAX_AXG							
Reset Value	--							
Read/Write	R	R	R	RW	RW	RW	RW	RW

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved
[4:3]	AR_TH	**Adaptive ramp trigger threshold in PS1 of CORE rail** [4:3] = 00 : 175mV, [4:3] = 01 : 150mV, [4:3] = 10 : 125mV, [4:3] = 11 : Disable
[2:0]	ICCMAX_A	**ICCMAX of AXG rail** ICCMAX = 22A + IccMAX_A[2:0] x 4

Register Address: 0x83h
Description: SET2 pin setting (V_{IXR}) for Dual Phases Function of CORE rail and K_{TON} (TONSET) of AXG rail.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_DBLR_KTON_AXG							
Reset Value	--							
Read/Write	R	R	R	RW	RW	RW	RW	R

Bits	**Name**	**Description**
[7:5]	Reserved	Reserved
[4]	Dual_Phases	**Dual Phases Function** [4] = 0 : Each PWM output drives one phase. [4] = 1 : Each PWM output drives two phases.
[3:1]	K_{TON}_A	**On-time (TON) K Factor Setting of AXG rail** [3:1] = 000 : 0.82, [3:1] = 001 : 0.91, [3:1] = 010 : 1.00, [3:1] = 011 : 1.09, [3:1] = 100 : 1.18, [3:1] = 101 : 1.27, [3:1] = 110 : 1.36, [3:1] = 111 : 1.55
[0]	Reserved	Reserved

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Register Address: 0x84h **Description**: SET3 pin setting ($V_{divider}$) for VID table and and IccMAX of CORE rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		DAC_SEL_ICCMAX							
Reset Value		--							
Read/Write		R	R	R	RW	RW	RW	RW	RW
Bits	**Name**	**Description**							
[7:5]	Reserved	Reserved							
[4]	DAC_SEL	**VID step** [4] = 0 : VID1 [4] = 1 : VID2							
[3:0]	ICCMAX	**ICCMAX of CORE rail** **83[4]= 0, Each PWM output drives one phase.** 4 phase operation ICCMAX = 93A + IccMAX[3:0] x 7A 5 phase operation ICCMAX = 134A + IccMAX[3:0] x 6A 6 phase operation ICCMAX = 170A + IccMAX[3:0] x 6A 7 phase operation ICCMAX = 206A + IccMAX[3:0] x 6A 8 phase operation ICCMAX = 232A + IccMAX[3:0] x 6A **83[4] = 1, Each PWM output drives two phases.** 8 phase operation ICCMAX = 232A + IccMAX[3:0] x 6A 10/12/14/16 phase operation ICCMAX = 233A + IccMAX[3:0] x 7A							

Register Address: 0x85h **Description**: SET3 pin setting (V_{IXR}) for VBOOT of CORE/AXG rail and adaptive ramp trigger threshold of AXG rail.									
Bits		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		MISC2							
Reset Value		--							
Read/Write		R	R	R	RW	RW	RW	RW	R
Bits	**Name**	**Description**							
[7:5]	Reserved	Reserved							
[4]	VBOOT	**VBOOT of CORE rail** [4] = 0 : 0V [4] = 1 : non-zero							
[3]	VBOOT_A	**VBOOT of AXG rail** [3] = 0 : 0V [3] = 1 : non-zero							
[2:1]	AR_TH_A	**Adaptive ramp trigger threshold of AXG rail** [2:1] = 00 : Disable, [2:1] = 01 : 125mV, [2:1] = 10 : 175mV, [2:1] = 11 : 225mV							
[0]	Reserved	Reserved							

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Register Address: 0x86h **Description**: TSEN pin setting ($V_{divider}$) for ZCD threshold of CORE rail and Ai gain of CORE/AXG rail								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MISC3							
Reset Value	--							
Read/Write	R	R	RW	RW	RW	RW	RW	R

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved
[5]	ZCD_TH	**ZCD threshold for CORE rail** [5] = 0 : 0.417mV [5] = 1 : 0.208mV
[4:3]	Ai_A	**Current gain (Ai) of AXG rail** [4:3] = 00 : 0.75, [4:3] = 01 : 1.13, [4:3] = 10 : 1.5, [4:3] = 11 : 1.88
[2:1]	Ai	**Current gain (Ai) of Core rail** [2:1] = 00 : 0.25, [2:1] = 01 : 0.5, [2:1] = 10 : 0.75, [2:1] = 11 : 1
[0]	Reserved	Reserved

Register Address: 0x87h **Description**: TSENA pin setting ($V_{divider}$) for sum OCP ratio of CORE/AXG rail and AQR threshold of CORE rail.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SUMOCP_ZCD_TH_AXG							
Reset Value	--							
Read/Write	R	R	RW	RW	RW	RW	RW	R

Bits	**Name**	**Description**
[7:6]	Reserved	Reserved
[5]	SUMOCP_CORE_AXG	Sum OCP threshold of CORE and AXG rail **While Reg. Addr 0x73h[2:0] =110 & 0x73h[5:3] =110 (Default)** [5] = 0 : 130%, [5] = 1 : 150%
[4]	ZCD_TH_AXG	Set ZCD threshold for AXG rail [4] = 0 : 0.063mV [4] = 1 : 0.188mV
[3:1]	AQR_TH	**AQR Starting Trigger Threshold of CORE rail** [3:1] = 000 : 240mV, [3:1] = 001 : 400mV, [3:1] = 010 : 560mV, [3:1] = 011 : 800mV, [3:1] = 100 : 880mV, [3:1] = 101 : 1040mV, [3:1] = 110 : 1200mV, [3:1] = 111 : Disable
[0]	Reserved	Reserved

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Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-60L 7x7 package, the thermal resistance, θ_{JA}, is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (25.5°C/W) = 3.92W for a WQFN-60L 7x7 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 39 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

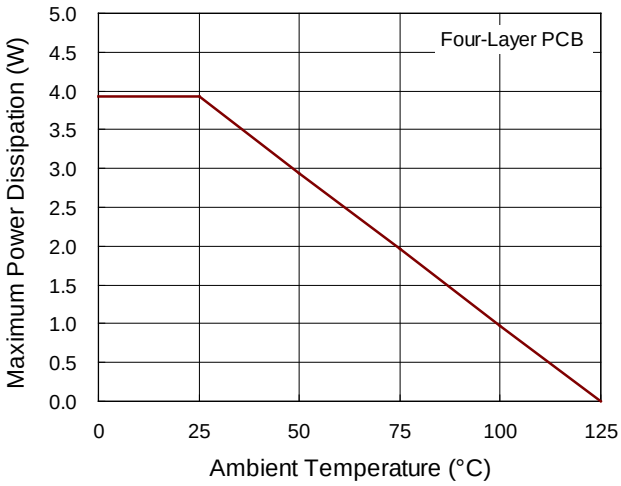

Figure 39. Derating Curve of Maximum Power Dissipation

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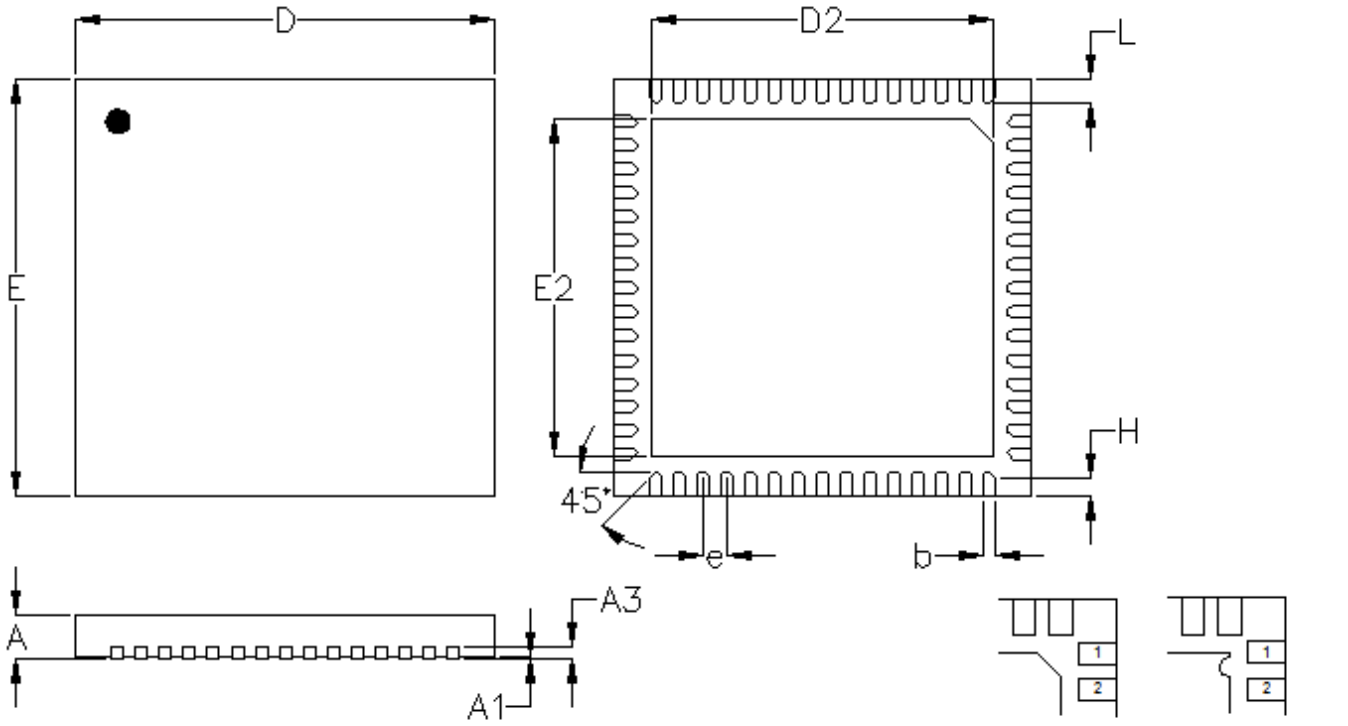
Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

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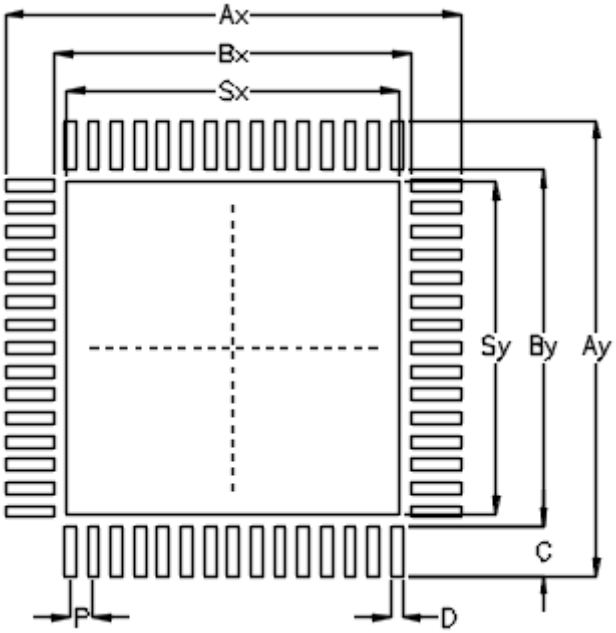
Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-60	60	0.40	7.80	7.80	6.10	6.10	0.85	0.20	5.70	5.70	±0.05

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