PJMG10H25NDL

N-Channel Enhancement Mode Power MOSFET

Product Summary

- V_{DS}= 100V,I_D= 24A
- $R_{DS(on)}$< 26mΩ @V_{GS}= 10V
- $R_{DS(on)}$< 33mΩ @V_{GS}= 4.5V

Features

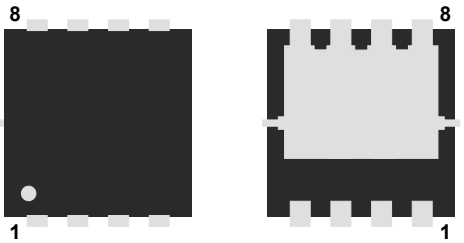
- Advanced Split Gate Trench Technology
- 100% Avalanche Tested
- RoHS Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3

Application

- Load Switch
- PWM Application
- Power Management

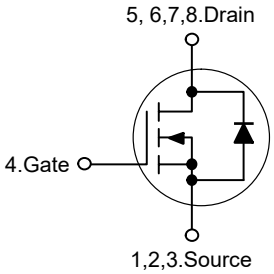
Marking Code

PDFN3x3-8L



Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain

Schematic Diagram



Absolute Maximum Ratings

Ratings at 25℃ case temperature unless otherwise specified.

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	T_C=25°C	I_D	24	A
	T_C=100°C		15	A
Drain Current-Pulsed Note1		I_{DM}	96	A
Single Pulse Avalanche Energy Note2		E_{AS}	27.6	mJ
Maximum Power Dissipation		P_D	25	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Characteristics

Thermal Resistance, Junction-to-Case Note3	$R_{\theta JC}$	5	°C/W

Electrical Characteristics

(T_C=25℃ unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage Note4	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	--	2.5	V
Drain-Source On-Resistance Note4	$R_{DS(on)}$	V_{GS}=10V,I_D=10A	--	--	26	mΩ
		V_{GS}=4.5V,I_D=8A	--	--	33	mΩ
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHz	--	660	--	pF
Output Capacitance	C_{oss}		--	375	--	pF
Reverse Transfer Capacitance	C_{rss}		--	21	--	pF
Total Gate Charge	Q_g	V_{DS}=50V, I_D=10A , V_{GS}=10V	--	25	--	nC
Gate-Source Charge	Q_{gs}		--	6	--	nC
Gate-Drain Charge	Q_{gd}		--	5	--	nC
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=10A, V_{GS}=10V, R_{GEN}=3Ω	--	14	--	nS
Turn-on Rise Time	t_r		--	12	--	nS
Turn-off Delay Time	$t_{d(off)}$		--	23	--	nS
Turn-off Fall Time	t_f		--	6	--	nS
Source-Drain Diode Characteristics						
Diode Forward Voltage Note4	V_{SD}	V_{GS}=0V,I_S=24A	--	--	1.2	V
Diode Forward Current	I_S		--	--	24	A

Note:

1. Repetitive Rating:Pulse width limited by maximum junction temperature
2. EAS condition: T_J=25℃,V_{DD}=50V, V_{GS}=10V, R_G=25Ω, L=0.5mH, I_{AS}=10.5A
3. Surface mounted on 1inch^2 FR-4 board with 2OZ copper
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Test Circuit

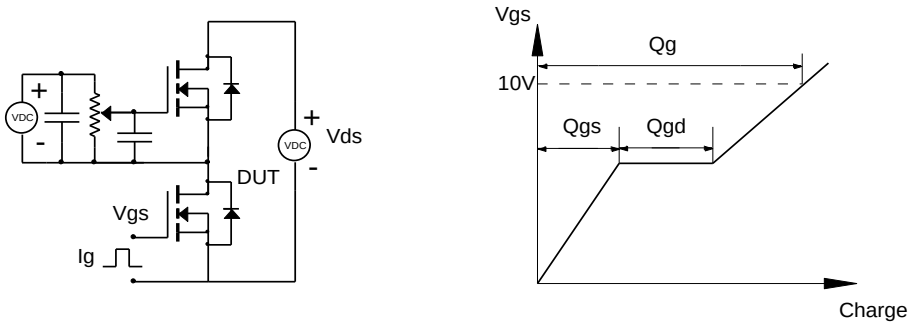


Figure 1: Gate Charge Test Circuit & Waveform

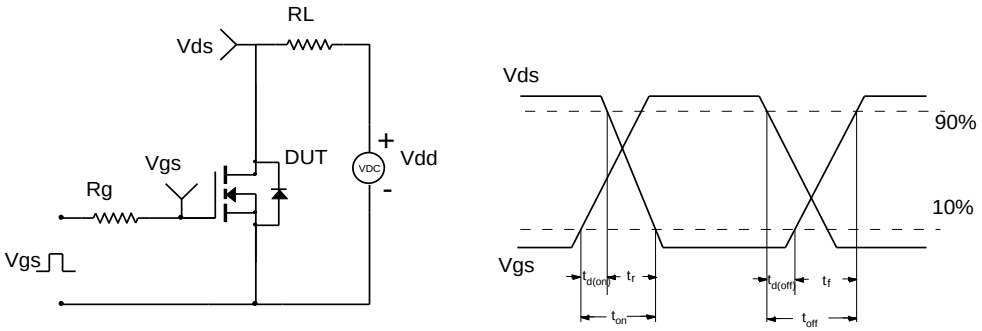


Figure 2: Resistive Switching Test Circuit & Waveform

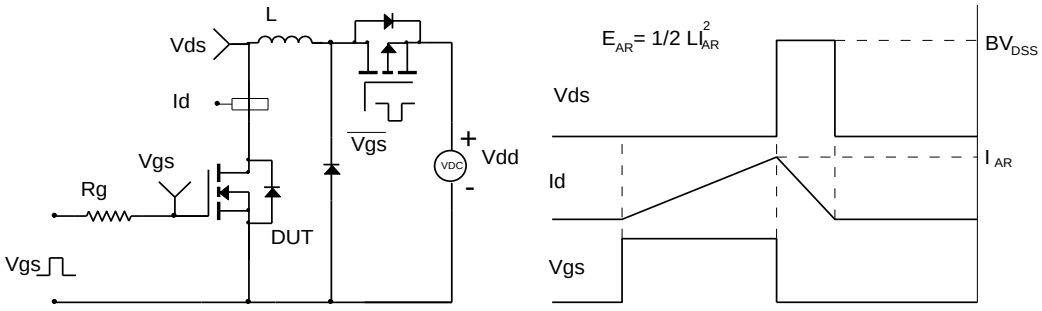


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

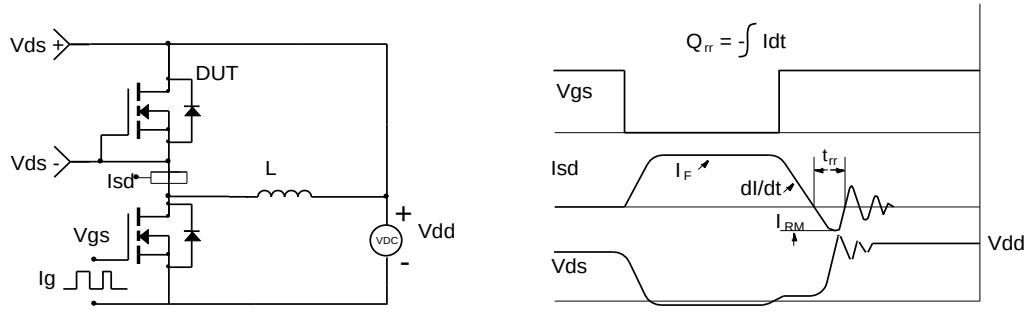
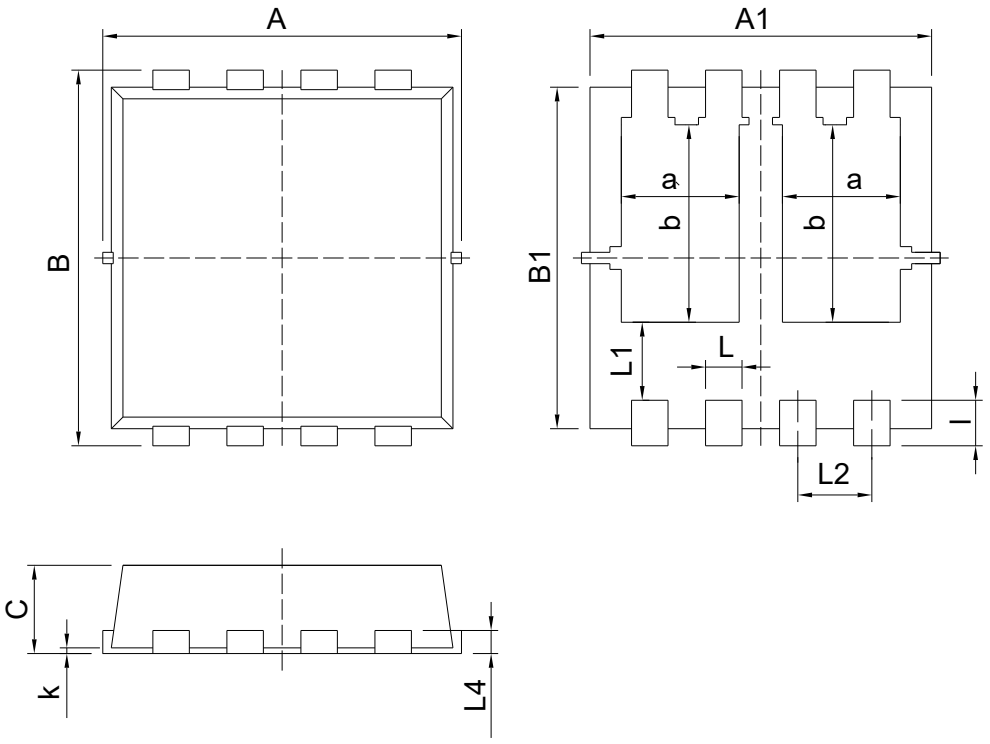


Figure 4: Diode Recovery Test Circuit & Waveform

Package Outline

PDFN3x3A-8L

Dimensions in mm



Symbol	Dimensions		Symbol	Dimensions	
	Min.	Max.		Min.	Max.
A	3.2	3.4	L2	0.55	0.75
A1	3.1	3.2	L4	0.14	0.20
B	3.2	3.4	a	0.935	1.135
B1	2.95	3.05	b	1.635	1.835
C	0.75	0.85	k	0.0	0.05
L	0.25	0.35	l	0.3	0.5
L1	-	0.75			