

DOS2181 700V Half Bridge MOSFET/IGBT Gate Driver

1 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ± 50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
 - UVLO forward 8.9V
 - UVLO reverse 8.2V
- Turn-on/Turn-off propagation delay
 - Ton/Toff =130ns/130ns
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 1.9A/2.3A
- RoSH compatible

2 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

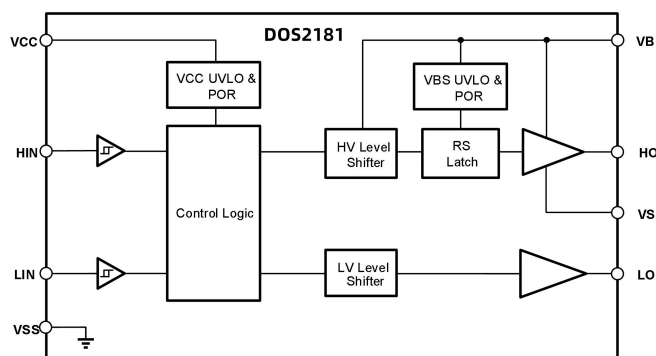
3 Description

The DOS2181 is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

Device information

Part Number	Package	Body size
DOS2181	SOIC8	4.9mm x 3.9mm

Functional Block Diagram



4 Selection Guide

Part No.	High-side input	Low-side input	Anti-cross	Dead-time	VBS UVLO	Ton/Toff (ns)	IO+/IO- (A)
DOS2181	HIN	LIN	NO	--	YES	130/130	1.9/2.3

5 Function Pin Description

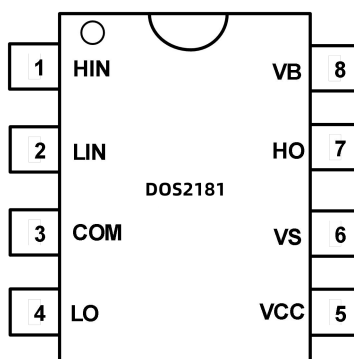


Figure 5-1 8-Pin SOIC8 Top view

Table 5-1 Lead Definitions

Number	Symbol	Description
1	HIN	Logic input for high side gate driver output (HO), in phase
2	LIN	Logic input for low side gate driver output (LO), in phase
3	COM	Low side return
4	LO	Low side gate drive output
5	VCC	Low side and logic fixed supply
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

6 Product specifications

6.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	-0.3	725	V
V _S	High side floating supply return	V _B - 25	V _B + 0.3	
V _{HO}	High side gate drive output	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side and main power supply	-0.3	25	
V _{LO}	Low side gate drive output	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input (HIN, LIN)	-0.3	V _{CC} + 0.3	

6.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1.5	—	kV
	Machine Model	500	—	V

6.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P _D	Package Power Dissipation @ TA ≤25°C	—	0.625	W

6.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
RthJA	Thermal Resistance, Junction to Ambient	—	200	°C /W
T _J	Junction Temperature	—	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	—	300	

6.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V _B	High side floating supply	V _S + 10	V _S + 20	V
V _S	High side floating supply return	-9	700	
V _{HO}	High side gate drive output	V _S	V _B	
V _{CC}	Low side and main power supply	10	20	
V _{LO}	Low side gate drive output	0	V _{CC}	
V _{IN}	Logic input of HIN & LIN	0	V _{CC}	
T _A	Ambient temperature	-40	125	°C

6. 6 Electrical Characteristics

Valid for temperature range at $T_A = 25^\circ\text{C}$, $V_{CC} = V_B = 15\text{V}$, $C_L = 1\text{nF}$, unless otherwise specified

6.6.1 Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	130	250	ns	$V_S = 0$
t_{OFF}	Turn-off propagation delay	—	130	250		$V_S = 0\text{V}$ or 700V
t_R	Turn-on rise time	—	15	20		$V_S = 0\text{V}$
t_F	Turn-off fall time	—	10	15		
MT	Matched propagation time delay	—	—	50		

6.6.2 Static electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0		
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—		
V_{BSUV+}	VBS supply UVLO threshold	8	8.9	9.8		
V_{BSUV-}		7.4	8.2	9.0		
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.7	—		
I_{LK}	High-side floating supply leakage current	—	—	50	μA	$V_B = V_S = 700\text{V}$
I_{QBS}	Quiescent VB supply current	—	50	100		$V_{IN} = 0\text{V}$ or 5V
I_{QCC}	Quiescent VCC supply current	—	150	240		
V_{IH}	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10 \sim 20\text{V}$
V_{IL}	Logic "0" input voltage	—	—	0.8		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4		$I_O = 0\text{A}$
V_{OL}	Low level output voltage, V_O	—	—	0.1		$I_O = 20\text{mA}$
I_{IN+}	Logic "1" Input bias current	—	25	60	μA	$V_O = 5\text{V}$,
I_{IN-}	Logic "0" Input bias current	—	—	2		$V_O = 0\text{V}$,
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	$V_O = 0\text{V}$ $PW \leq 10\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		$V_O = 15\text{V}$ $PW \leq 10\mu\text{s}$

7 Function Description

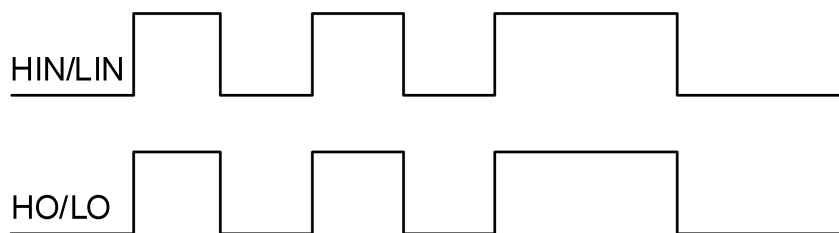


Figure 7 -1 DOS2181 Input and output timing waveform

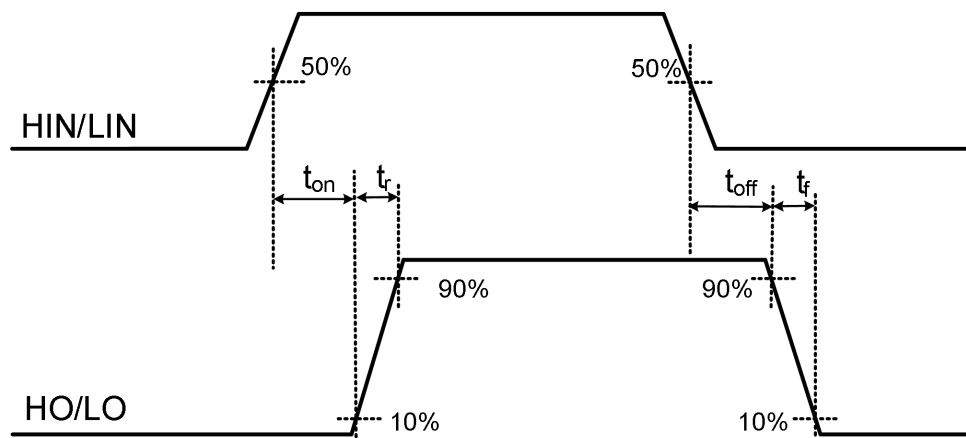


Figure 7 -2 Propagation Time Waveform Definition

8 DOS2181 Description

8.1 Function Block Diagram

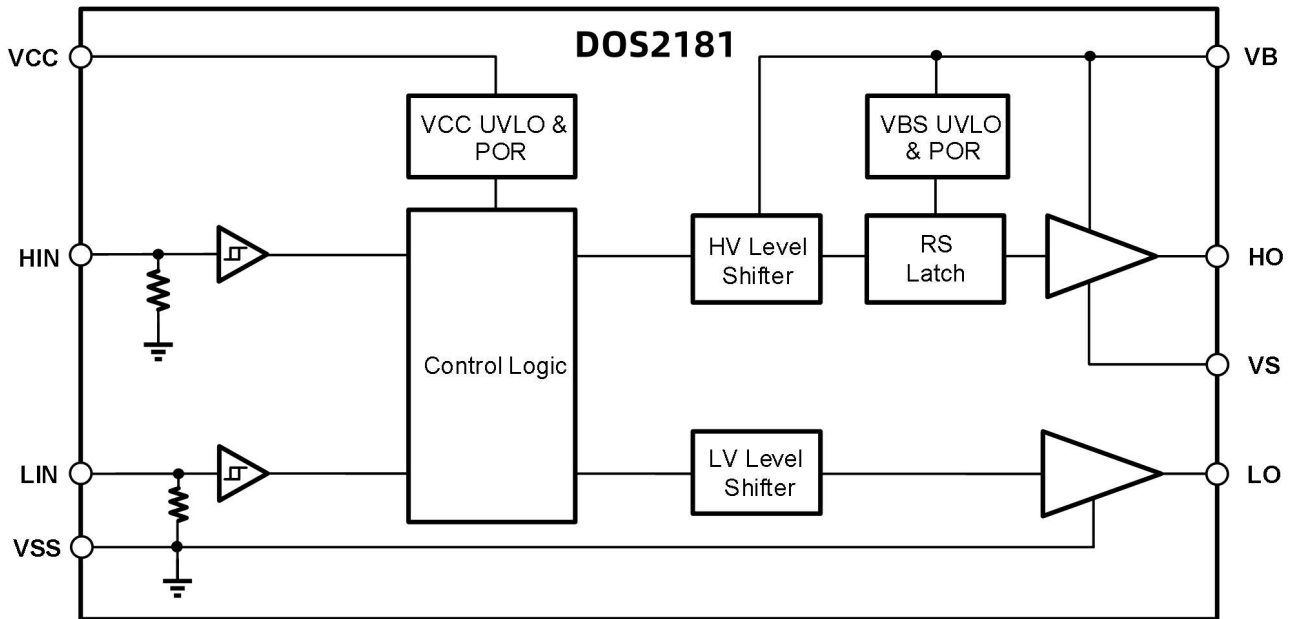


Figure 8 -1 Function Block Diagram of DOS2181

8.2 Application message

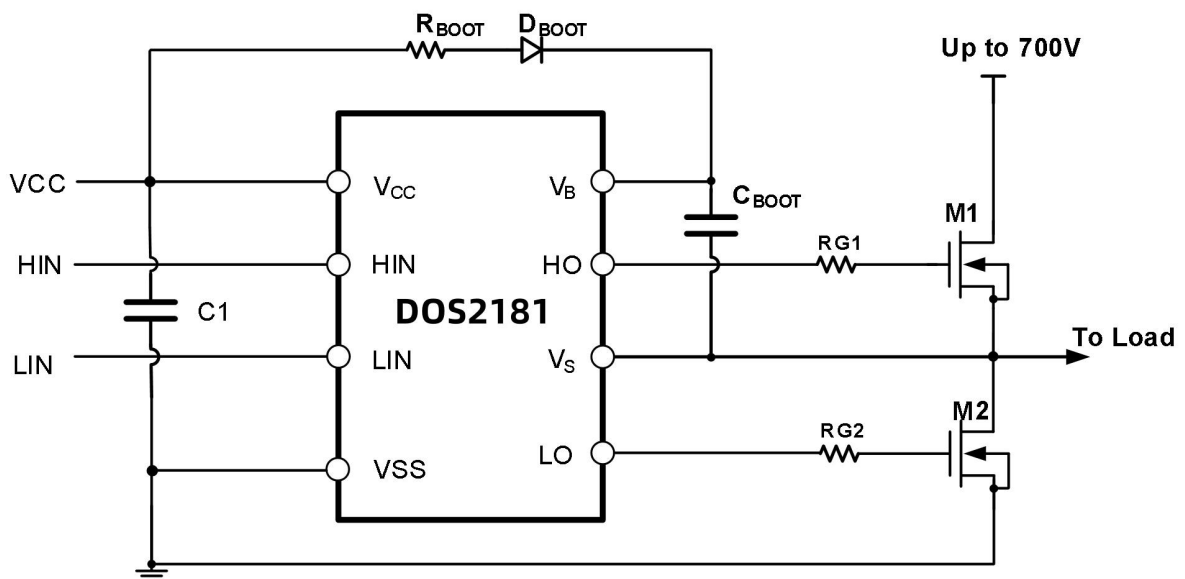


Figure 8-2 Typical application circuit of DOS2181

9. Package Information

SOIC-8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50		
c	0.21	-	0.26	L1	1.05BSC	-	-
c1	0.19	0.20	0.21	θ	0	-	8°

SOIC-8 Package Outlines

