AFE954/AFE956/AFE958/AFE959

低功耗、8 通道、24 位生物电位测量的模拟前端

1. 特性

- 8 个低噪声可编程增益放大器(PGA)和 8 个高分辨率模数转换器(ADC)
- 工作模式:
  - 高速模式(只有 AFE959 有)
  - 高分辨率模式
  - 低功耗模式：每通道 1.56mW
  - 超级低功率模式(只有 AFE959 有)
- 输入引入噪声：5μV_{PP} (150Hz 带宽(BW)，G = 6)
- 输入偏置电流：100pA
- 数据速率：125PS 至 64kSPS
- 共模抑制比(CMRR)：123dB
- 可编程增益：1、2、3、4、6、8、12 或 24
- 支持满足 AAMI EC11、EC13、IEC 60601-1、IEC 60601-2-27 和 IEC 60601-2-51 标准的系统
- 单极或双极电源:
  - AVDD = 2.7V 至 5.5V
  - DVDD = 1.65V 至 3.6V
  - IOVDD = 1.65V 至 3.6V
- 内置右腿驱动放大器、导联断开检测、威尔逊中心终端、起搏检测、测试信号
- 集成呼吸阻抗测量
  - 调制频率：32kHz、43kHz、64kHz
  - 独立数据速率：125SPS 至 16kSPS
- 内置数字转换电压，水晶振荡器，交流导联脱落激励
- 内置振荡器与基准
- SPI™兼容串口，菊花链

2. 应用

- 医疗仪器(心电图(ECG)、肌电图(EMG)和脑电图(EEG))：病人监护；动态心电图，事件，压力，以及生命体征，包括 ECG、AED、远程医疗双谱指数(BIS)、诱发音频电位(EAP)、睡眠监护仪

3. 说明

AFE954、AFE955、AFE956、AFE957、AFE958 和 AFE959 (AFE95x)是多通道同步采样 24 位 Δ-Σ 模数转换器(ADC)系列，内置有可编程增益放大器(PGA)、内部基准以及板载振荡器。AFE95x 包含医疗心电图(ECG)和脑电图应用中通常所需的全部功能。凭借高集成度和出色性能，AFE95x 能够以大幅缩小的尺寸、显著降低的功耗和整体成本开发可扩展的医疗仪器系统。

AFE95x 的每个通道都有一个灵活的输入复用器(mux)，此复用器能够独立连接至内部生成的信号以进行测试、温度、和导联断开检测。此外，可选择输入通道的任一配置生成右腿驱动(RLD)输出信号。AFE95x 工作数据速率高达 64kSPS，因此可实现软件起搏检测。可通过上拉/下拉电阻或激励电流阱/电流源在器件内部实现导联断开检测。3 个集成放大器用于生成标准 12 导联 ECG 所需的威尔逊中心终端(WCT)。可在高通道数系统中采用菊花链配置串联多个 AFE95x 器件。

封装采用微型 8mm × 8mm、64 焊球 BGA。BGA 版本的工业级额定温度范围为–40°C 至+85°C。

有关订购信息，请参阅 Table 1。

Note: AFE95x refers to AFE954, AFE956, AFE958, and AFE959 in this document.

Simplified Schematic

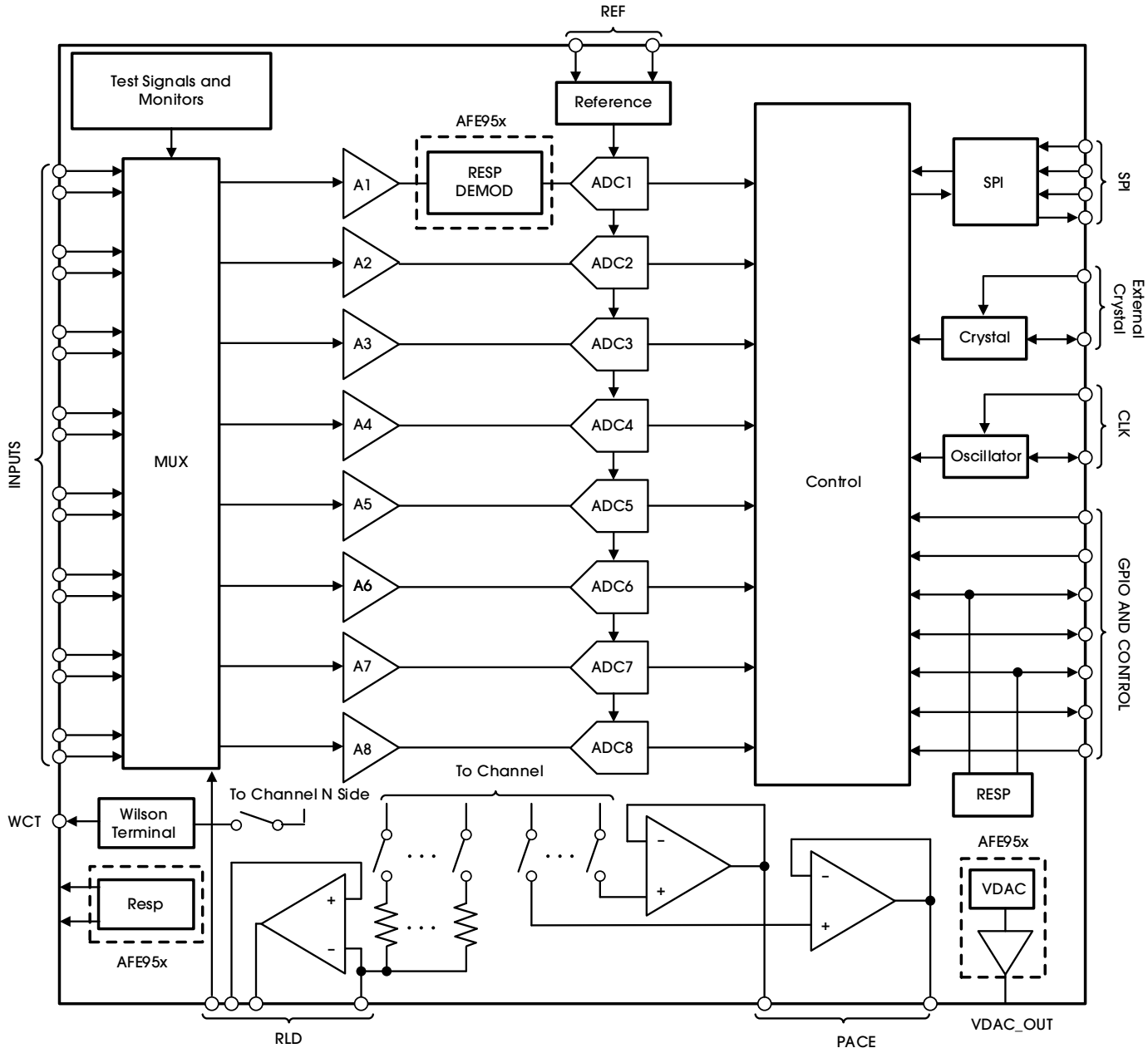


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER(1)	CH (#)	PACKAGE	RESOLUTION (BIT)	OUTPUT DATA RATE	RESPIRATION	ANALOG PACE	AC LEAD-OFF	NOISE, G = 6 (μV_{PP})	FEATURES	OP. TEMP (°C)	MARK	RATING	MSL	PKG. OPTION
AFE954ABGA64	4	BGA-64	24	250/32k	Y	Y	Y	4.9	RESP, WCT, DAC	–40-85	Company Logo AFE954 XXXXXX(3)	Industrial	3	T/R-1000
AFE956ABGA64	6	BGA-64	24	250/32k	Y	Y	Y	4.9	RESP, WCT, DAC	–40-85	Company Logo AFE956 XXXXXX(3)	Industrial	3	T/R-1000
AFE958ABGA64	8	BGA-64	24	250/32k	Y	Y	Y	4.9	RESP, WCT, DAC	–40-85	Company Logo AFE958 XXXXXX(3)	Industrial	3	T/R-1000
AFE959ABGA64(2)	8	BGA-64	24	125/64k	Y	Y	Y	4.9	RESP, WCT, DAC	–40-85	Company Logo AFE959 XXXXXX(3)	Industrial	3	T/R-1000

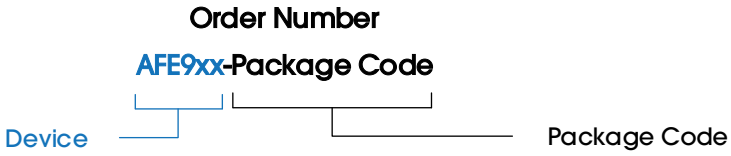
Table 2. Family Selection Guide

ORDER NUMBER(1)	CH (#)	PACKAGE	RESOLUTION (BIT)	OUTPUT DATA RATE	RESPIRATION	ANALOG PACE	AC LEAD-OFF	NOISE, G = 6 (μV_{PP})	FEATURES	OP. TEMP (°C)	MARK	RATING	MSL	PKG. OPTION
AFE924AQFP64	4	QFP-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE924 XXXXXX(3)	Industrial	3	T/R-1000
AFE926AQFP64	6	QFP-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE926 XXXXXX(3)	Industrial	3	T/R-1000
AFE928AQFP64	8	QFP-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE928 XXXXXX(3)	Industrial	3	T/R-1000
AFE924ABGA64	4	BGA-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE924 XXXXXX(3)	Industrial	3	T/R-1000
AFE926ABGA64	6	BGA-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE926 XXXXXX(3)	Industrial	3	T/R-1000
AFE928ABGA64	8	BGA-64	24	125/8k	N	Y	N	8	WCT, DAC	–40-85	Company Logo AFE928 XXXXXX(3)	Industrial	3	T/R-1000
AFE944AQFP64	4	QFP-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE944 XXXXXX(3)	Industrial	3	T/R-1000
AFE946AQFP64	6	QFP-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE946 XXXXXX(3)	Industrial	3	T/R-1000
AFE948AQFP64	8	QFP-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE948 XXXXXX(3)	Industrial	3	T/R-1000
AFE949AQFP64(2)	8	QFP-64	24	125/64k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE949 XXXXXX(3)	Industrial	3	T/R-1000
AFE944ABGA64	4	BGA-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE944 XXXXXX(3)	Industrial	3	T/R-1000
AFE946ABGA64	6	BGA-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE946 XXXXXX(3)	Industrial	3	T/R-1000
AFE948ABGA64	8	BGA-64	24	250/32k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE948 XXXXXX(3)	Industrial	3	T/R-1000
AFE949ABGA64(2)	8	BGA-64	24	125/64k	N	Y	Y	6	WCT, DAC	–40-85	Company Logo AFE949 XXXXXX(3)	Industrial	3	T/R-1000

ORDER NUMBER[1]	CH (#)	PACKAGE	RESOLUTION (BIT)	OUTPUT DATA RATE	RESPIRATION	ANALOG PACE	AC LEAD-OFF	NOISE, G = 6 (μVPP)	FEATURES	OP. TEMP (°C)	MARK	RATING	MSL	PKG. OPTION
AFE964AQFP64	4	QFP-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE964 XXXXXX[3]	Industrial	3	T/R-1000
AFE966AQFP64	6	QFP-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE966 XXXXXX[3]	Industrial	3	T/R-1000
AFE968AQFP64	8	QFP-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE968 XXXXXX[3]	Industrial	3	T/R-1000
AFE964ABGA64	4	BGA-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE964 XXXXXX[3]	Industrial	3	T/R-1000
AFE966ABGA64	6	BGA-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE966 XXXXXX[3]	Industrial	3	T/R-1000
AFE968ABGA64	8	BGA-64	24	125/32k	N	N	Y	1.5	DAC	–40-85	Company Logo AFE968 XXXXXX[3]	Industrial	3	T/R-1000
AFE914AQFP64	4	QFP-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE914 XXXXXX[3]	Industrial	3	T/R-1000
AFE916AQFP64	6	QFP-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE916 XXXXXX[3]	Industrial	3	T/R-1000
AFE918AQFP64	8	QFP-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE918 XXXXXX[3]	Industrial	3	T/R-1000
AFE914ABGA64	4	BGA-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE914 XXXXXX[3]	Industrial	3	T/R-1000
AFE916ABGA64	6	BGA-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE916 XXXXXX[3]	Industrial	3	T/R-1000
AFE918ABGA64	8	BGA-64	16	125/8k	N	Y	N	12	WCT	–40-85	Company Logo AFE918 XXXXXX[3]	Industrial	3	T/R-1000
AFE934ABGA64[2]	4	BGA-64	24	125/8k	Y	Y	N	8	RESP, WCT, DAC	–40-85	Company Logo AFE934 XXXXXX[3]	Industrial	3	T/R-1000
AFE936ABGA64[2]	6	BGA-64	24	125/8k	Y	Y	N	8	RESP, WCT, DAC	–40-85	Company Logo AFE936 XXXXXX[3]	Industrial	3	T/R-1000
AFE938ABGA64[2]	8	BGA-64	24	125/8k	Y	Y	N	8	RESP, WCT, DAC	–40-85	Company Logo AFE938 XXXXXX[3]	Industrial	3	T/R-1000
AFE904AQFP64[2]	4	QFP-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE904 XXXXXX[3]	Industrial	3	T/R-1000
AFE906AQFP64[2]	6	QFP-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE906 XXXXXX[3]	Industrial	3	T/R-1000
AFE908AQFP64[2]	8	QFP-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE908 XXXXXX[3]	Industrial	3	T/R-1000
AFE904ABGA64[2]	4	BGA-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE904 XXXXXX[3]	Industrial	3	T/R-1000
AFE906ABGA64[2]	6	BGA-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE906 XXXXXX[3]	Industrial	3	T/R-1000
AFE908ABGA64[2]	8	BGA-64	24	62.5/8k	N	Y	N	9	WCT	–40-85	Company Logo AFE908 XXXXXX[3]	Industrial	3	T/R-1000

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or,
2. Contact our sales team by mailing to sales@analogysemi.com.

Note 1:



Note 2: Available in the future.

Note 3: "XXXXXX": For internal use.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

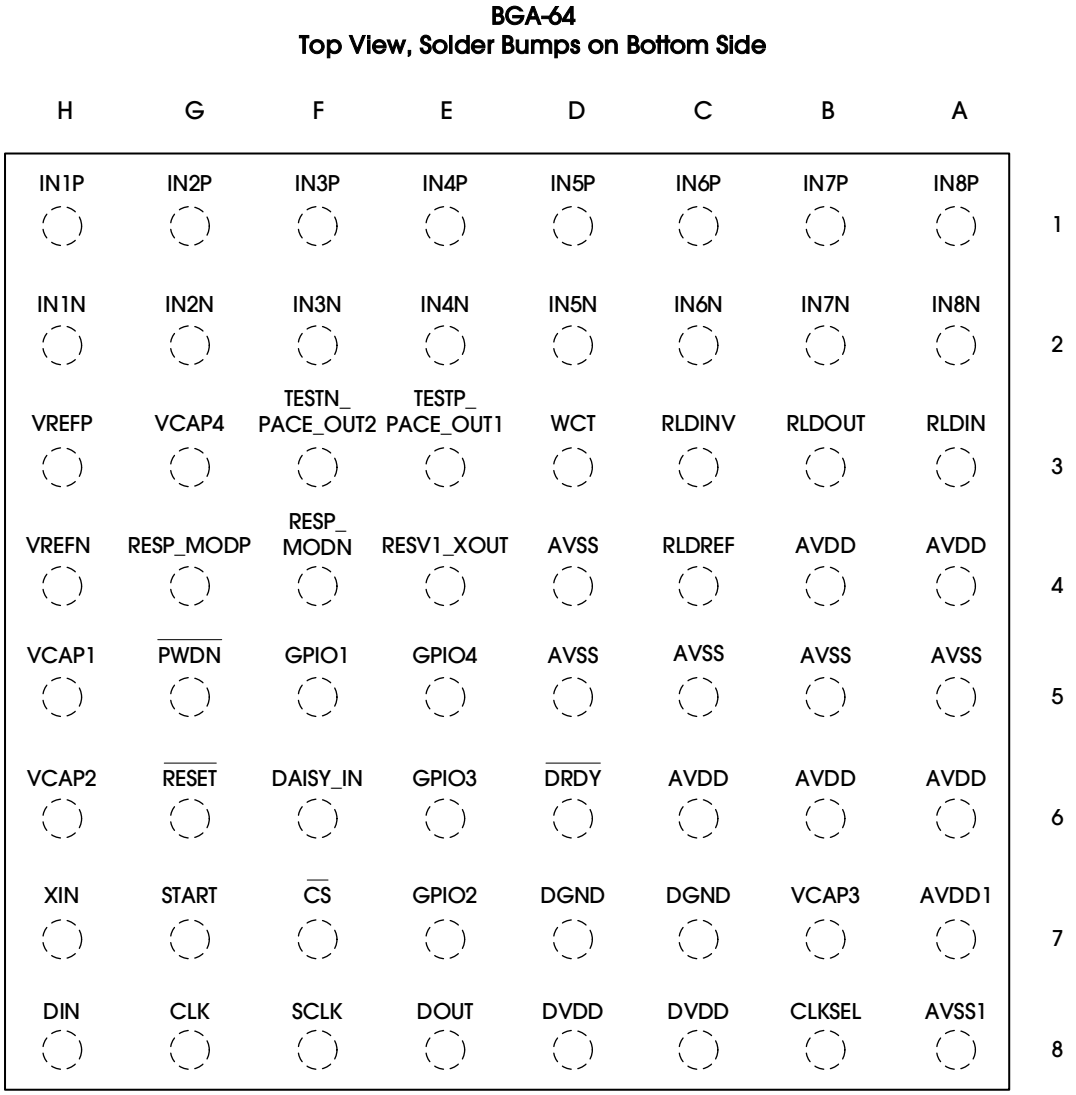


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

PIN	POSITION	TYPE	DESCRIPTION
IN8P(1)	1A	Analog input	Differential analog positive input 8 (AFE958, AFE959)
IN7P(1)	1B	Analog input	Differential analog positive input 7 (AFE958, AFE959)
IN6P(1)	1C	Analog input	Differential analog positive input 6 (AFE956, AFE958, AFE959)
IN5P(1)	1D	Analog input	Differential analog positive input 5 (AFE956, AFE958, AFE959)
IN4P(1)	1E	Analog input	Differential analog positive input 4
IN3P(1)	1F	Analog input	Differential analog positive input 3
IN2P(1)	1G	Analog input	Differential analog positive input 2
IN1P(1)	1H	Analog input	Differential analog positive input 1
IN8N(1)	2A	Analog input	Differential analog negative input 8 (AFE958, AFE959)
IN7N(1)	2B	Analog input	Differential analog negative input 7 (AFE958, AFE959)
IN6N(1)	2C	Analog input	Differential analog negative input 6 (AFE956, AFE958, AFE959)
IN5N(1)	2D	Analog input	Differential analog negative input 5 (AFE956, AFE958, AFE959)
IN4N(1)	2E	Analog input	Differential analog negative input 4

PIN	POSITION	TYPE	DESCRIPTION
IN3N(1)	2F	Analog input	Differential analog negative input 3
IN2N(1)	2G	Analog input	Differential analog negative input 2
IN1N(1)	2H	Analog input	Differential analog negative input 1
RLDIN(1)	3A	Analog input	Right leg drive input to mux
RLDOUT	3B	Analog output	Right leg drive output
RLDINV	3C	Analog input/output	Right leg drive inverting input
WCT_IO	3D	Analog output	Wilson central terminal output
TESTP_PACE_OUT1(1)	3E	Analog input/buffer output	Internal test signal or single-ended buffer output based on register settings
TESTN_PACE_OUT2(1)	3F	Analog input/output	Internal test signal or single-ended buffer output based on register settings
VCAP4	3G	—	Analog bypass capacitor; connect 1μF capacitor to AVSS
VREFP	3H	Analog input/output	Positive reference input/output voltage
AVDD	4A	Supply	Analog supply
AVDD	4B	Supply	Analog supply
RLDREF	4C	Analog input	Right leg drive non-inverting input
AVSS	4D	Supply	Analog ground
RESV1/XOUT	4E	Digital input	Reserved for future use; must tie to logic low (DGND).
RESP_MODN	4F	Analog output	Modulation clock for respiration measurement, negative side.
RESP_MODP	4G	Analog output	Modulation clock for respiration measurement, positive side.
VREFN	4H	Analog input	Negative reference voltage
AVSS	5A	Supply	Analog ground
AVSS	5B	Supply	Analog ground
AVSS_VDAC	5C	Supply	Analog ground
AVSS	5D	Supply	Analog ground
GPIO4	5E	Digital input/output	General-purpose input/output pin 4
GPIO1	5F	Digital input/output	General-purpose input/output pin 1
$\overline{\text{PWDN}}$	5G	Digital input	Power-down pin; active low
VCAP1	5H	—	Analog bypass capacitor; connect 22μF capacitor to AVSS
AVDD	6A	Supply	Analog supply
AVDD	6B	Supply	Analog supply
AVDD	6C	Supply	Analog supply
$\overline{\text{DRDY}}$	6D	Digital output	Data ready; active low
GPIO3	6E	Digital input/output	General purpose input/output pin 3
DAISY_IN(2)	6F	Digital input	Daisy-chain input; if not used, short to DGND.
$\overline{\text{RESET}}$	6G	Digital input	System-reset pin; active low
VCAP2	6H	—	Analog bypass capacitor; connect 1μF capacitor to AVSS
AVDD1	7A	Supply	Analog supply for charge pump
VCAP3	7B	—	Analog bypass capacitor; internally generated AVDD + 1.9V; connect 1μF capacitor to AVSS
DGND	7C	Supply	Digital ground
DGND	7D	Supply	Digital/IO ground
GPIO2	7E	Digital input/output	General-purpose input/output pin 2
$\overline{\text{CS}}$	7F	Digital input	SPI chip select; active low
START	7G	Digital input	Start conversion
DGND/XIN	7H	Supply	Digital ground
AVSS1	8A	Supply	Analog ground for charge pump

PIN	POSITION	TYPE	DESCRIPTION
CLKSEL	8B	Digital input	Master clock select
DVDD	8C	Supply	Digital power supply
DVDD	8D	Supply	Digital power supply, I/O power supply
DOUT	8E	Digital output	SPI data output
SCLK	8F	Digital input	SPI clock
CLK	8G	Digital input/output	External Master clock input or internal clock output
DIN	8H	Digital input	SPI data input

Note 1: Connect unused pins to AVDD.
Note 2: When DAISY_IN is not used, tie to logic 0.

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the AFE95x.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Power Supply Voltage	AVDD to AVSS	–0.3	7.0	V
	AVSS to DGND	–3	0.2	
	DVDD to DGND	–0.3	5.0	
	VREFP input to AVSS	AVSS – 0.3	AVDD + 0.3	
Analog Input Voltage		AVSS – 0.3	AVDD + 0.3	
Digital Input Voltage		DGND – 0.3	DVDD + 0.3	
Digital Output voltage		DGND – 0.3	DVDD + 0.3	
Input Current	Momentary		100	mA
	Continuous		10	
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–60	150	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the AFE95x.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the AFE95x.

Table 6. Recommended Operating Conditions

PARAMETER		SYMBOL	MIN	NOM	MAX	UNITS
POWER SUPPLY						
Analog Power Supply (AVDD – AVSS)			2.7	3	5.5	V
Digital Power Supply (DVDD)			1.65	1.8	3.6	V
AVDD – DVDD			–2.1		3.6	V
ANALOG INPUTS						
Full-Scale Differential Input Voltage Range (AINP – AINN)				$\pm V_{REF}$ / Gain		V
Common-Mode Input Voltage			See the INPUT COMMON-MODE RANGE section			
VOLTAGE REFERENCE INPUTS						
Differential Reference Voltage	3V Supply V_{REF} = (VREFP – VREFN)			2.5		V
	5V Supply V_{REF} = (VREFP – VREFN)			4		V
Negative Input (VREFN)				AVSS		V
Positive Input (VREFP)				AVSS + 2.5		V
CLOCK INPUT						
External Clock Input Frequency	CLKSEL Pin = 0		1.94	2.048	2.25	MHz
DIGITAL INPUTS						
Input Voltage			DGND		DVDD	V
TEMPERATURE RANGE						
Operating Temperature Range	Commercial Grade		0		85	°C
	Industrial Grade		–40		125	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the AFE95x.

Table 7. Thermal Information

PARAMETER	SYMBOL	BGA-64	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	29.4	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	10.4	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	0.2	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	10.27	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	9.2	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	7.53	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of the AFE95x. Minimum and maximum specifications apply for T_A = 0°C to 85°C devices. Typical specifications at T_A = 25°C. All specifications at DVDD = 1.8V, AVDD – AVSS = 3V(1), V_{REF} = 2.4V, external f_{CLK} = 2.048MHz, data rate = 500SPS, HR mode(2), and gain = 6, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Input Capacitance				20		pF
Input Bias Current		T_A = 25°C, input = 1.5V		100		pA
DC Input Impedance		No lead-off		5000		MΩ
		Current source lead-off detection		500		MΩ
PGA PERFORMANCE						
Gain Settings			1, 2, 3, 4, 6, 8, 12, 24			
Bandwidth			See Table 21			
ADC PERFORMANCE						
Resolution		Data rates up to 8kSPS, no missing codes	24			Bits
		16kSPS data rate	19			Bits
		32kSPS data rate	17			Bits
		64kSPS data rate	16			Bits
Data Rate		f_{CLK} = 2.048MHz, HS mode	1000		64000	SPS
		f_{CLK} = 2.048MHz, HR mode	500		32000	SPS
		f_{CLK} = 2.048MHz, LP mode	250		16000	SPS
		f_{CLK} = 2.048MHz, ULP mode	125		8000	SPS
DC CHANNEL PERFORMANCE						
Input-Referred Noise		Gain = 6(3), 10 seconds of data		5		μV_{PP}
		Gain = 6, 256 points, 0.5 seconds of data		4	7	μV_{PP}
		Gain settings ≠ 6, data rates ≠ 500SPS	See NOISE MEASUREMENTS section			
Integral Nonlinearity(4)		Full-scale with gain = 6, best fit		6		ppm
		Full-scale with gain = 6, best fit, channel 1		8		ppm
Offset Error				±20		µV
Offset Error		After calibration		±2		µV
Offset Error Drift				5		nV/°C
Gain Error		Excluding voltage reference error		±0.2	±0.5	% of FS
		Gain= 1 and 4, excluding voltage reference error		±1		% of FS
Gain Drift		Excluding voltage reference drift		3		ppm/°C
Gain Match between Channels				0.3		% of FS
AC CHANNEL PERFORMANCE						
Common-Mode Rejection Ratio	CMRR	f_{CM} = 50Hz, 60Hz(5)	–108	–123		dB
Power-supply Rejection Ratio	PSRR	f_{PS} = 50Hz, 60Hz		90		dB
Crosstalk		f_{IN} = 50Hz, 60Hz		–140		dB
Signal-to-Noise Ratio	SNR	f_{IN} = 10Hz input, gain = 6		110		dB
Total Harmonic Distortion(4)	THD	10Hz, –0.5dB FS		–108		dB
		Channel 1, 10Hz, –0.5dB FS		–95		dB
		100Hz, –0.5dB FS(6)		–120		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Channel 1, 100Hz, –0.5dB FS(6)		–96.8		dB
		Channel 1, 100Hz, –20dB FS(6)		–108.4		dB
DIGITAL FILTER						
–3dB Bandwidth				0.262 f_{DR}		Hz
Digital Filter Settling		Full setting		4		Conversions
RIGHT LEG DRIVE (RLD) AMPLIFIER AND PACE AMPLIFIERS						
RLD Integrated Noise		BW = 150Hz		0.9		μV_{RMS}
Pace Integrated Noise		BW = 8kHz		20		μV_{RMS}
Pace-Amplifier Crosstalk		Crosstalk between pace amplifiers		60		dB
Gain Bandwidth Product		50kΩ || 10pF load, gain = 1		100		kHz
Slew Rate		50kΩ || 10pF load, gain = 1		0.25		V/µs
Pace and RLD Amplifier Drive Strength		Short circuit to GND (AVDD = 3V)		270		µA
		Short circuit to supply (AVDD = 3V)		550		µA
		Short circuit to GND (AVDD = 5V)		490		µA
		Short circuit to supply (AVDD = 5V)		810		µA
Pace and RLD Current		Peak swing (AVSS + 0.3V to AVDD + 0.3V) at AVDD = 3V		50		µA
		Peak swing (AVSS + 0.3V to AVDD + 0.3V) at AVDD = 5V		75		µA
Pace-Amplifier Output Resistance				100		Ω
Total Harmonic Distortion		f_{IN} = 100Hz, gain = 1		–70		dB
Common-Mode Input Range			AVSS + 0.7		AVDD – 0.3	V
Common-Mode Resistor Matching		Internal 200kΩ resistor matching		0.1%		
Short-Circuit Current				±0.25		mA
Quiescent Power Consumption		Either RLD or pace amplifier		12		µA
WILSON CENTRAL TERMINAL (WCT) AMPLIFIER						
Integrated Noise		BW = 150Hz	See Table 22			nV/√Hz
Gain Bandwidth Product			See Table 22			kHz
Slew Rate			See Table 22			V/s
Offset				±500		µV
Total Harmonic Distortion		f_{IN} = 100Hz		90		dB
Common-Mode Input Range			AVSS + 0.3		AVDD – 0.3	V
Short-Circuit Current		Through internal 30kΩ resistor		±0.25		mA
Quiescent Power Consumption			See Table 22			µA
LEAD-OFF DETECT						
Frequency		See Table 33 for settings		0, f_{DR} / 4		kHz
DC Current		See Table 33 for settings	5, 10, 15, 20			nA
AC Current			2.5, 5, 10, 20, 40			nA
Current Accuracy				±20%		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator Threshold Accuracy				±30		mV
RESPIRATION						
Frequency		Internal source		32, 43, 64		kHz
		External source	32	43	64	kHz
Phase Shift		See Table 33 for settings	0	112.5	168.75	Degrees
Impedance Range		I_{RESP} = 30µA			10	kΩ
Impedance Measurement Noise		0.05Hz to 2Hz brick wall filter, 32kHz modulation clock, phase = 112.5, I_{RESP} = 30µA with 2kΩ baseline load, gain = 4		20		$mΩ_{PP}$
Modulator Current		Internal reference, signal path = 82kΩ, baseline = 2.21kΩ		29		µA
EXTERNAL REFERENCE						
Input Impedance				13.6		kΩ
INTERNAL REFERENCE						
Output Voltage		Register bit CONFIG3.VREF_4V = 0, AVDD ≥ 2.7V		2.4		V
		Register bit CONFIG3.VREF_4V = 1, AVDD ≥ 4.4V		4		V
V_{REF} Accuracy				±0.03%		
Internal Reference Drift		T_A = 25°C		35		ppm/°C
		Industrial grade, –40°C to 85°C		8		ppm
Start-up Time				30		ms
SYSTEM MONITORS						
Analog Supply Reading Error				2%		
Digital Supply Reading Error				2%		
Device Wakeup		From power up to $\overline{DRDY}$ low		150		ms
		STANDBY mode		9		ms
Temperature Sensor Reading, Voltage		T_A = 25°C		143.54		mV
Temperature Sensor Reading, Coefficient				337.64		µV/°C
Test Signal Frequency		See Table 33 for settings		f_{CLK} / 2^{21}, f_{CLK} / 2^{20}		Hz
Test Signal Voltage		See Table 33 for settings		±1, ±2, ±10		mV
Test Signal Accuracy				±2%		
CLOCK						
Internal Oscillator Clock Frequency		Nominal frequency		2.048		MHz
Internal Clock Accuracy		T_A = 25°C			±0.5%	
		0°C ≤ T_A ≤ 70°C			±2%	
		–40°C ≤ T_A ≤ 85°C, industrial grade versions only			±2.5%	
Internal Oscillator Start-up Time					5	µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Oscillator Power Consumption				100		µW
DIGITAL INPUT/OUTPUT (DVDD = 1.65V to 3.6V)						
High-Level Input Voltage	V_{IH}		0.8 DVDD		DVDD + 0.1	V
Low-Level Input Voltage	V_{IL}		–0.1		0.2 DVDD	V
High-Level Output Voltage	V_{OH}	I_{OH} = –500µA	DVDD – 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 500µA			0.4	V
Input Current	I_{IN}	0V < VDigitalInput < DVDD	–10		10	µA
POWER SUPPLY (RLD, WCT, AND PACE AMPLIFIERS TURNED OFF)						
AVDD Current	I_{AVDD}	AFE959, AVDD – AVSS = 3V, HS mode		3		mA
		AFE958, AVDD – AVSS = 3V, HR mode		5		mA
		AFE958, AVDD – AVSS = 3V, LP mode(2)		1.5		mA
		AFE959, AVDD – AVSS = 3V, ULP mode(2)		2.1		mA
		AFE959, AVDD – AVSS = 5V, HS mode		3.4		mA
		AFE958, AVDD – AVSS = 5V, HR mode		5.7		mA
		AFE958, AVDD – AVSS = 5V, LP mode		1.6		mA
		AFE959, AVDD – AVSS = 5V, ULP mode(2)		2.3		mA
DVDD Current	I_{DVDD}	AFE959, DVDD = 1.8V, HS mode		0.2		mA
		AFE958, DVDD = 1.8V, HR mode		0.2		mA
		AFE958, DVDD = 1.8V, LP mode		0.12		mA
		AFE959, DVDD = 1.8V, ULP mode(2)		0.15		mA
		DVDD = 3V, HR mode		0.37		mA
		DVDD = 3V, LP mode		0.27		mA
Power Dissipation		AFE954, AVDD – AVSS = 3V, HR mode		5.7		mW
		AFE954, AVDD – AVSS = 3V, LP mode (250SPS)		4		mW
		AFE956, AVDD – AVSS = 3V, HR mode		7.5		mW
		AFE956, AVDD – AVSS = 3V, LP mode (250SPS)		5.3		mW
		AFE958, AVDD – AVSS = 3V, HR mode		9.4		mW
		AFE958, AVDD – AVSS = 3V, LP mode (250SPS)		6.5		mW
		AFE954, AVDD – AVSS = 5V, HR mode		11.3		mW
		AFE954, AVDD – AVSS = 5V, LP mode (250SPS)		8.3		mW
		AFE956, AVDD – AVSS = 5V, HR mode		14.7		mW
		AFE956, AVDD – AVSS = 5V, LP mode (250SPS)		10		mW
		AFE958, AVDD – AVSS = 5V, HR mode		18.2		mW
		AFE958, AVDD – AVSS = 5V, LP mode (250SPS)		12.5		mW
Power-Down		AVDD – AVSS = 3V		10		µW
		AVDD – AVSS = 5V		20		µW
Standby Mode		AVDD – AVSS = 3V		2		mW
		AVDD – AVSS = 5V		4		mW
Quiescent Channel Power		AVDD – AVSS = 3V, PGA + ADC		818		µW
		AVDD – AVSS = 5V, PGA + ADC		1.5		mW

Note 1: Performance is applicable for 5V operation as well. Production testing for limits is performed at 3V.
Note 2: LP mode = Low-power mode.

Note 3: Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.
Note 4: The presence of internal demodulation circuitry on channel 1 causes degradation of INL and THD. The effect is pronounced for full-scale signals and is less for small ECG-type signals.
Note 5: CMRR is measured with a common-mode signal of AVSS + 0.3V to AVDD – 0.3V. The values indicated are the maximum of the eight channels.
Note 6: Harmonics above the second harmonic are attenuated by the digital filter.

5.6 TIMING REQUIREMENTS: SERIAL INTERFACE

Table 9 lists the timing requirements (2.7V ≤ IOVDD ≤ 3.6V). T_A = –40°C to +85°C, unless otherwise noted. Load on D_{OUT} = 20pF || 100kΩ.

Table 9. Timing Requirements (2.7V ≤ IOVDD ≤ 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Master Clock Period	t_{CLK}		414		514	ns
$\overline{CS}$ Low to First SCLK, Setup Time	t_{CSSC}		6			ns
SCLK Period	t_{SCLK}		50			ns
SCLK Pulse Width, High and Low	$t_{SPWH, L}$		15			ns
DIN Valid to SCLK Falling Edge: Setup Time	t_{DIST}		10			ns
Valid DIN after SCLK Falling Edge: Hold Time	t_{DIHD}		10			ns
$\overline{CS}$ High Pulse	t_{CSH}		2			t_{CLK}
Eighth SCLK Falling Edge to $\overline{CS}$ High	t_{SCCS}		4			t_{CLK}
Command Decode Time	$t_{SDECODE}$		4			t_{CLK}
DAISY_IN Valid to SCLK Falling Edge: Setup Time	$t_{DISCK2ST}$		10			ns
DAISY_IN Valid after SCLK Falling Edge: Hold Time	$t_{DISCK2HT}$		10			ns

Table 10 lists the timing requirements (1.65V ≤ IOVDD ≤ 2.7V). T_A = –40°C to +85°C, unless otherwise noted. Load on D_{OUT} = 20pF || 100kΩ.

Table 10. Timing Requirements (1.65V ≤ IOVDD ≤ 2.7V)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Master Clock Period	t_{CLK}		414		514	ns
$\overline{CS}$ Low to First SCLK, Setup Time	t_{CSSC}		17			ns
SCLK Period	t_{SCLK}		66.6			ns
SCLK Pulse Width, High and Low	$t_{SPWH, L}$		25			ns
DIN Valid to SCLK Falling Edge: Setup Time	t_{DIST}		10			ns
Valid DIN after SCLK Falling Edge: Hold Time	t_{DIHD}		11			ns
$\overline{CS}$ High Pulse	t_{CSH}		2			t_{CLK}
Eighth SCLK Falling Edge to $\overline{CS}$ High	t_{SCCS}		4			t_{CLK}
Command Decode Time	$t_{SDECODE}$		4			t_{CLK}
DAISY_IN Valid to SCLK Falling Edge: Setup Time	$t_{DISCK2ST}$		10			ns
DAISY_IN Valid after SCLK Falling Edge: Hold Time	$t_{DISCK2HT}$		10			ns

5.7 SWITCHING CHARACTERISTICS: SERIAL INTERFACE

Table 11 lists the switching characteristics (2.7V ≤ DVDD ≤ 3.6V). T_A = –40°C to +85°C, unless otherwise noted. Load on D_{OUT} = 20pF || 100kΩ.

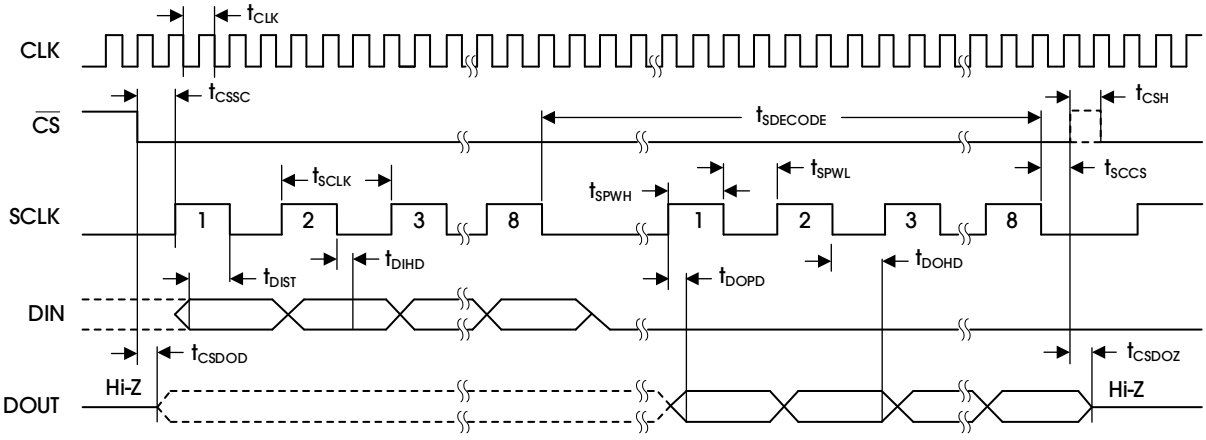
Table 11. Switching Characteristics (2.7V ≤ DVDD ≤ 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
SCLK Falling Edge to Invalid DOUT: Hold Time	t_{DOHD}		10			ns
SCLK Rising Edge to DOUT Valid: Setup Time	t_{DOPD}				17	ns
$\overline{CS}$ Low to DOUT Driven	t_{CSDOD}		10			ns
$\overline{CS}$ High to DOUT Hi-Z	t_{CSDOZ}				10	ns

Table 12 lists the switching characteristics (1.65V ≤ DVDD ≤ 2.7V). T_A = –40°C to +85°C, unless otherwise noted. Load on D_{OUT} = 20pF || 100kΩ.

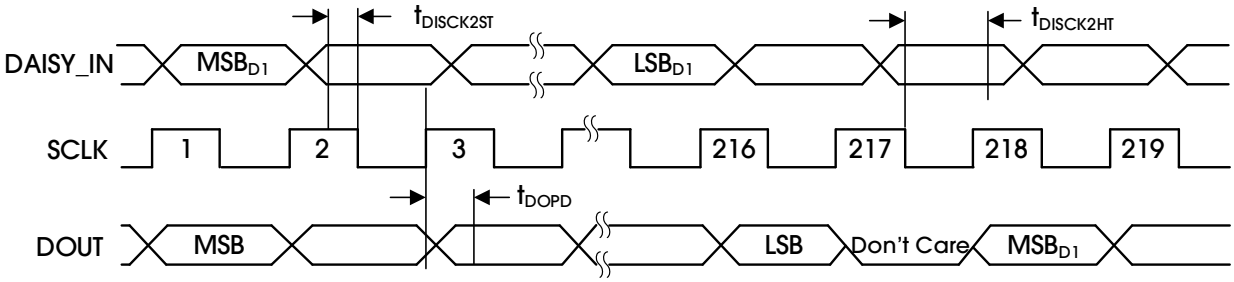
Table 12. Switching Characteristics (1.65V ≤ DVDD ≤ 2.7V)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
SCLK Falling Edge to Invalid DOUT: Hold Time	t_{DOHD}		10			ns
SCLK Rising Edge to DOUT Valid: Setup Time	t_{DOPD}				32	ns
$\overline{CS}$ Low to DOUT Driven	t_{CSDOD}		20			ns
$\overline{CS}$ High to DOUT Hi-Z	t_{CSDOZ}				20	ns



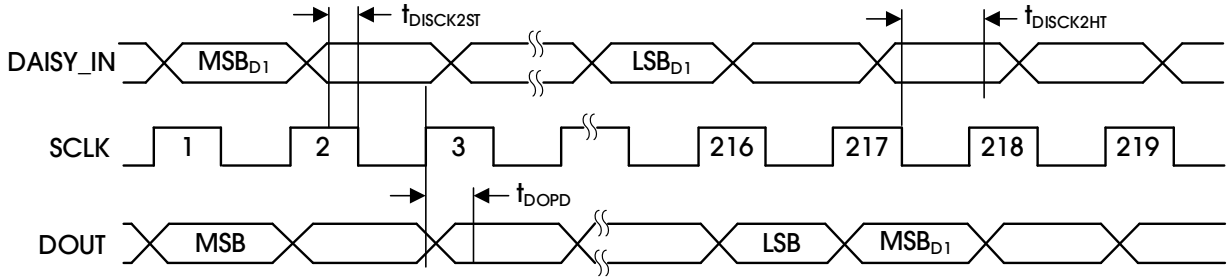
NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 2. Serial Interface Timing



NOTE: Daisy-chain timing shown for eight-channel devices.

Figure 3. Daisy-Chain Interface Timing When DAISY_ONE_BIT is '1'



NOTE: Daisy-chain timing shown for eight-channel devices.

Figure 4. Daisy-Chain Interface Timing When DAISY_ONE_BIT is '0'

6. TYPICAL CHARACTERISTICS

T_A = 25°C, AVDD = 3V, AVSS = 0V, DVDD = 1.8V, internal VREFP = 2.4V, VREFN = AVSS, external clock = 2.048MHz, data rate = 500SPS, high-resolution mode, and gain = 6, unless otherwise noted.

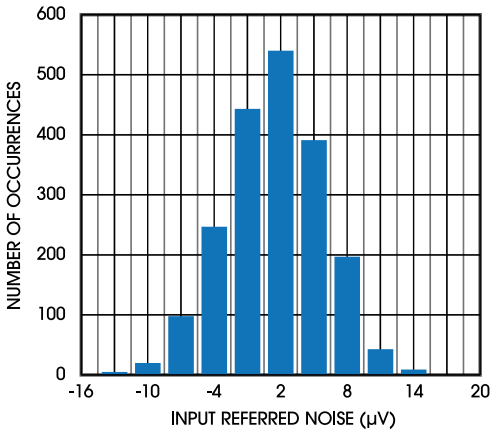


Figure 5. Noise Distribution

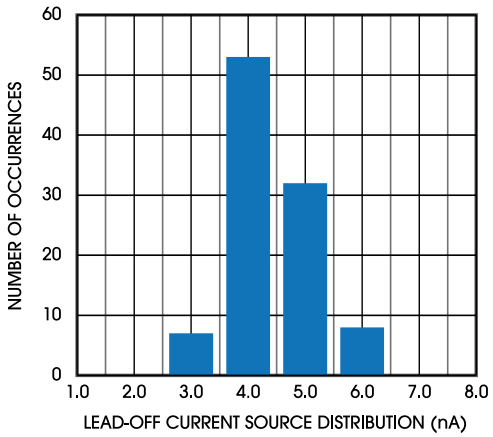


Figure 6. Lead-off Current Source Accuracy Distribution

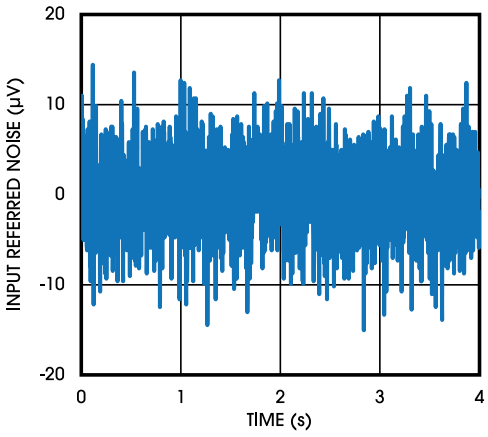


Figure 7. Input Referred Noise

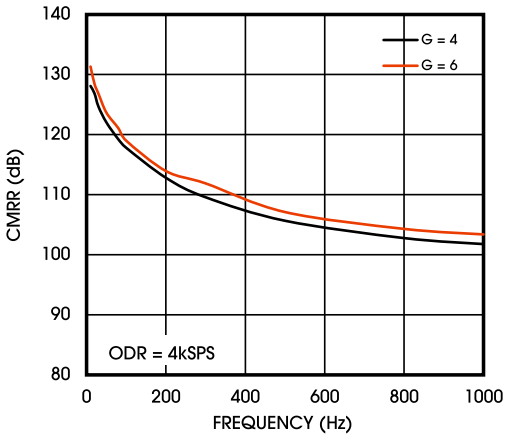


Figure 8. CMRR vs. Frequency

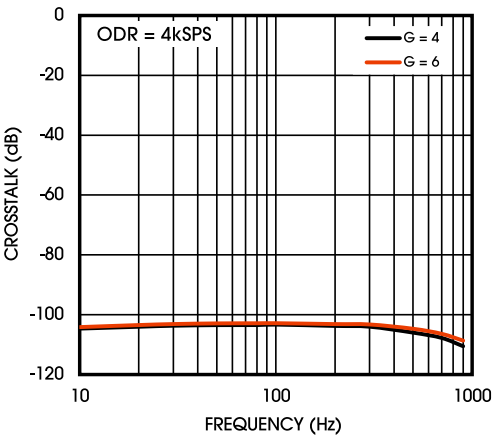


Figure 9. THD vs. Frequency

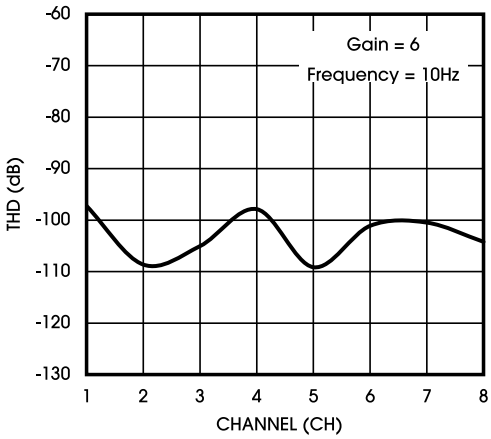


Figure 10. THD vs. Channel

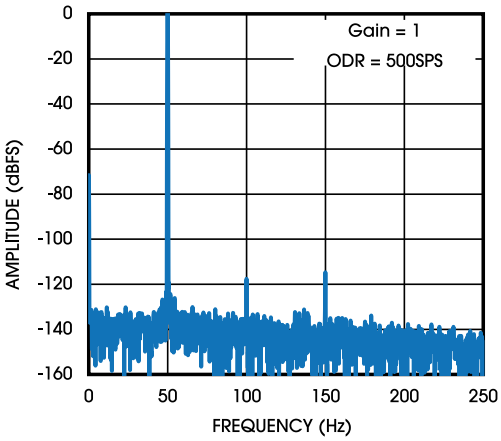


Figure 11. THD Plot (G = 1)

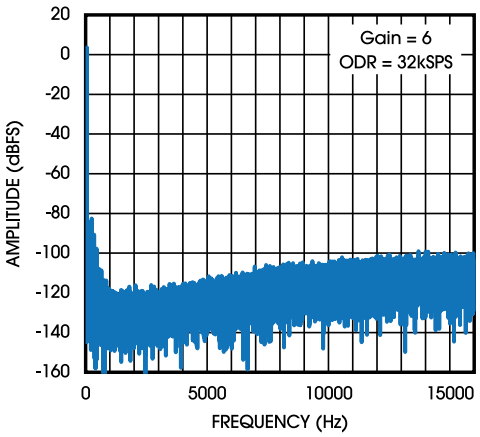


Figure 12. THD Plot (G = 6)

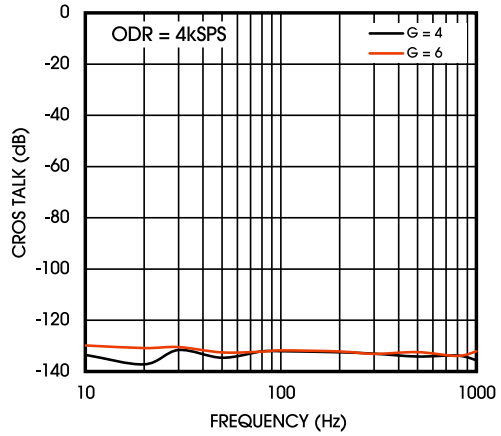


Figure 13. Crosstalk vs. Frequency

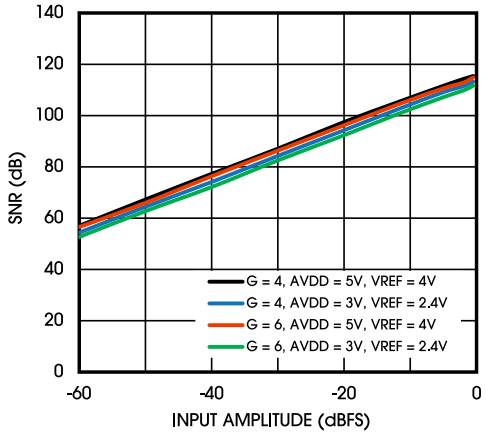


Figure 14. SNR vs. Input Amplitude

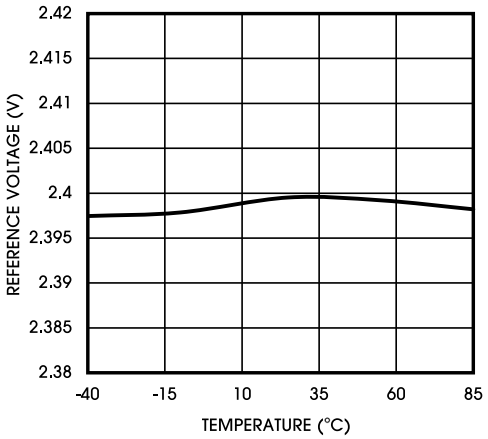


Figure 15. Internal Reference vs. Temperature

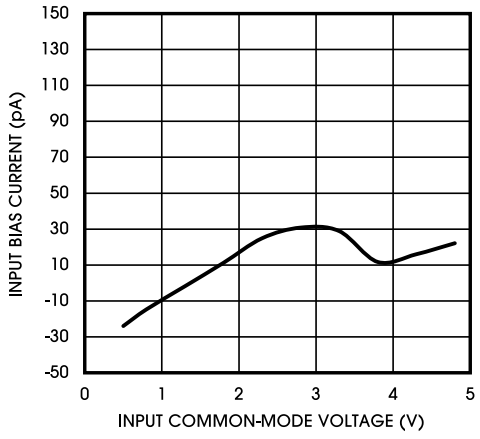


Figure 16. Leakage Current vs. Input Common-Mode Voltage

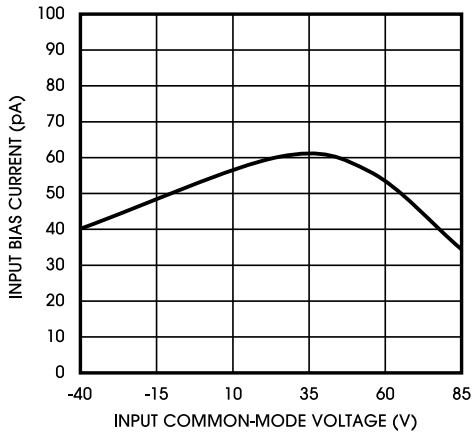


Figure 17. Leakage Current vs. Temperature

Figure 18. Offset vs. Gain

7. 参数测量信息

7.1 噪声测量

可通过调整数据速率和 PGA 设置来优化 AFE95x 噪声性能。降低数据速率可增加平均值，噪声也会相应地降低。增加 PGA 值可降低输入参考噪声。在测量低水平生物电势信号时，这种方法降低噪声的水平十分显著。Table 13 和 Table 14 分别总结了使用 3V 模拟电源时在高分辨率(HR)模式和低功耗(LP)模式下 AFE95x 的噪声性能。Table 15 和 Table 16 分别总结了使用 5V 模拟电源时在 HR 模式和 LP 模式下 AFE95x 的噪声性能。这些数据代表 T_A = 25°C 时的典型噪声性能。表格展示的数据是在输入短路的情况下对来自多个器件的测量读数求平均值的结果。至少使用了 1000 个连续读数来计算每个读数的 RMS 和峰峰值噪声。对于两个最高数据速率，噪声受到 ADC 的量化噪声的限制，未按高斯分布排列。因此，RMS 噪声与峰峰值噪声之间的比率约为 10。对于较低的数据速率，该比率约为 6.6。

Table 13 至 Table 20 展示了使用内部基准进行测量的结果。这些数据还代表使用低噪声外部基准时的 AFE95x 噪声性能。

Table 13. Input-Referred Noise μV_{PP} in High-Resolution Mode, 3V Analog Supply and 2.4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	32000	8398	2804.05	1405.02	946.63	696.53	468.34	346.02	226.69	112.10
001	16000	4193	716.56	358.67	227.38	169.61	106.60	80.42	52.55	31.10
010	8000	2096	167.17	81.92	55.56	40.87	29.32	23.67	19.34	17.28
011	4000	1048	74.04	37.47	27.53	21.25	16.15	14.28	12.54	11.33
100	2000	524	52.68	27.28	18.49	15.09	11.71	9.92	9.03	8.00
101	1000	262	37.89	19.83	12.59	10.48	8.18	6.96	6.31	5.58
110	500	131	24.91	12.44	8.33	7.21	5.23	4.86	4.21	3.79

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 14. Input-Referred Noise μV_{PP} in Low-Power Mode, 3V Analog Supply and 2.4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	16000	4193	2762.17	1393.05	932.69	701.01	454.39	338.55	214.74	101.64
001	8000	2096	727.78	379.95	238.62	177.83	116.93	86.40	53.42	28.98
010	4000	1048	168.02	87.57	56.12	42.52	28.90	22.53	16.83	13.73
011	2000	524	78.13	43.36	28.25	21.78	15.91	13.01	10.78	9.07
100	1000	262	54.28	28.37	19.83	15.69	11.51	9.39	7.65	6.62
101	500	131	37.23	20.08	13.50	10.51	7.21	6.28	5.07	4.30
110	250	65	23.26	12.96	8.91	6.93	4.95	4.18	3.33	2.90

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 15. Input-Referred Noise μV_{PP} in High-Resolution Mode, 5V Analog Supply and 4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	32000	8398	4663.47	2351.66	1584.38	1173.33	777.24	576.70	389.45	188.50
001	16000	4193	1254.08	631.42	410.14	305.41	189.71	136.20	85.93	42.96
010	8000	2096	273.47	130.81	83.21	61.09	42.22	31.85	22.95	16.83
011	4000	1048	112.74	57.56	38.26	29.27	20.05	16.82	13.34	11.33
100	2000	524	73.81	37.53	25.60	20.35	14.41	11.75	9.20	7.66
101	1000	262	48.64	25.48	17.42	13.34	10.21	8.11	6.47	5.37
110	500	131	35.25	17.54	11.72	9.47	6.79	5.42	4.48	3.60

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 16. Input-Referred Noise μV_{PP} in Low-Power Mode, 5V Analog Supply and 4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	16000	4193	4693.34	2321.79	1557.82	1180.81	778.91	569.23	378.66	178.11
001	8000	2096	1276.46	641.36	413.86	304.17	200.71	151.46	94.54	43.64
010	4000	1048	268.94	135.18	89.60	67.78	43.11	33.38	22.13	13.90
011	2000	524	118.80	62.33	41.69	31.34	21.83	16.84	12.62	9.21
100	1000	262	78.34	43.10	28.39	21.32	14.65	11.54	8.66	6.51
101	500	131	52.93	26.84	19.38	14.13	9.72	7.99	6.10	4.25
110	250	65	33.89	18.97	12.31	9.50	6.57	4.80	3.83	2.90

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 17. Input-Referred Noise μV_{RMS} in High-Resolution Mode, 3V Analog Supply and 2.4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	32000	8398	234.50	117.30	78.64	59.20	39.38	29.61	20.08	10.48
001	16000	4193	44.57	22.55	15.16	11.61	8.05	6.36	4.75	3.40
010	8000	2096	14.00	7.33	5.19	4.14	3.19	2.77	2.40	2.13
011	4000	1048	8.51	4.57	3.27	2.65	2.09	1.86	1.65	1.49
100	2000	524	5.98	3.21	2.30	1.86	1.48	1.30	1.17	1.05
101	1000	262	4.25	2.29	1.63	1.32	1.04	0.92	0.82	0.75
110	500	131	3.02	1.60	1.15	0.93	0.74	0.65	0.58	0.53

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 18. Input-Referred Noise μV_{RMS} in Low-Power Mode, 3V Analog Supply and 2.4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	16000	4193	232.83	117.63	78.12	59.11	39.24	29.28	19.64	10.19
001	8000	2096	44.52	22.70	15.28	11.53	7.92	6.10	4.42	2.95
010	4000	1048	14.26	7.70	5.35	4.18	3.05	2.54	2.08	1.73
011	2000	524	8.81	4.86	3.41	2.68	1.98	1.68	1.41	1.21
100	1000	262	6.23	3.42	2.39	1.88	1.40	1.18	1.00	0.85
101	500	131	4.45	2.42	1.69	1.34	0.99	0.84	0.71	0.60
110	250	65	3.13	1.72	1.20	0.94	0.71	0.59	0.49	0.42

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 19. Input-Referred Noise μV_{RMS} in High-Resolution Mode, 5V Analog Supply and 4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	32000	8398	390.05	195.86	130.25	97.74	65.47	49.03	32.71	16.74
001	16000	4193	71.88	36.41	24.25	18.29	12.37	9.46	6.63	4.00
010	8000	2096	19.32	9.93	6.73	5.28	3.82	3.14	2.54	2.08
011	4000	1048	10.76	5.63	3.91	3.08	2.32	1.98	1.66	1.43
100	2000	524	7.59	3.93	2.74	2.15	1.62	1.38	1.17	1.01
101	1000	262	5.45	2.84	1.96	1.54	1.16	0.98	0.83	0.71
110	500	131	3.99	2.02	1.40	1.10	0.82	0.70	0.59	0.50

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

Table 20. Input-Referred Noise μV_{RMS} in Low-Power Mode, 5V Analog Supply and 4V Reference

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12	PGA GAIN = 24
000	16000	4193	390.69	194.56	130.45	97.36	64.82	48.71	32.58	16.58
001	8000	2096	71.57	36.43	24.40	18.30	12.27	9.31	6.40	3.71
010	4000	1048	19.62	10.09	6.97	5.30	3.74	2.98	2.30	1.74
011	2000	524	11.01	5.86	4.02	3.13	2.24	1.84	1.47	1.18
100	1000	262	7.83	4.18	2.87	2.21	1.59	1.30	1.04	0.84
101	500	131	5.66	3.01	2.07	1.59	1.13	0.93	0.74	0.59
110	250	65	4.15	2.19	1.47	1.14	0.81	0.65	0.52	0.42

注：至少使用 1000 个连续读数来计算本表中的 RMS 和峰峰值噪声值。

8. 详细说明

8.1 概述

AFE95x 是具有集成式可编程增益放大器(PGA)的低功耗、多通道、同步采样、24 位 Δ-Σ 模数转换器(ADC)。这些器件包含各种 ECG 专用功能，使其非常适用于可扩展心电图(ECG)、脑电图和肌电图(EMG)应用。当关闭了 ECG 专用电路，这些器件还可用于高性能、多通道数据采集系统。

AFE95x 具有高度可编程的多路复用器(mux)，用于实现温度、电源、输入短路和 RLD 测量。此外，多路复用器允许任何输入电极被编写为患者参照驱动。可以从以下七种设置中选择 PGA 增益：1、2、3、4、6、8、12 或 24。器件中的 ADC 提供 250SPS 至 32kSPS 的数据速率。器件间通信采用与 SPI 兼容的接口。该器件提供四个通用 GPIO 引脚。可使用 START 引脚同步多个器件。

将内部基准编程为 2.4V 或 4V。内部振荡器会产生频率为 2.048MHz 的时钟。多功能右腿驱动(RLD)模块允许选择任何电极组合的平均值来生成患者驱动信号。可通过使用上拉或下拉电阻器或者电流源或电流阱来完成导联脱落检测。还提供内部交流导联脱落检测功能。这些器件支持硬件起搏信号检测和软件起搏信号检测。可使用威尔逊中心端子(WCT)块来生成标准 12 导联 ECG 的 WCT 点。

另外，AFE95x 在通道 1 的信号路径中提供了内部呼吸调制器和解调器电路的选项。

8.2 功能模块框图

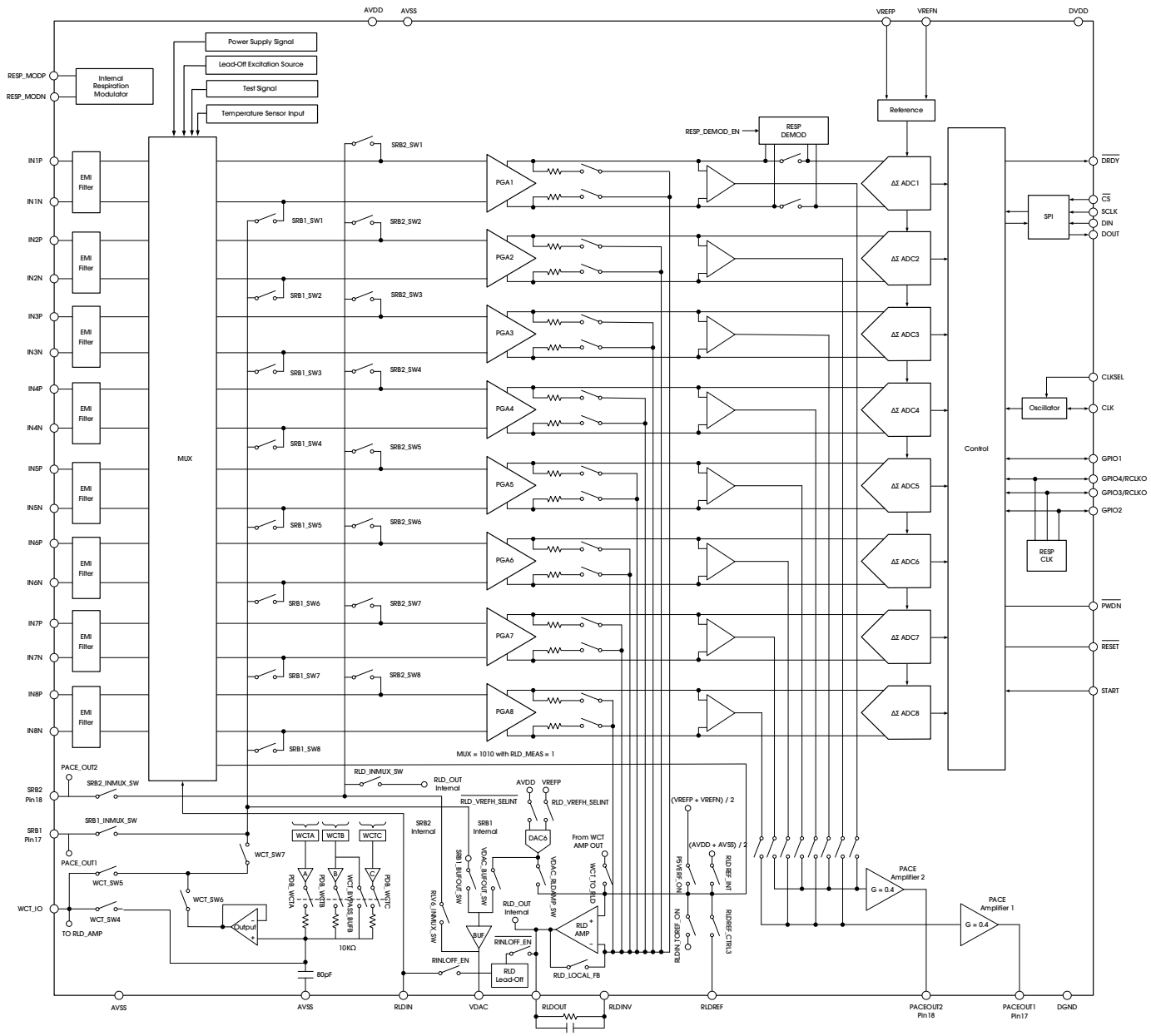


Figure 19. Functional Block Diagram

8.3 特性描述

该部分介绍 AFE95x 内部功能元件的详细信息。首先介绍模拟块，然后介绍数字接口。最后介绍实现 ECG 专用功能的模块。

在整个文档中 f_{CLK} 表示 CLK 引脚上的信号频率，t_{CLK} 表示 CLK 引脚上信号的周期，f_{DR} 表示输出数据速率，t_{DR} 表示输出数据的时长，f_{MOD} 表示调制器输入采样频率。

8.3.1 模拟功能

8.3.1.1 EMI 滤波器

输入端的 RC 滤波器用作所有通道的 EMI 滤波器。–6dB 滤波器带宽大约为 3MHz。

8.3.1.2 模拟输入结构

AFE95x 的模拟输入如 Figure 20 所示。

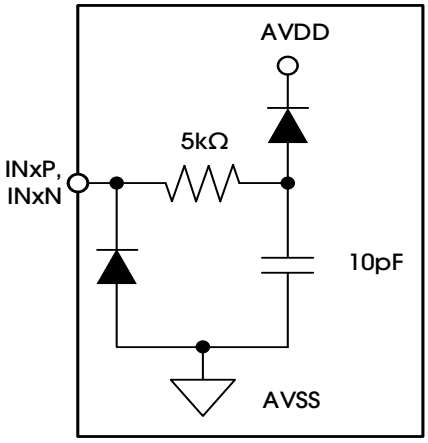
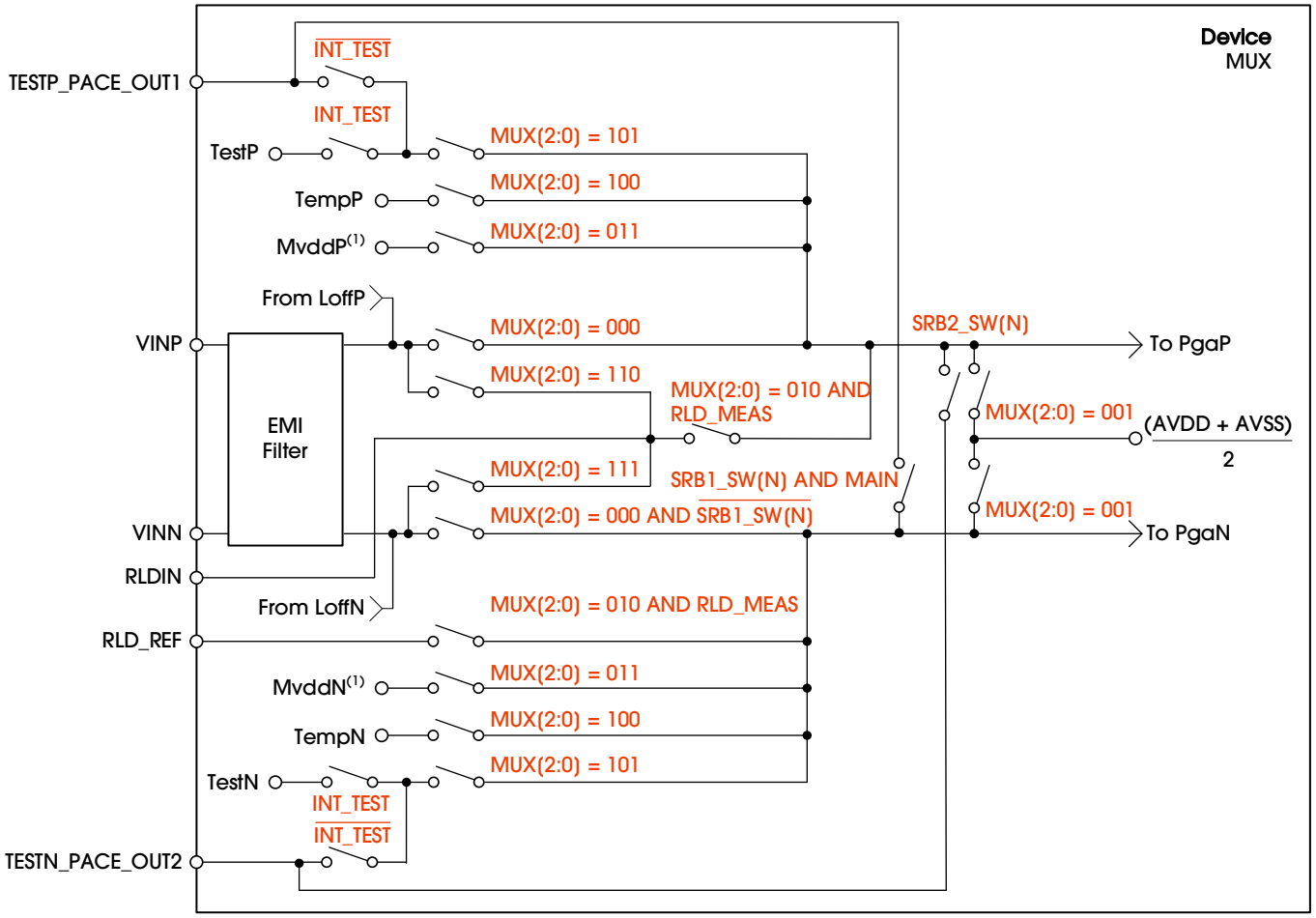


Figure 20. Analog Input Protection Circuit

8.3.1.3 输入多路复用器

AFE95x 的输入端多路复用器非常灵活，它提供了多种可配置的信号切换选择，Figure 21 所示为该设备的一个信号通道的多路复用器。一个设备有八块该模块，每个通道各有一个。TEST_PACE_OUT1、TEST_PACE_OUT2 和 RLD_IN 是每个通道都有的。八个通道都分别有 VINP 和 VINN。这种灵活性可以进行重要的设备和子系统诊断，校准和配置。通过将 1 写入寄存器 CHnSET(2:0)的适当位置和寄存器 CONFIG3 的 RLD_MEAS 位，可选择开关设置。关于心电图特定性能的多路复用器的细节在 INPUT MULTIPLEXER (REROUTING THE RIGHT LEG DRIVE SIGNAL 小节中描述。



(1) MVDD monitor voltage supply depends on channel number; see the Supply Measurements (MVDDP, MVDDN) section.
(2) MAIN is equal to either MUX(2:0) = 000, MUX(2:0) = 110, or MUX(2:0) = 111

Figure 21. Input Multiplexer Block for One Channel

8.3.1.3.1 设备噪声测量

配置寄存器 CHnSET(2:0) = 001，设置共模电压(AVDD – AVSS) / 2 到每个通道的两个输入端，利用该设置可测试设备的固有噪声。

8.3.1.3.2 测试信号(TESTP 和 TESTN)

设置寄存器 CHnSET(2:0) = 101，可提供内部测试信号，用于在电源接通时进行子系统验证。该功能可测试整个信号链。尽管测试信号与 IEC 60601-2-51 规范中描述的 CAL 信号类似，但此功能目的不是用于遵从性测试。

利用寄存器设置来控制测试信号。(查看 CONFIG2: CONFIGURATION REGISTER 2 (ADDRESS = 02H) (RESET = 40H)可获得详细信息)。TEST_AMP 位控制信号放大器，TEST_AMP 位控制所需的频率切换。

测试信号在 TESTP_PACE_OUT1 和 TESTN_PACE_OUT2 引脚上被复用和传输出设备。位寄存器(CONFIG2.INT_TEST = 0)关闭内部测试信号，使其可被外部驱动。该特性使得多个设备可用相同的信号校准。测试信号的功能不能与外部硬件起搏器特性(hardware pace feature)一起使用。(详情参见 EXTERNAL HARDWARE APPROACH 部分内容)。

8.3.1.3.3 辅助差分输入(TESTP_PACE_OUT1, TESTN_PACE_OUT2)

当不使用硬件步长检测(hardware pace detection)时，TESTP_PACE_OUT1 和 TESTN_PACE_OUT2 可被用于多路复用差分输入通道。这些输入可以被用于八个通道的任意一个。通过这些引脚输入的差分信号的性能与正常通道的性能一样。

8.3.1.3.4 温度传感器(TEMPP, TEMPN)

AFE95x 包含一个片上温度传感器。该传感器用两个内部二极管，其中一个二极管的电流密度为另一个的 16 倍，如 Figure 22 所示。二极管电流密度的差异产生的电压的差异与绝对温度成正比。

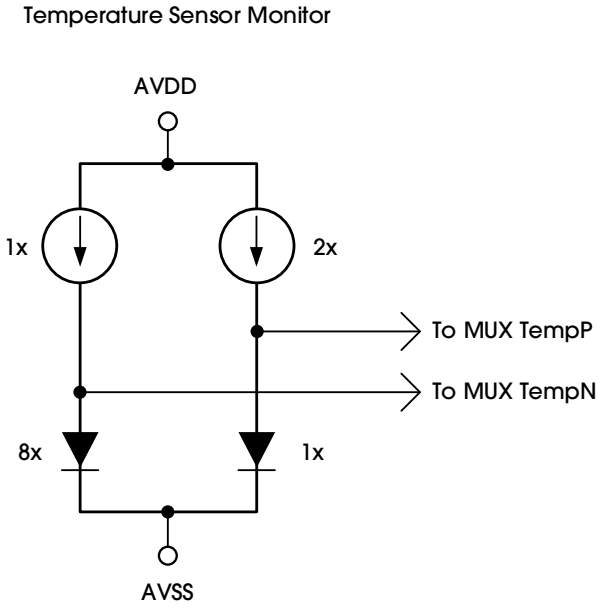


Figure 22. Measurement of the Temperature Sensor in the Input

由于封装印刷电路板(PCB)的热阻低，内部传感器与 PCB 温度很接近。AFE95x 的自热(Self-heating)导致读数比 PCB 周围的温度高。

Equation 1 中的比例因子将温度读数转化为°C。在用这个公式之前，温度读数的单位为微伏 μV。

$$\text{Temperature (°C)} = \left[\frac{\text{Temperature Reading (μV)} - 143,200\text{μV}}{481\text{μV/°C}}\right] + 25\text{°C} \quad (1)$$

8.3.1.3.5 电源测量(MVDDP, MVDDN)

设置 CHnSET(2:0) = 011 将通道输入端设置为不同电源供电。

1. 对于通道 1，2，5，6，7，8，(MVDDP – MVDDN) = (0.5 × (AVDD – AVSS))
2. 对于通道 3，4，(MVDDP – MVDDN) = DVDD / 4

为了避免 PGA 在测量电源时饱和，设置增益为 1。例如，如果 AVDD = 2.5V，AVSS = –2.5V，则测量结果为 2.5V。

8.3.1.3.6 导联激励信号(LOFFP, LOFFN)

导联激励信号在开关前输入多路复用器。检测导联状态的比较器也在开关之前接入多路复用模块。关于导联模块的详细内容参考 LEAD-OFF DETECTION 部分的内容。

8.3.1.3.7 辅助单端输入

RLD_IN 引脚主要用于将右腿驱动(RLD)信号路由到任意电极，以防 RLD 电极脱落。然而，RLD_IN 引脚可以用作多个单端输入通道。参照 RLD_REF 引脚处的电压，可以用八个通道中的任何一个来测量 RLD_IN 引脚处的信号。通过将通道多路复用器设置为 010，并将 CONFIG3 寄存器的 RLD_MEAS 位设置为 1 来完成此测量。

8.3.1.4 模拟输入

AFE95x 的模拟输入是全差分的。假设 PGA = 1，则差分输入(INP – INN)可以为从–VREF~VREF 的跨度。INP 和 INN 的绝对范围必须在 AVSS –0.3V ~ AVDD + 0.3V 之间。模拟输入和数字代码(digital codes)之间的相关性说明见 Table 29。

Figure 23 和 Figure 24 所示为两种驱动 AFE95x 模拟输入的两种通用方法：单端或差分。在差分输入的方法中，INP 和 INN 有 180°的相位差。当输入是单端输入时，INN 输入保持在共模电压(CM)，最好是在中间电源。INP 的输入在相同的共模附近波动，峰峰值幅度在 CM – V_{REF} 到 CM + V_{REF} 之间。但输入是差分时，共模由(INP + INN)/2 给出。INN 和 INP 输入均在 CM + 1/2 V_{REF} 至 CM- 1/2 V_{REF} 之间。为了获得最佳性能，请使用差分输入。

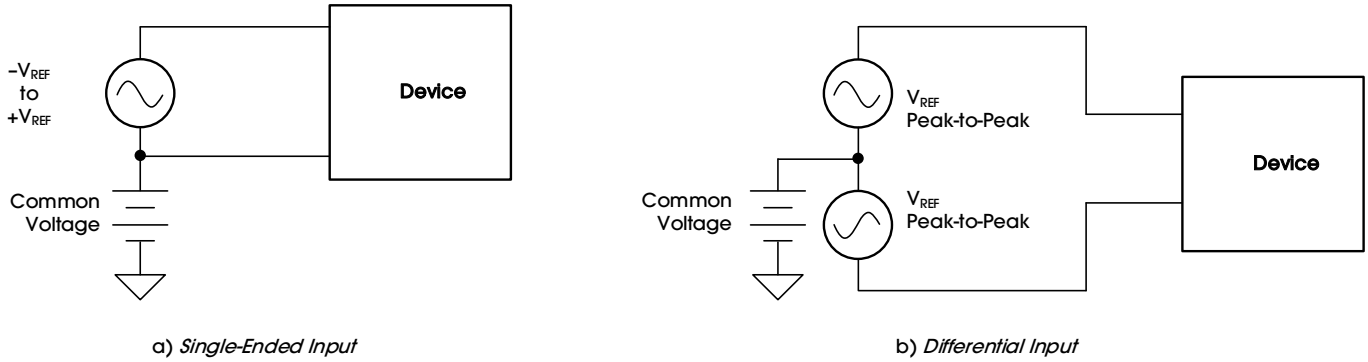
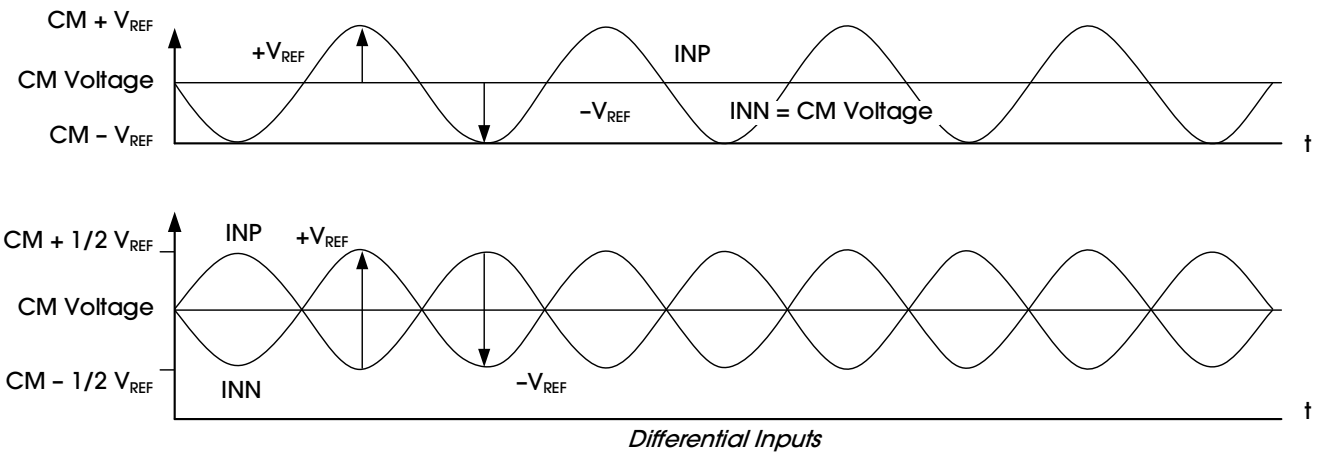


Figure 23. Methods of Driving the AFE95x: Single-Ended or Differential



$$\text{Common-Mode Voltage (Differential Mode)} = \frac{(\text{INP}) + (\text{INN})}{2}, \text{Common-Mode Voltage (Single-Ended Mode)} = \text{INN}$$

Input Range (Differential Mode) = (AINP – AINN) = 2 V_{REF}

Figure 24. Using the AFE95x in Single-Ended and Differential Input Modes

8.3.1.5 PGA 设置和输入范围

PGA 是一个差分输入和差分输出的放大器，如 Figure 25 所示。PGA 有 7 个增益设置(1，2，3，4，6，8，12 和 24),可通过写寄存器 CHnSET 来设置。AFE95x 有 CMOS 输入，因此电流噪声可忽略不计。Table 21 所示为不同增益设置的小信号带宽典型值。

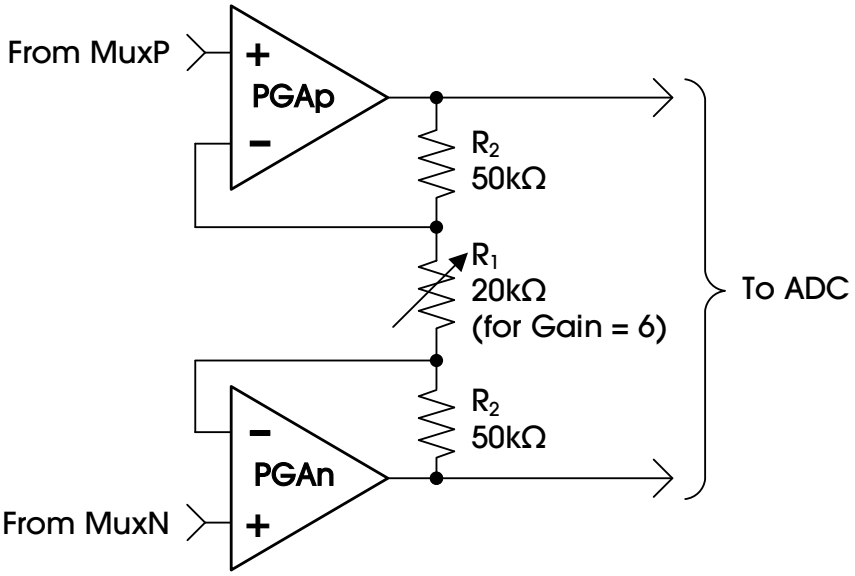


Figure 25. PGA Implementation

Table 21. PGA Gain vs. Small-Signal Bandwidth

GAIN	CHANNEL 1 NOMINAL BANDWIDTH (kHz) AT ROOM TEMPERATURE WITH INTERNAL RESPIRATION DISABLE	CHANNEL1 NOMINAL BANDWIDTH (kHz) AT ROOM TEMPERATURE WITH INTERNAL RESPIRATION ENABLE	CHANNEL 2 TO CHANNEL 8 NOMINAL BANDWIDTH (kHz) AT ROOM TEMPERATURE
1	210	399	210
2	104	198	104
3	70	133	70
4	52	100	52
6	35	66	35
8	25	50	25
12	17	33	17
24	9	17	9

实现 6 倍增益的电阻串有 120kΩ，在差分输入信号存在的情况下，该阻抗提供了一个通过 PGA 输出的电流路径。该电流是在存在差分信号输入的情况下，设备规定的静态电流之外的电流。

8.3.1.5.1 输入共模范围

前端的可用输入共模范围取决与各种参数，包括最大的差分输入信号、电源电压、PGA 增益等。该范围可用 Equation 2 表述。

$$AVDD - 0.2V - \left(\frac{Gain \times VMAX\_DIFF}{2}\right) > CM > AVSS + 0.2V + \left(\frac{Gain \times VMAX\_DIFF}{2}\right) \quad (2)$$

其中：

- V_{MAX_DIFF} = 输入处的最大差分信号
- CM = 共模范围

例如，如果 V_{DD} = 3V，增益 = 6，且 V_{MAX_DIFF} = 350mV，则 1.25V < CM < 1.75V。

8.3.1.5.2 输入差分动态范围

差分信号(INP – INN)范围取决于系统使用的模拟电压和模拟参考电压，可用 Equation 3 表示。

$$Full\text{-}Scale\ Range = \frac{\pm V_{REF}}{Gain} = \frac{2V_{REF}}{Gain} \quad (3)$$

3V 电源(基准为 2.4V，ECG 增益为 6)针对功率进行了优化，差分输入信号约为 300mV。对于更高的动态范围，请使用 5V 电源以及 4V 基准电压(由 CONFIG3 寄存器的 VREF_4V 位进行设置)，以增大差分动态范围。

8.3.1.5.3 ADC DELTA-SIGMA 调制器

AFE95x 的每个通道都有一个 24 位的 Δ-Σ 的 ADC。为低功耗应用优化，该转换器使用一个二阶的调制器。该调制器在高分辨率(HR)模式下采用数据率 $f_{MOD} = f_{CLK} / 4$ 对输入信号进行采样，在低功耗模式下数据率为 $f_{MOD} = f_{CLK} / 8$。就像任何 Δ-Σ 调制器一样，AFE95x 的噪声在 $f_{MOD} / 2$ 时才会发生改变。如 Figure 26 所示。利用片上的数字抽取滤波器(详情见 DIGITAL DECIMATION FILTER 部分)可滤除高频噪声。这些片上抽取滤波器还提供平滑滤波(antialias filtering)。这些 Δ-Σ 转换器的特性大幅度地减少了奈奎斯特 ADC 通常所需的模拟平滑滤波的复杂性。

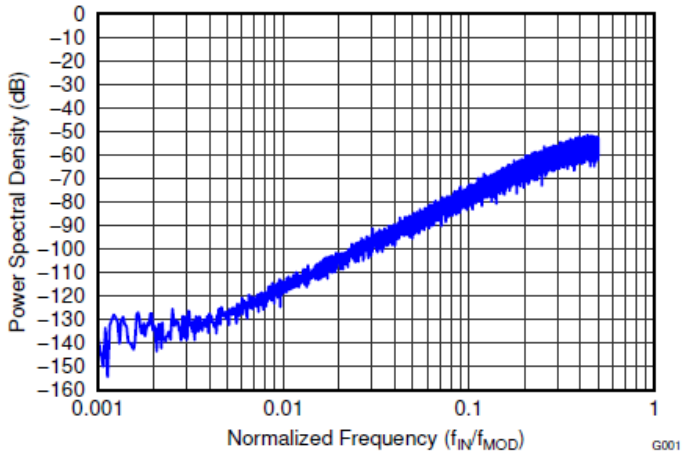
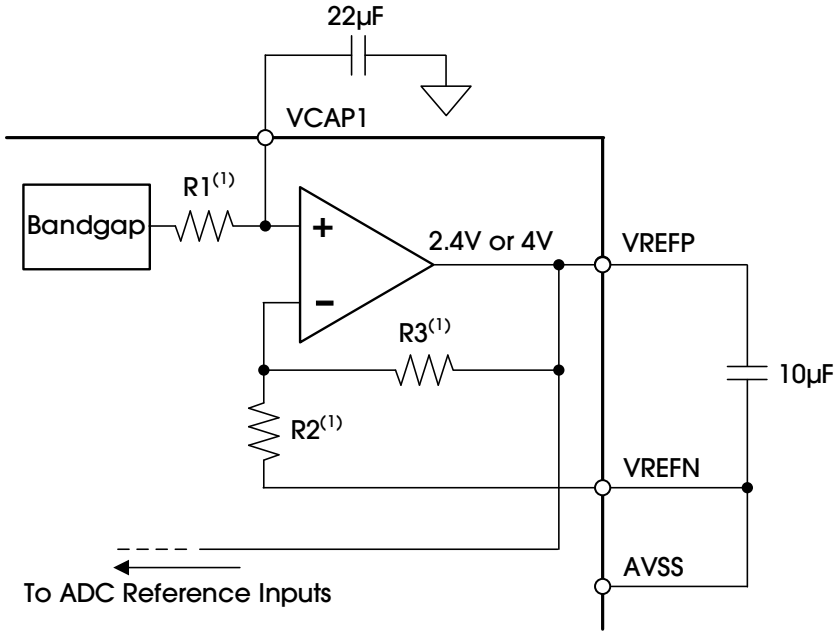


Figure 26. Modulator Noise Spectrum up to 0.5 × f_{MOD}

8.3.1.6 参考

Figure 27 所示为 AFE95X 内部参考的简化模块图。参考电压是相对于(with respect to AVSS) AVSS 产生的。当使用内部参考电压基准时，将 VREFN 连接到 AVSS。



(1) For V_{REF} = 2.4V: R1 = 12.5kΩ, R2 = 25kΩ, and R3 = 25kΩ. For V_{REF} = 4V: R1 = 10.5kΩ, R2 = 15kΩ, and R3 = 35kΩ.

Figure 27. Internal Reference

外部限带(band-limiting)电容器决定了参考噪声贡献的大小。对于高端心电图系统，选择带宽限制在 10Hz 以内的电容值，使参考噪声不为主要的系统噪声。当使用一个 3V 模拟电源时，设置内部参考为 2.4V。当使用 5V 的模拟电源时，通过写寄存器 CONFIG2 的 VREF_4V 位，设置内部参考为 4V。

另外，内部参考电压缓存可以被关闭，VREFP 可由外部提供。Figure 28 所示为典型的外部参考驱动电路。寄存器 CINFIG3 的PD_REFBUF位控制内部参考电压缓存关闭(power down)。默认情况下，设备在外部参考模式下唤醒。

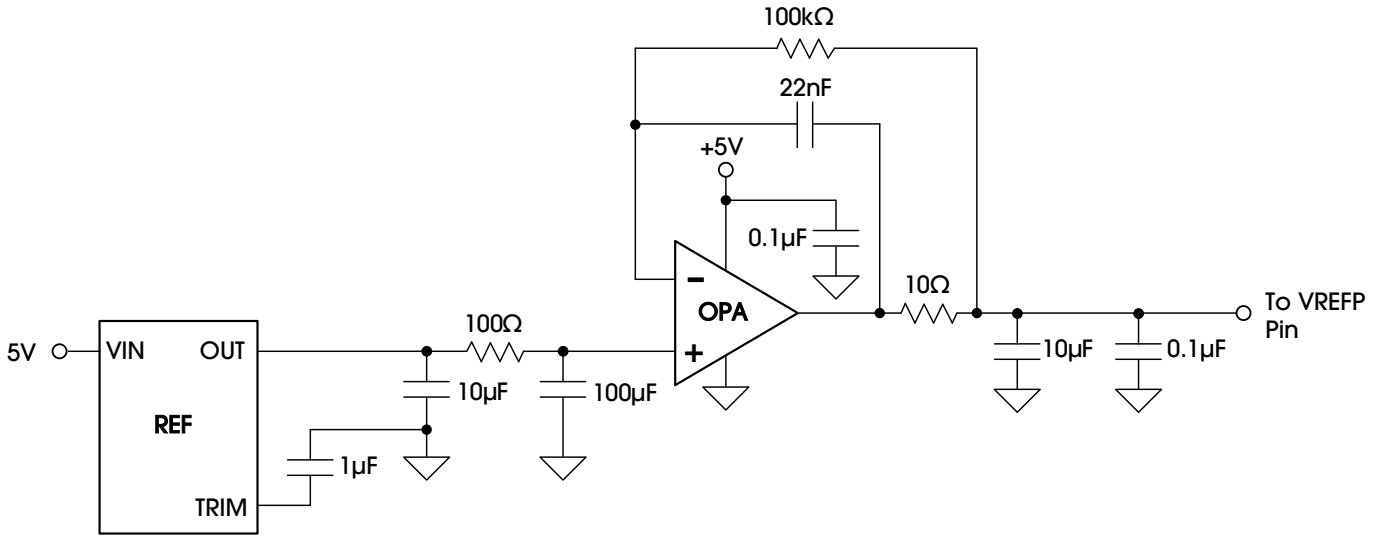
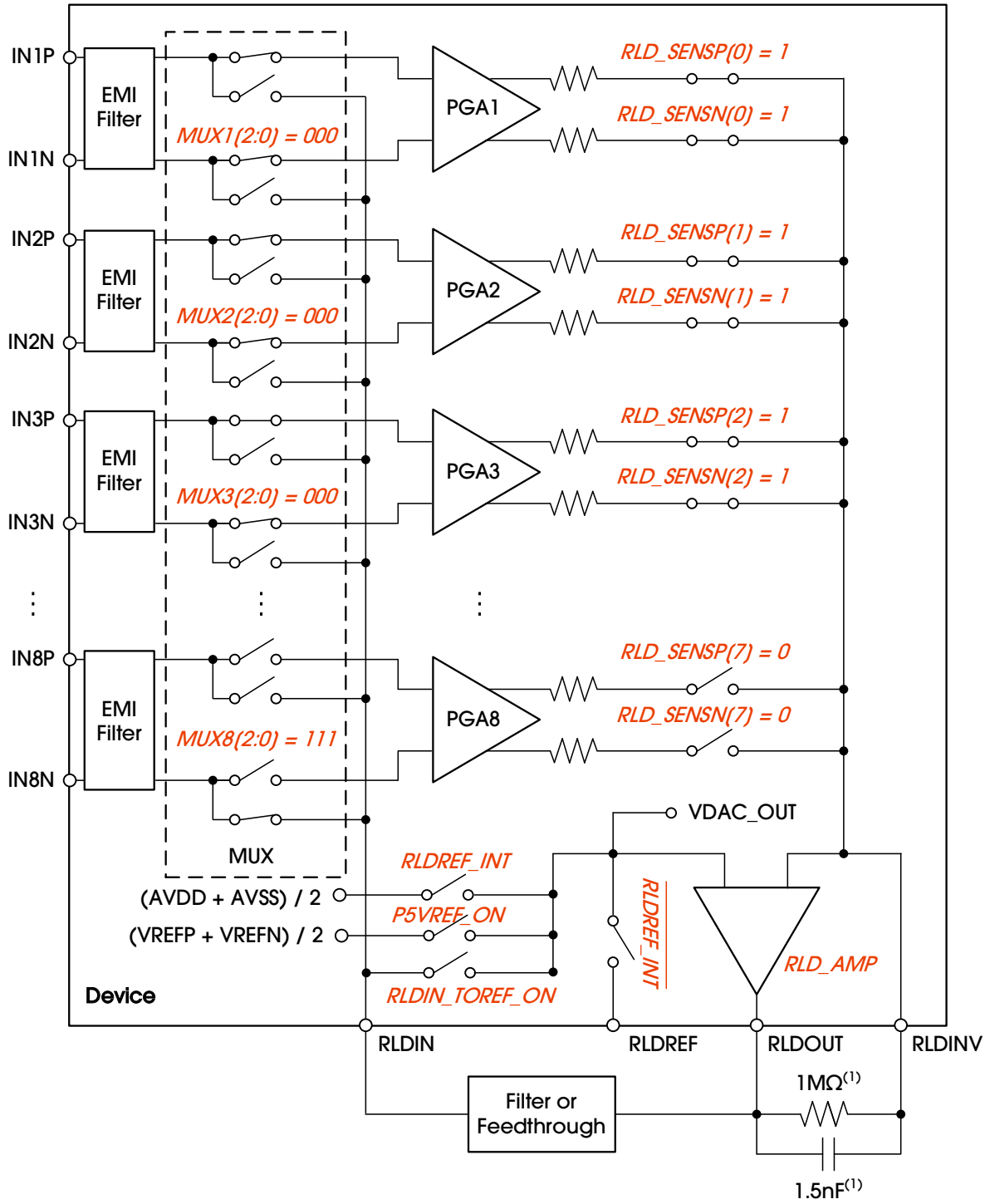


Figure 28. External Reference Driver

8.3.1.7 ECG 特定功能

8.3.1.7.1 输入多路复用器(重新路由右腿驱动信号)

输入多路复用器具有用于右腿驱动信号的心电图特定功能。选择适当的信号作为右腿驱动之后，RLDOUT 引脚的 RLD 信号则为可用的。反馈元件安装在芯片外部，环路为闭环的。该信号可以经过滤波后馈电，或者直接馈电到 RLDIN 引脚上，如 Figure 29 所示。通过设置适当通道寄存器的 mux 位为 110(P 侧)，和 111(N 侧)可 RLDIN 信号复用到任意一个输入电极。Figure 29 所示为通道 1，2，3 产生的 RLD 信号接到通道 8 的 N 侧。利用这一特性可以动态改变用于驱动患者身体的参考信号的电极。相对应的通道则不能被使用，可以将其关闭。

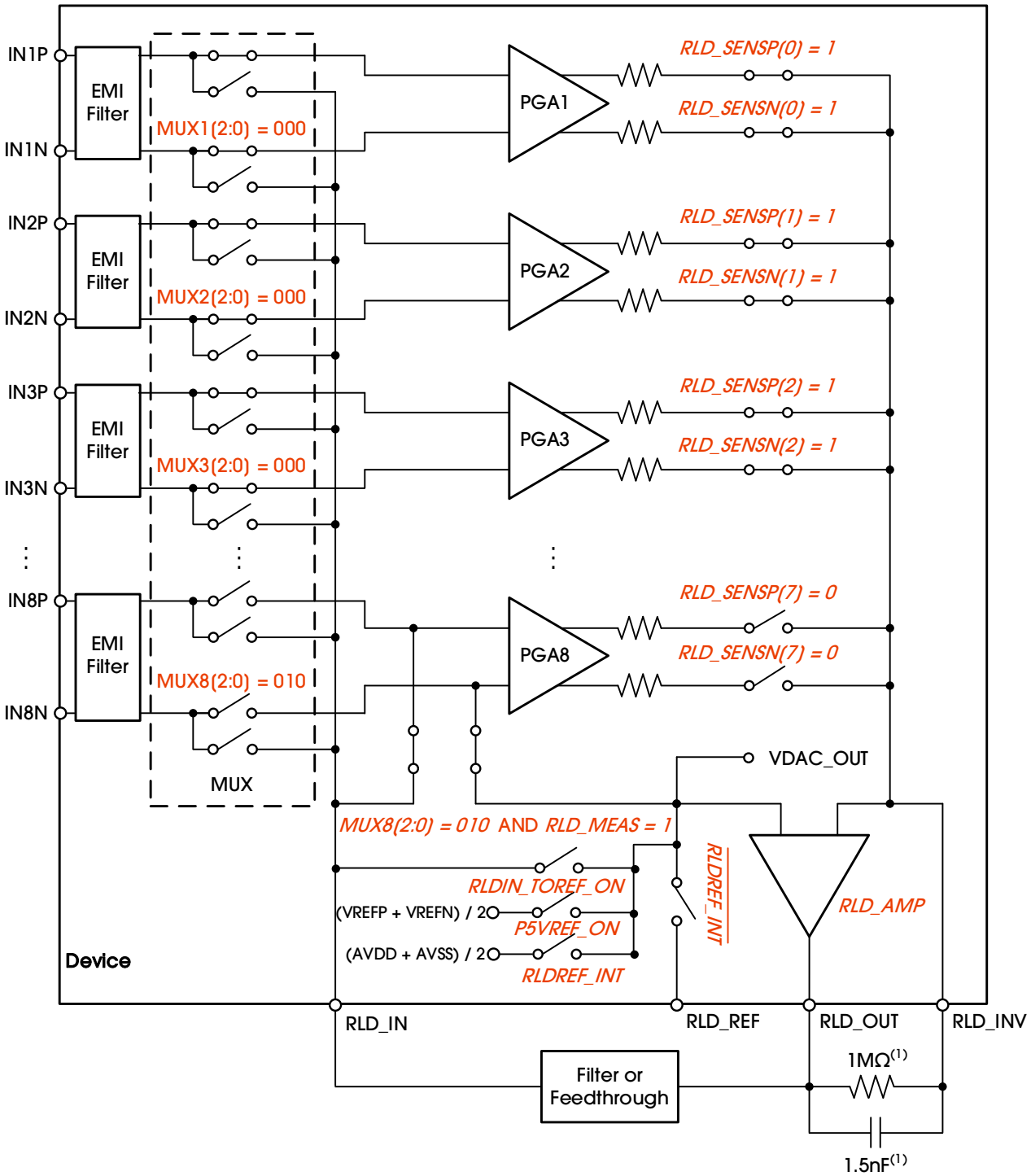


(1) Typical values for example only.

Figure 29. Example of RLDOUT Signal Configured to be Routed to IN8N

8.3.1.7.2 输入多路复用器(测量右腿驱动信号)

RLDOUT 信号可以被接到一个通道(不是用于计算 RLD 的)来进行测量。Figure 30 所示为将 RLDIN 信号接到通道 8 的寄存器设置。对 RLDREF 引脚上的电压进行测量。若 RLDREF 是设置为内部，则为(AVDD + AVSS) / 2。该特性对于产品开发过程中的调试非常有用。



(1) Typical values for example only.

Figure 30. RLDOUT Signal Configured to be Read Back by Channel 8

8.3.1.7.3 威尔逊中部终端和胸部导联

在标准的十二导联心电图中，WCT 电压定义为右臂(RA)、左臂(LA)和左腿(LL)的电极的平均电压。该电压被用作测量胸前导联的参考电压。AFE95x 有三个集成的可生成 WCT 电压的低噪声滤波器。Figure 31 所示为实现框图。

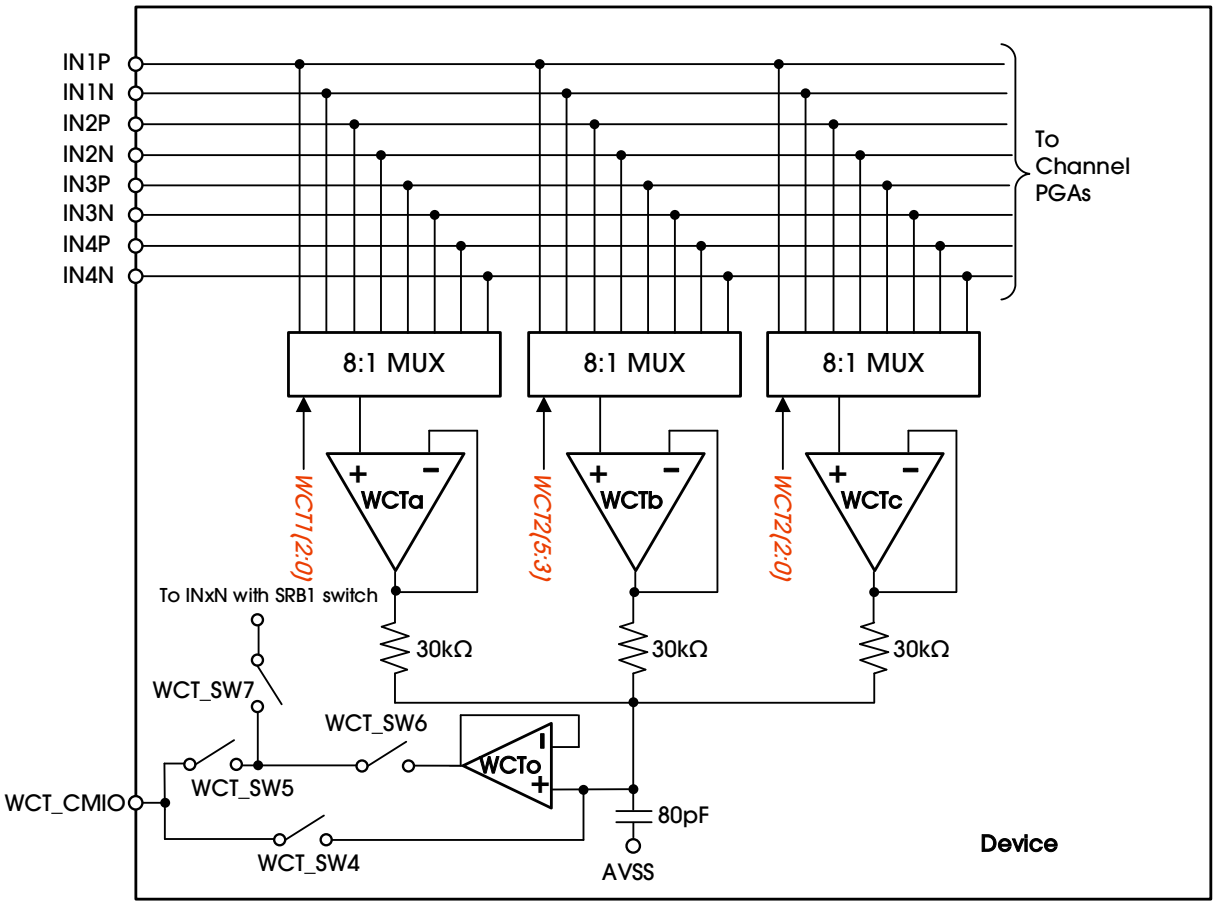


Figure 31. WCT Voltage

这些设备提供了将八通道的任意一个信号(IN1P to IN4N)连接到每个放大器来生成平均值的灵活性。这种灵活性使得 RA,LA,LL 电极可以被连接到前四个通道的任意输入端，具体取决与导联的设置。

WCT 电路中的三个放大器都可以通过寄存器设置单独关掉。通过给两个放大器供电，WCT 引脚可以产生任意两个电极的平均值。给一个放大器通电，则在 WCT 引脚处提供了一个缓冲电极电压。WCT 放大器具有有限的限制强度，故如果用于驱动低阻抗负载，则必须有缓冲。WCT 放大器的斩波由 WCT_CHOP_DISABLE 控制。

Table 22 显示使用任意 1、2 或 3 个 WCT 缓冲区时的典型 WCT 性能。

Table 22. Typical WCT Performance

PARAMETER	ANY ONE (A, B, or C)	ANY TWO (A + B, A + C, or B + C)	ALL THREE (A + B + C)	UNITS
Integrated Noise	472	335	274	nV_{RMS}
Power	87	153	219	µW
–3dB BW	30	59	89	kHz
Slew Rate	BW limited	BW limited	BW limited	V/µs

如 Table 22 所示，当一个以上的 WCT 放大器通电时，整体噪声降低。这种噪声降低是由于噪声被放大器输出处的无源累加网络(passive summing network)平均的结果。关闭单个缓冲器的电源节省的电能可以忽略不计，因为电路的很大一部分是在三个放大器之间共享的。WCT 节点的带宽被 RC 网络限制。内部累加网络(summing network)包括三个 30kΩ 的电阻和一个 80pF 的电容。为了获得最佳性能，添加一个外部 100pF 的电容。有效带宽取决于通电的放大器个数，如 Table 22 所示。

只能使用 WCT 节点来驱动非常高的输入阻抗(通常大于 500MΩ)。一个典型的应用将 WCT 信号连接到 AFE95x 的负端输入，作为胸部导联的参考信号。

8.3.1.7.3.1 WCT 放大器

当 WCT_CHOP_DISABLE 为 0 时，放大器的输入是斩波的，并且截断频率随着 AFE95x 的数据速率而变化。三种最高数据速率的斩波频率为 1:1。例如，在 32kSPS 数据速率下，在 WCT_chop = 0 时的 HR 模式下，截断频率为 32kHz。四个较低数据速率的截断频率固定在 4kHz。当 WCT_CHOP = 1 时，截断频率固定为最高数据速率频率(即 f_{MOD} / 16)，如 Table 23 所示。截断频率以直流上出现一个小方波的形式出现在 WCT 放大器的输出。方波的振幅是放大器的偏移量，通常为 5mVPP。作为带外截断的结果，该现象不会干扰 ECG 相关测量。如 Figure 32 所示，由于斩波功能，连接 WCT 放大器的引脚上的输入电流泄漏在更高的数据速率下增加，以及随着输入共模电压在 0V(AVSS)附近摆动。

如果连接到 WCT 放大器的通道(比如 V 导联通道(V-lead channels))的输出连接到一个用于外部步数检测(pace detection)的放大器来中，则截断现象(chopping artifact)出现在 pace amplifier 的输出。

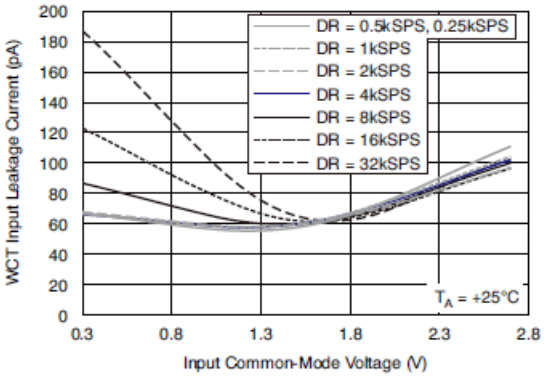


Figure 32. WCT Input Leakage Current vs. Input Voltage (WCT_CHOP = 0)

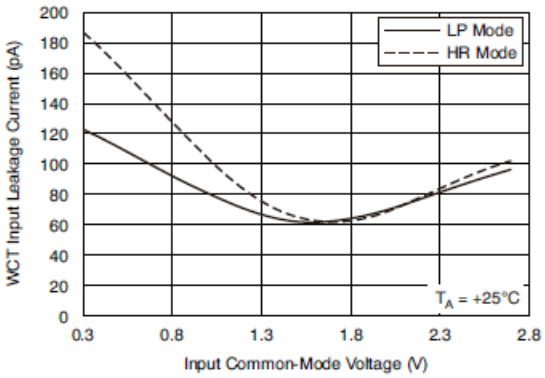


Figure 33. WCT Input Leakage Current vs. Input Voltage (WCT_CHOP = 1)

Table 23. WCT Amplifiers Chop Frequency

CONFIG1.DR(2:0) BIT	CONFIG2.WCT_CHOP = 0	CONFIG2.WCT_CHOP = 1
000	f_{MOD} / 16	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
001	f_{MOD} / 32	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
010	f_{MOD} / 64	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
011	f_{MOD} / 128	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
100	f_{MOD} / 128	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
101	f_{MOD} / 128	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16
110	f_{MOD} / 128	REDR2P.WCT_CHOP(2:0), default f_{MOD} / 16

8.3.1.7.3.2 使用 WCT 的右腿驱动

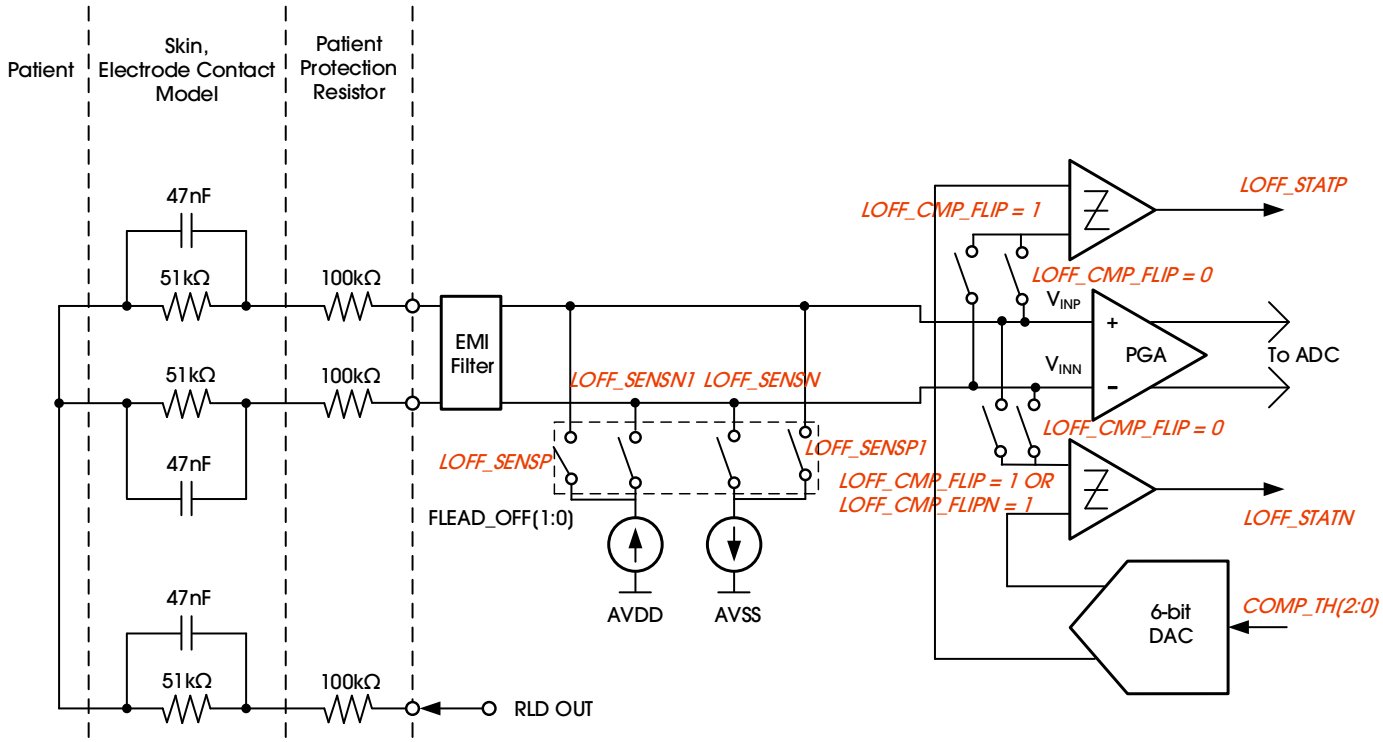
在某些应用中，WCT 的非相位版本(out-of-phase version)被用作 RLD 的参考。AFE95x 提供了一个在 RLD_OUT 引脚处有一个 WCT 终端的缓冲版本的选择。信号可以通过外部放大器进行倒相，作为右腿的驱动。(详情参考 RIGHT LEG DRIVE (RLD DC BIAS CIRCUIT)一节)

8.3.1.7.4 导联脱落检测

患者电极阻抗随时间衰减，因此必须对这些电极连接持续监控，以确保合适的连接。在 AFE95x 是导联检测功能模块提供了很大的灵活性来选择不同的导联检测策略，尽管叫做导联脱落检测(lead-off detection)，这种特性实际上是电极导通检测。(electrode-off detection)。

基本原理是注入激励信号，然后测量响应来确定电极是否断开。如 Figure 34 导联检测功能框图所示，电路提供了两个不同的方法来确定患者的电极状态。这两种方法在激励信号的频率含量上是不同的。可使用 LOFF_SENSP 和 LOFF_SENSE 寄存器在每个通道的基础上有选择性地导联。当传感电路使能时，内部激励电路可以被禁用。

在启用 LOFF_SENS_DEC 的情况下，可以使用 LOFF_SENSEP1 和 LPFF_SENSN1 翻转 DC 引出，并在电流源和电流阱翻转的情况下进行 LOFF_CMP_FLIP。当 LOFF_SENSP、LOFF_SENS1 和 LOFF_CMP_FLIP 都设置为 1 时，OFF_SENSN、LOFF_SENSN1 和 LOFF_CMP_FLIPN 都被清零，则在源电流模式下对所有输入引脚执行直流导联脱落检测。



NOTE: The R_P value must be selected in order to be below the maximum allowable current flow into a patient (in accordance with the relevant specification in the latest revision of IEC 60601).

Figure 34. Lead-Off Detection

8.3.1.7.4.1 直流导联脱落

该方法中，导联脱落激励是使用直流信号完成的。从外部上拉或下拉电阻器或从内部电流源或电流阱中选择一个直流激励信号，如 Figure 35 所示。通过设置 LOFF 寄存器的 VLEAD_OFF_EN 位来选择。通道的一端被拉向 AVDD，另一端被拉向 AVSS。通过设置寄存器 LOFF_FLIP 来交换电流源与电流阱的开关，如 Figure 35 所示。如果使用电流源或电流阱，则通过设置寄存器 LOFF 的 ILEAD_OFF(1：0)位或寄存器 LOFF_CFG1 的 ISTEP(5:0)位来设置电流的量级，ILEAF_OFF 和 ISTEP 的有效设置由 LOFF_CFG1 寄存器的 CUR_LEVEL 决定。电流源和电流阱提供更大的输入阻抗。

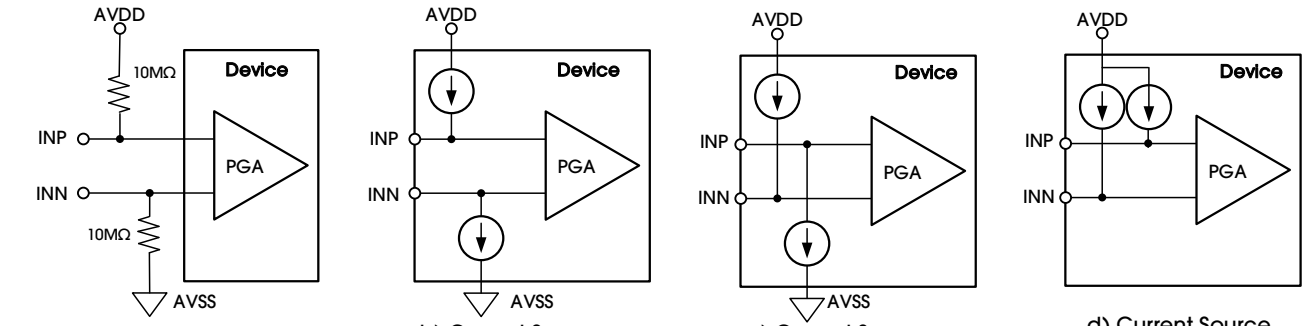


Figure 35. DC Lead-Off Excitation Options

通过查看设备的数字输出码或使用片上比较器来监控输入电压可以实现响应检测。如果有任一电极是关闭的，则上拉或下拉电阻会使通道饱和。查看输出码可确定 P 端或 N 端是否关闭。要查明哪一侧关闭，可以检测比较器的输出。在转换过程中，输入电压由一个比较器和一个六位的 DAC 同时监控，电平由 LOFF 寄存器中的 COMP_TH(2:0)位设置，比较器可以将输入电压与用 LOFF_CMP_FLIP 寄存器中的 LOFF_CMP_FLIP1 设置的电压相比较。比较器的输出储存在寄存器 LOFF_STATP 和 LOFF_STATN 在。这两个寄存器作为输出数据流的一部分提供 (请参阅 DATA OUTPUT PIN (DOUT)部分)。如果直流导联没有被使用，则导联比较器可以通过设置 CONFIG4 的 PD_LOFF_COMP 位来关闭。

LEAD-OFF 部分给出了打开直流导联脱落的示例过程。

8.3.1.7.4.2 采用带外方法的交流导联脱落

该方法使用带外交流信号作为激励。交流信号有一个固定频率，是通过在输入端提供上拉和下拉电阻产生的。该交流信号通过一个平滑滤波器来防止混叠。用 LOFF 寄存器中的 FLEAD_OFF(1:0)位来选择频率。激励频率是输出信号速率的函数，为 f_{DR} / 4。该带外激励信号通过通道并在输出端处被测量。

交流信号传感(sensing)是通过使信号经过通道来量化信号，然后测量输出来实现的。交流信号以高于有用频带的频率引入，产生可以被单独滤除和处理的带外差分信号。通过测量输出谱的激励信号的大小可以计算出导联状态。所以，交流导联检测是与心电信号获取同步进行的。

8.3.1.7.4.3 采用直接数字合成方法的交流导联脱落

该方法使用直接数字合成(DDS)进行激励。交流信号是通过提供可配置的正弦波和方波来产生的。使用 LOFF_ACLO2 中的 ACDIV_FRQ(3:0)和 ACDIV_FACTOR 选择频率。SQUARE_WAVE 用于设置正弦和方形交流激励。IDAC_OFFSET_EN 用于设置 AC 激励中的 DC 偏移。LOFF_CFG2 中的 AC_EXCT_IMAG2 用于设置 AC 激励幅度。激励信号通过通道并进行测量。查看 LOFF_ACLO2 和 LOFF_CFG2 了解详细信息

AC 信号感测是通过使信号通过通道来进行数字化并测量输出来实现的。交流激励信号以寄存器配置的频率引入。通过测量输出频谱上激励信号的幅度，计算出导通状态。因此，交流导通脱落检测与 ECG 信号采集同时完成。

8.3.1.7.5 右腿驱动导联脱落

通过关闭 RLD 放大器的电源可以确定 RLD 电极是否连接到 AFE95x 中。在断电后，确定 RLD 电极连接状态有两个测量步骤：上拉电阻或下拉电阻或电流源或电流宿，如 Figure 36 所示。设置比较器的参考电平来确定可接受的 RLD 阻抗阈值。

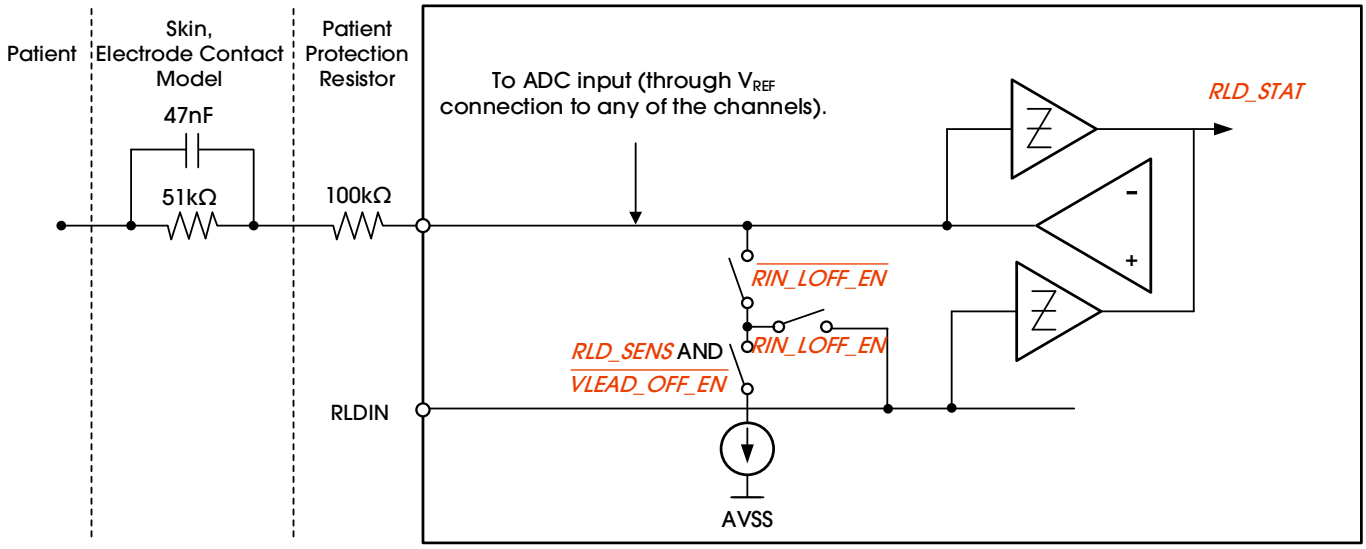


Figure 36. RLD Lead-Off Detection at Power-Up

当 RLD 放大器通电时，电流源，上拉和下拉电阻的方法都不起作用。利用比较器来检测 RLD 放大器两端的电压。比较器的阈值是通过设置与用于设置其它负端输入的阈值相同的 LOFF(7:5)位或 RLD_COMP_TH(2:0)位来实现的。当 LOFF_CFG1 中的 RLD_COMP_EN 被设置时，RLD_COMP_TH(2:0)位是专用阈值设置。RIN_LOFF_EN 用于选择 RLDIN 或 RLDOUT 上的 LEAD-OFF 检测。

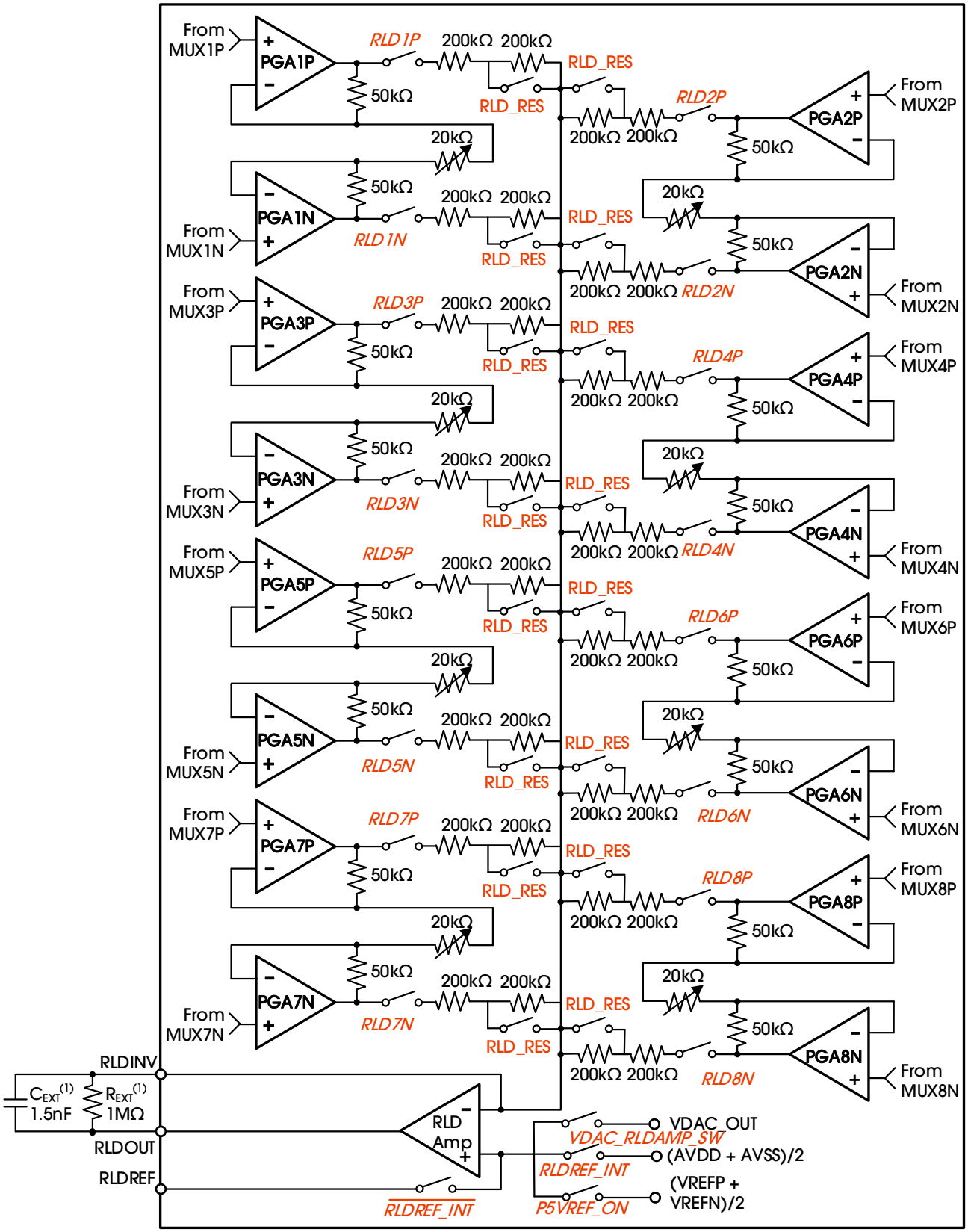
8.3.1.7.6 右腿驱动(RLD)直流偏置电路

使用右腿驱动电路来对抗电源线和其它源(包括荧光灯)对 ECG 系统造成的共模干扰。RLD 电路感知选定的一组电极的共模电压，通过用一个与共模信号相反的信号来驱动身体，以产生负反馈环路。根据环路增益，负反馈环路将共模运动限制在一个很窄的范围内。基于环路中的不同极点，使整个环路稳定是特定于通道单个系统的。AFE95x 集成了用于选择运放通道的多路选择器。所有放大器的终端都在引脚处可用，允许选择负反馈环路的元间。Figure 37 所示的电路图显示了 RLD 偏置电路的整个功能连接。

可设置内部生成的 RLD 基准电压((AVDD + AVSS) / 2)，也可以通过电阻分压器在外部提供该基准电压。通过将适当的值写入 CONFIG3 寄存器中的 RLDREF_INT 位来确定为 RLD 环路选择内部基准电压还是外部基准电压。CONFIG9 寄存器中的 RLD_RES 位能够通过 RLD 放大器控制 200kΩ 或 400kΩ 电阻。

如果未使用 RLD 功能，则使用 PD_RLD 位使放大器断电(有关详细信息，请参阅 CONFIG3: CONFIGURATION REGISTER 3 (ADDRESS = 03H) (RESET = 40H)部分)。该位还用于菊花链模式来关闭除一个之外的所有 RLD 放大器。

RLDIN 引脚的功能在 INPUT MULTIPLEXER 部分介绍。一个使用 RLD 放大器的例程在 RIGHT LEG DRIVE 小节中的推荐供电电源部分进行介绍。



(1) Typical values.

(2) When CONFIG3 bit RLDREF_INT = 0, the $\overline{\text{RLDREF\_INT}}$ switch is closed and the RLDREF_INT switch is open.
When CONFIG3 bit RLDREF_INT = 1, the $\overline{\text{RLDREF\_INT}}$ switch is open and the RLDREF_INT switch is closed.

Figure 37. RLD Channel Selection

8.3.1.7.6.1 WCT 作为 RLD

在某些应用中，RLD 是由 RA、LA、LL 的平均值推导得到的。该电平与 WCT 的电平一样。WCT 放大器具有有限的驱动强度，只能直接用 WCT 来驱动非常高的阻抗。AFE95x 提供了一个通过设置寄存器 CONFIG4 的 WCT_TO_RLD 位来对 WCT 信号进行内部缓冲的选择。在设备外部短接 RLD_OUT 和 RLD_INV 引脚。在 RLD_OUT 信号连接到 RLD 电极之前，利用一个外部放大器来反转信号的相位作为负反馈。

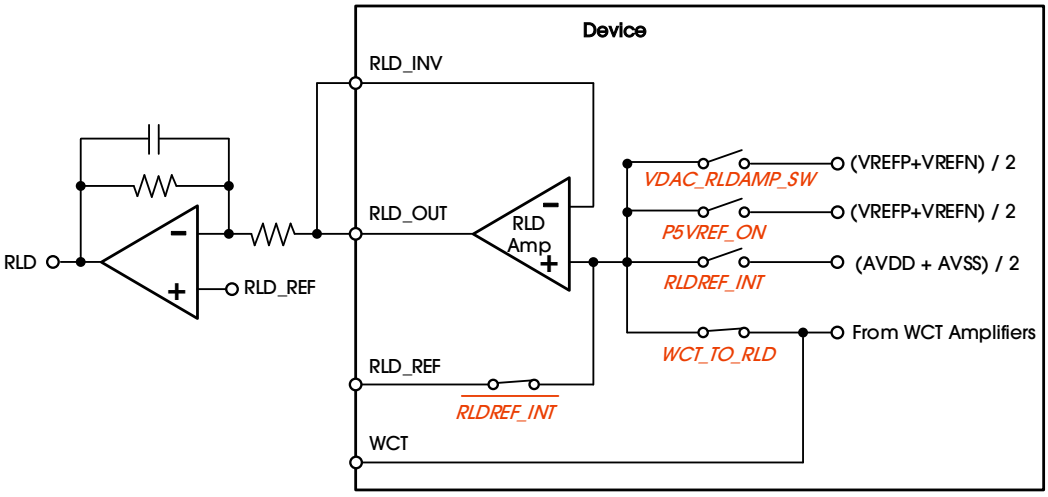


Figure 38. Using the WCT as the Right Leg Drive (RLD)

8.3.1.7.6.2 多个设备的 RLD 配置

Figure 39 显示了连接到 RLD 的多个设备。

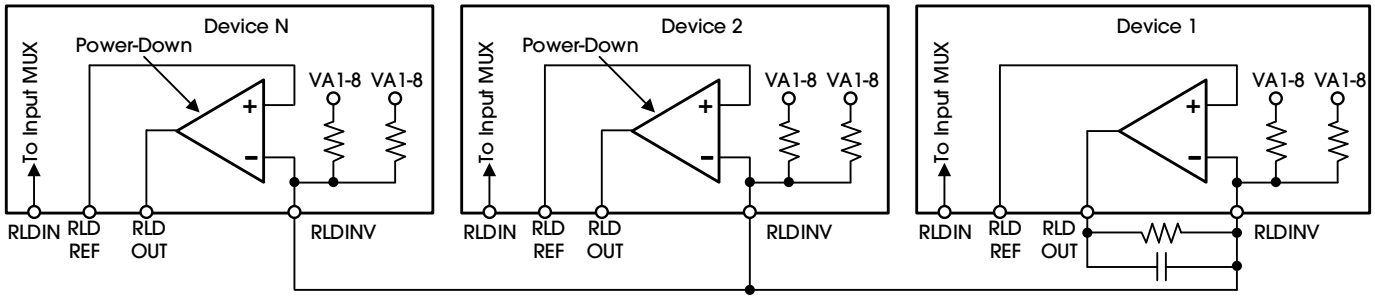


Figure 39. RLD Connection for Multiple Devices

8.3.1.7.7 起搏检测

AFE95x 提供了通过软件或外部硬件进行起搏检测的灵活性。软件方法是通过提供高于 64kSPS 的采样率来实现的。外部硬件方法是通过引出 PGA 的输出到两个引脚：TESTP_PACE_OUT1 and TESTN_PACE_OUT2。如果 WCT 放大器被连接到信号通道，那么会由于斩波产生开关噪声。

8.3.1.7.7.1 软件方法

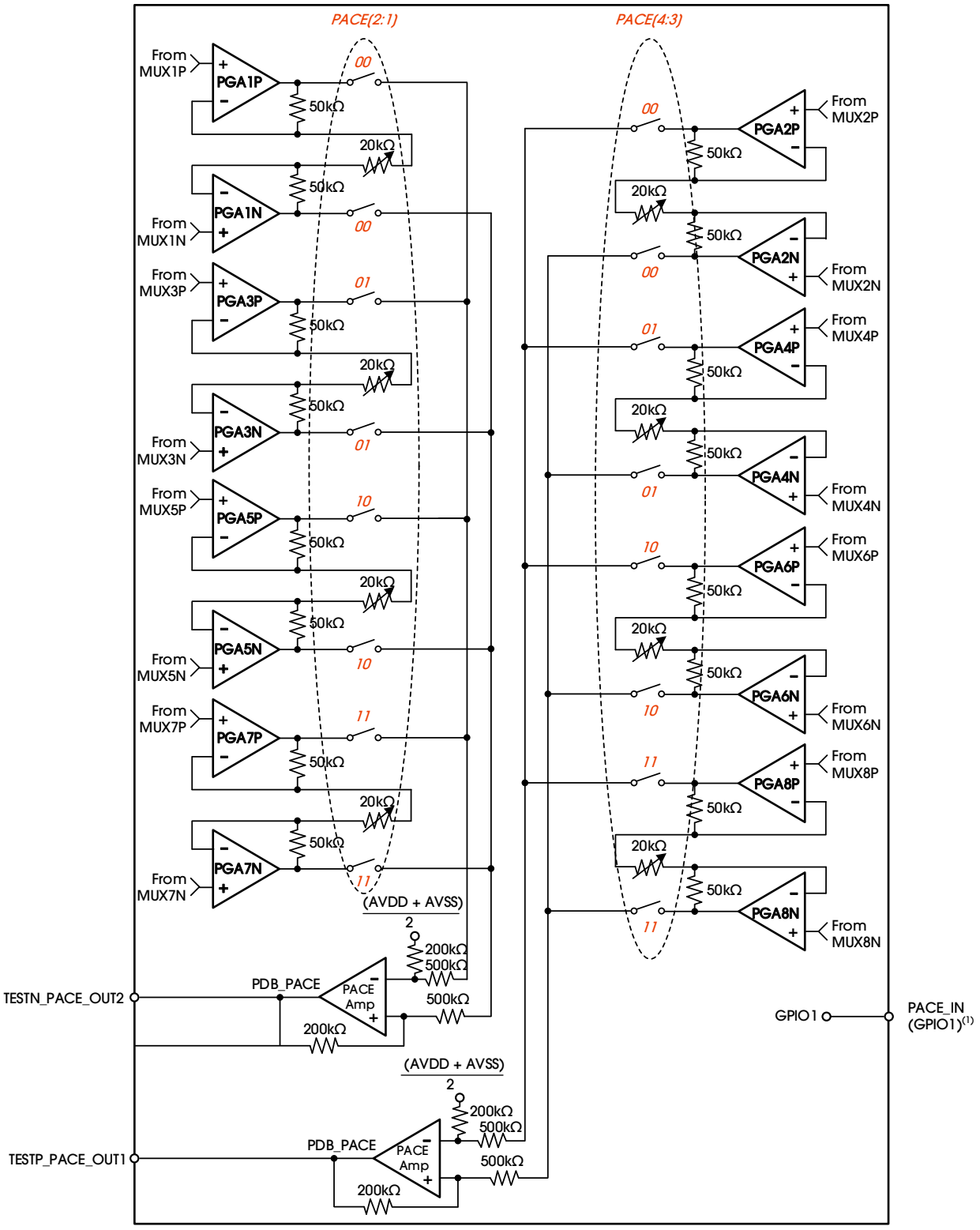
使用软件方法时，将设备设置为 8kSPS 或更高的速率以捕获快速脉冲。然后，进行数字信号处理，以确认起搏器脉冲是否存在(pacemaker pulse)。软件方法为通过软件动态编程起搏器检测阈值(pace detect threshold)提供了最大限度的灵活性。随着起搏器的发展(evolve)该灵活性变得越来越重要。

1. PGA 带宽：决定了可使用的增益设置
2. 设置时间：决定了设备的操作数据速率。对于输入的阶跃变化，数字抽取滤波器需要 3 × t_{DR} 才能稳定。

8.3.1.7.7.2 外部硬件方法

使用软件方法的缺点是一个设备的所有通道都必须操作在高数据率上。对于一些难以使用高速率的系统，AFE95x 提供了一个连接外部硬件到 PGA 的输出来检测脉冲存在与否的选择。于是起搏器检测(pace detection)逻辑的输出通过一个 GPIO 引脚被送进设备。通用接口 GPIO 的数据通过 SPI 口进行传输，在$\overline{DRDY}$变低之前需加载 2 t_{CLK}s。利用寄存器 PACE 选择八个通道中的两个通道，其中一个为奇数通道，一个为偶数通道。在差分到单端转换时，有一个 0.4 的衰减。因此 PACE 路径的总增益为 0.4 × PGA_GAIN。PACE 的输出信号分别通过 TESTP_PACE_OUT1 和 TESTN_PACE_OUT 引脚复用到 $\overline{TESTP}$ 和 $\overline{TESTN}$ 信号。通过设置 PACE 寄存器的(4:1)位可进行通道选择。如果不使用 PACE 电路，则通过 PACE 寄存器的$\overline{PD_PACE}$位来关闭 PACE 放大器。

如果一个连接到 WCT 放大器(比如，V-lead 通道)的通道的输出连接到了一个 PACE 放大器来进行外部起搏器检测(pace detection)，则 pace 放大器的输出会出现截断现象(chopping artifacts)。详情请见 WILSON CENTRAL TERMINAL (WCT) AND CHEST LEADS 部分。



(1) GPIO1 can be used as the PACE_IN signal.

Figure 40. Hardware Pace Detection Option

8.3.1.7.7.3 呼吸

AFE95x 提供三种呼吸阻抗测量选项：外部呼吸、使用片上调制信号的内部呼吸以及使用用户生成的调制信号的内部呼吸。

Table 24. Respiration Control

RESP.RESP_CTRL(1)	RESP.RESP_CTRL(0)	DESCRIPTION
0	0	Respiration disabled
0	1	Generates modulation and demodulation signals for external respiration circuitry. RESP_CLK signals on GPIO2, GPIO3, and GPIO4.
1	0	Respiration measurement using internally-generated RESP_MOD signals.
1	1	Respiration measurement using user-generated modulation and blocking signal.

注：如果 CLKSEL = 1(内部主时钟)，请勿设置 RESP_CTRL(1:0) = 11。

8.3.1.7.7.4 外部呼吸电路(RESP_CTRL = 01B)

使用此选项，GPIO2、GPIO3 和 GPIO4 将自动配置为输出。信号之间的相位关系如 Figure 41 所示。GPIO2 是 GPIO3 和 GPIO4 的异或，如 Figure 42 所示。GPIO3 是调制信号，GPIO4 是解调信号。使用该选项时，GPIO2、GPIO3、GPIO4 的通用引脚功能不可用。通过使用 CONFIG4 寄存器中的 RESP_FREQ(2:0)位将调制频率设置为 64kHz 或 32kHz。RESP_FREQ(2:0)的其余位选项在 GPIO3 和 GPIO4 上生成方波。GPIO2 上的异或输出仅适用于 64kHz 或 32kHz。GPIO4 相对于 GPIO3 的相位由 RESP 和 CONFIG7 寄存器中的 RESP_PH(3:0)位设置。

使用此选项可在 AFE95x 外部实现自定义呼吸阻抗电路。

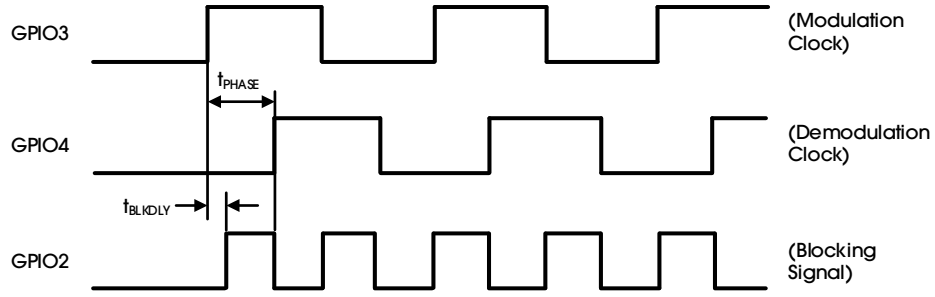


Figure 41. External Respiration (RESP_CTRL = 01b) Timing

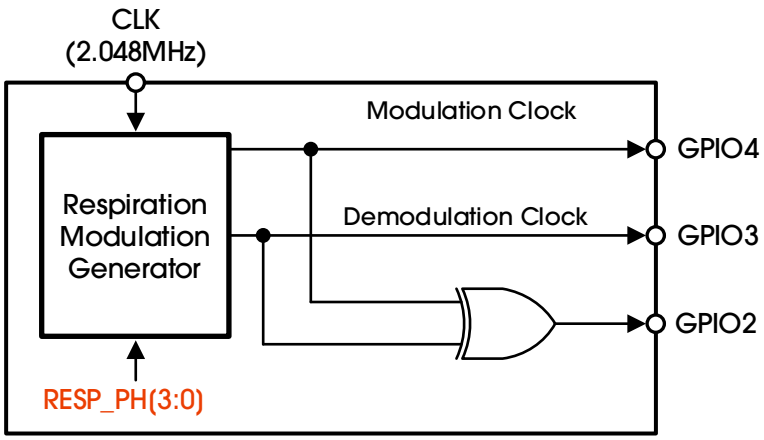


Figure 42. External Respiration (RESP_CTRL = 01b) Block Diagram

Table 25. Switching Characteristics for Figure 42

PARAMETER	SYMBOL	2.7V ≤ DVDD ≤ 3.6V			1.65V ≤ DVDD ≤ 2V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Respiration Phase Delay, Set by RESP.RESP_PH(2:0)	t_{PHASE}	22.5		157.5	22.5		157.5	Degrees
Modulation Clock Rising Edge to XOR Signal	t_{BLKDLY}		1			5		ns

Note: Specifications apply from –40°C to 85°C.

8.3.1.7.7.5 带内部时钟的内部呼吸电路(RESP_CTRL = 10B)

Figure 43 显示了内部呼吸电路的框图。可以选择性地使用内部调制和解调器电路。

调制模块由 RESP_MOD_EN 位控制，解调模块由 RESP_DEMOD_EN 位控制。调制信号是幅度为 VREFP–AVSS 的方波。使用此选项，调制电路的输出可在器件的 RESP_MODP 和 RESP_MODN 引脚上使用。此可用性允许将自定义滤波添加到方波调制信号中。使用此选项，GPIO2、GPIO3 和 GPIO4 可以用于其他目的。调制频率为 64kHz、32kHz 或 42.667kHz(在 FEATUERS 部分称为 43kHz)，由 CONFIG4 寄存器中的 RESP_FREQ(2:0)和 RESP_43K_FREQ 位设置。内部解调信号的相位由 RESP 和 CONFIG7 寄存器中的 RESP_PH_MSB 和 RESP_PH(2:0)位设置。

启用此呼吸选项后，AFE95x 通道 1 无法用于接收 ECG 信号。如果 RA 和 LA 导联用于测量呼吸和 ECG 信号，请将两条导联连接到用于呼吸的通道 1 和用于 ECG 信号的通道 2。RESP_DR_EN 能够增强呼吸性能，CONFIG7 寄存器的 RESP_DR(2:0)位可用于控制通道 1ODR，以获得更好的噪声性能。请注意，RESP_DR(2:0)设置不得小于 ECG 通道 DR(2:0)设置。

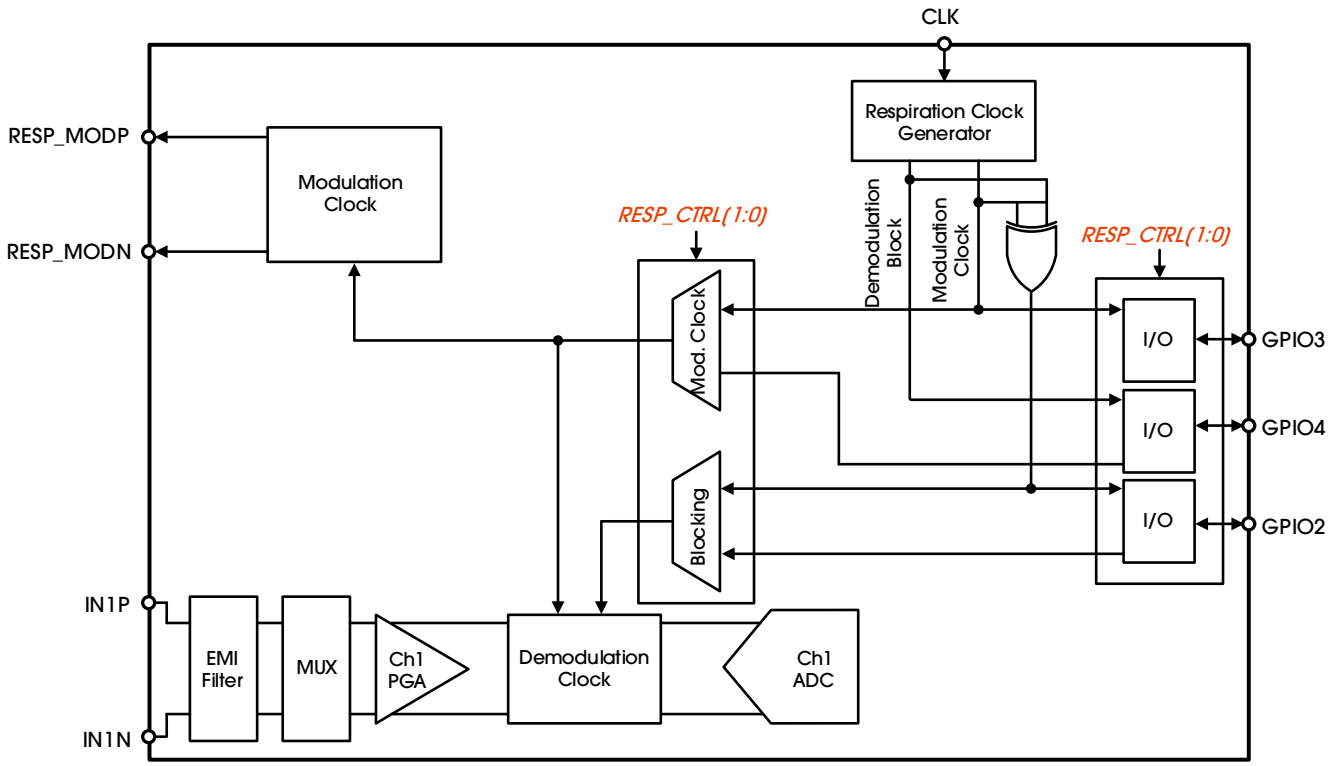


Figure 43. Internal Respiration Block Diagram

8.3.1.7.7.6 用户产生信号时钟的内部呼吸电路(RESP_CTRL = 11B)

在此模式下，GPIO2、GPIO3 和 GPIO4 自动配置为输入，不能用于其他用途。必须如 Figure 44 中所述提供信号。请勿在此模式下使用内部主时钟。

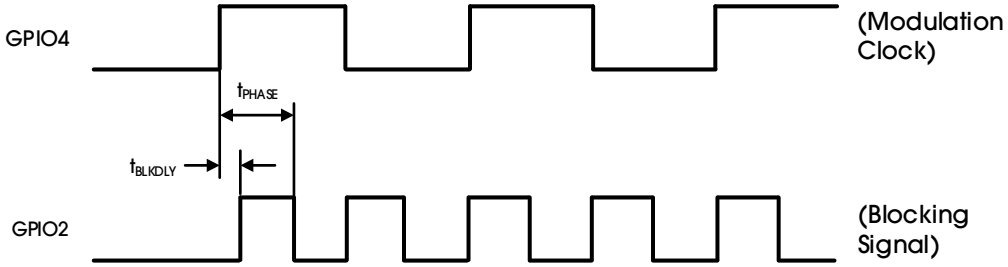


Figure 44. Internal Respiration (RESP_CTRL = 11b) Timing Diagram

Table 26. Switching Characteristics for Figure 44

PARAMETER		1.65V ≤ DVDD ≤ 3.6V			UNITS
		MIN	TYP	MAX	
Respiration Phase Delay	t_{PHASE}	0		167.85	Degrees
Modulation Clock Rising Edge to XOR Signal	t_{BLKDLY}		0	5	ns

注：技术指标适用于–40°C 至 85°C。

8.3.2 数字功能

8.3.2.1 GPIO 引脚(GPIO[4:1])

AFE95x 一共有 4 通用数字输入/输出引脚可作为正常操作使用。通过寄存器 GPIO 的 GPIOC 位，可以单独设置数字 IO 引脚为输入或输出。寄存器 GPIO 的 GPIOD 位控制引脚的电平。当读取 GPIOD 位时，返回的数据是引脚的逻辑电平，无论他们被设置为输入或输出。当 GPIO 引脚被设置为输入时，对相应的 GPIO 位进行写操作则为无效的。当 GPIO 被设置为输出时，对 GPIOD 写的值则为输出的值。

当被配置为输入时，有三个引脚必须被驱动，不能使它们悬空(float)。GPIO 引脚是在开启电源(power-on)或者复位后被设置为输入的。Figure 45 所示为 GPIO 口的结构。如果不使用，则将这三个引脚短接到地。

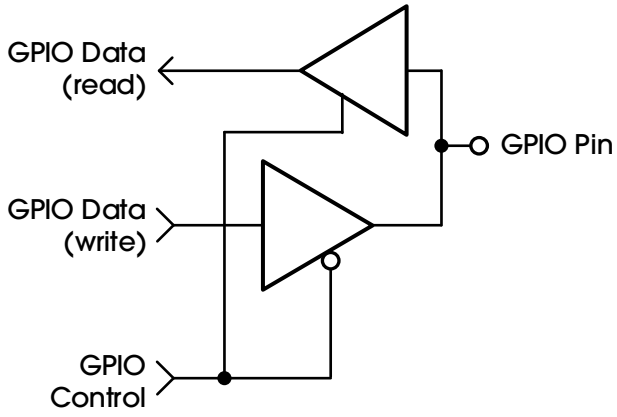


Figure 45. GPIO Port Pin

8.3.2.2 断电($\overline{PWDN}$)

将$\overline{PWDN}$拉至低电平后，所有片上电路都会断电。要退出关断模式，请将$\overline{PWDN}$引脚置于高电平。一旦退出关断模式，内部振荡器和基准就需要一段时间才能唤醒。在关断期间，关闭外部时钟以省电。

8.3.2.3 复位(RESET引脚和重置命令)

可通过两种方法来对 AFE95x 进行复位：将RESET引脚拉至低电平，或发送复位指令(请参阅 RESET: RESET REGISTERS TO DEFAULT VALUES 部分)。将 RESET 引脚置于低电平可强制复位。在将RESET引脚重新置为高电平之前，要确保满足时序特性要求的最小脉冲宽度。复位命令在复位指令的第八个 SCLK 下降沿生效。复位时，需要 18 个 t_{CLK} 周期来完成默认寄存器配置和开始转换的初始化。有关更多信息，请参阅 RESET: RESET REGISTERS TO DEFAULT VALUES 部分。当使用 WREG 命令将寄存器 CONFIG1 和 RESP 设置为新值时，内部会对数字滤波器自动进行复位。

8.3.2.4 数字抽取滤波器

数字滤波器接收调制器的输出然后将数据流进行抽取。通过调整滤波器的总数，可以在分辨率和数据率上进行权衡：滤波器多则可获得更高分辨率，而滤波器少可获得高数据率。高数据率被典型用于心电图应用中，以实现软件起搏信号检测和交流导联检测。

每个通道上的数字滤波器由一个三阶的 sinc 滤波器构成。Sinc 滤波器的抽取比率可有 CONFIG1 的 DR 位来调整。(详情见 Table 33)。这是一个会影响所有的通道的全局设置，所以在这个设备中，所有通道都工作在相同的数据率下。

8.3.2.4.1 SINC 滤波器级(SINX / X)

Sinc 滤波器是一个可改变抽取滤倍数，三阶的低通滤波器。数据由工作在数据率为 f_{MOD} 的调制器输出到该模块。Sinc 滤波器对调制器的高频噪声进行衰减，然后抽取数据流使其变成并行数据。抽取倍数会影响整个转换器的数据率。

Equation 4 显示了 sinc 滤波器的缩放 Z 域传递函数。

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3 \tag{4}$$

sinc 滤波器的频域传递函数如 Equation 5 所示。

$$|H(f)| = \left| \frac{\sin\left[\frac{N\pi f}{f_{MOD}}\right]}{N \times \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^3 \tag{5}$$

其中：

- N = 抽取率

Sinc 滤波器在输出数据率的倍数上会出现零陷。在这些频率上，滤波器有无限的衰减。Figure 46 所示为 sinc 滤波器的频率响应，Figure 47 所示为 sinc 滤波器的衰减图。当输入有一个阶跃跳变，滤波器需要 3 个 t_{DR} 的转换周期来稳定。在 START 引脚有一个上升沿或一个 START 指令完成后，滤波器需要花 t_{SETTLE} 周期来产生第一个数据输出。在不同数据率情况下的滤波器的设置时间(setting time)在 SPI 接口部分的 START MODE 小节中进行讨论。Figure 48 和 Figure 49 所示为滤波器分别在 f_{MOD} / 2 和 f_{MOD} / 16 的不同数据率下的传递函数。Figure 50 所示为扩展到 4 × f_{MOD} 的传递函数，如 Figure 50 所示，AFE95x 的通带在每一个 f_{MOD} 的倍数重复出现。为系统选择 RC 平滑滤波器来衰减 f_{MOD} 倍数附近的频率干扰。

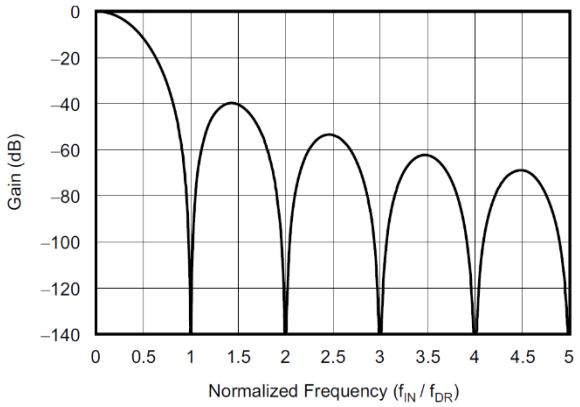


Figure 46. Sinc Filter Frequency Response

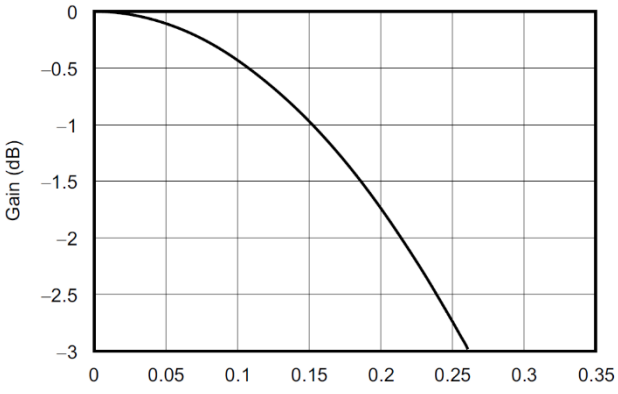


Figure 47. Sinc Filter Roll-Off

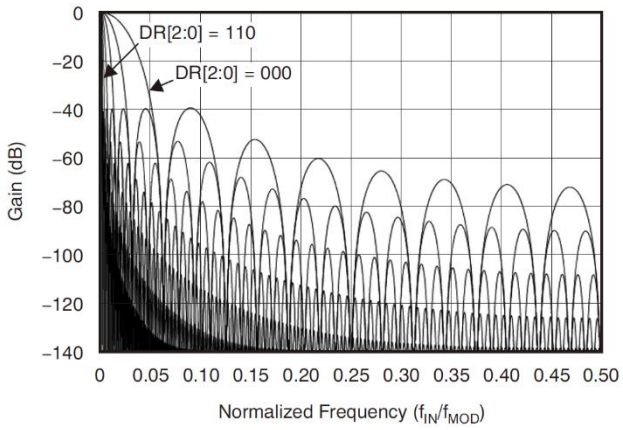


Figure 48. Transfer Function of On-Chip Decimation Filters to f_{MOD} / 2

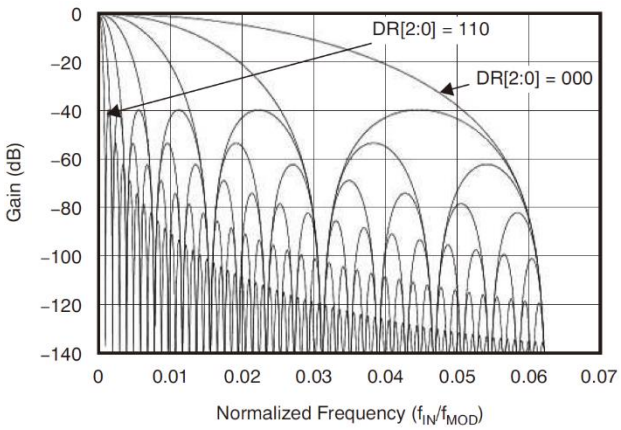


Figure 49. Transfer Function of On-Chip Decimation Filters to f_{MOD} / 16

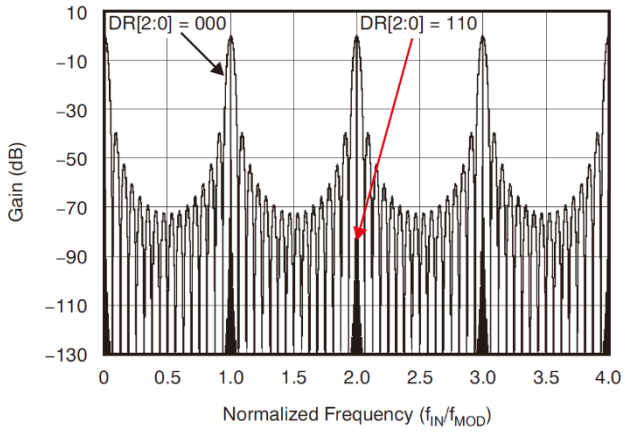


Figure 50. Transfer Function of On-Chip Decimation Filters to 4 × f_{MOD} for DR(2:0) = 000 and DR(2:0) = 110

8.3.2.5 时钟

AFE95x 为设备的时钟提供了两种不同方法：内部和外部。内部时钟是理想地适用于低功耗，电池供电的系统。内部振荡器在室温下进行了微调以确保精度。该精度随着特定温度范围变化。详情见 ELECTRICAL CHARACTERISTICS 部分。时钟的选择由 CLKSEL 引脚和 CLK_EN 寄存器位控制。

用 CLKSEL 引脚来选择内部或外部时钟。在 CONFIG1 寄存器的 CLK_EN 位可以使能或不使能振荡器时钟在 CLK 引脚作为输出。一个关于这两个引脚的真值表在 Table 27 中展示。当多个设备连接一起，处于菊花链的配置时，使用 CLK_EN 位。当关闭电源时，关闭外部时钟来节省能源。

Table 27. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	Tri-state
1	1	Internal clock oscillator	Output: internal clock oscillator

8.4 设备功能模式

8.4.1 数据获取

本节介绍 START 和$\overline{\text{DRDY}}$引脚、稳定数据和数据读回相关的数据采集过程。

8.4.1.1 开启模式

拉高 START 引脚，并持续至少 2 × t_{CLK} 时钟周期，然后发送 START 指令以开始转换。当 START 引脚为低时，或者当 START 指令没有被发送，则设备不发送$\overline{\text{DRDY}}$信号。(转换暂停)

当使用 START 指令来启动转换时，保持 START 引脚为低。AFE95x 有两种模式来控制转换：连续模式和单次模式。这些模式由 SINGLE_SHOT (寄存器 CONFIG4 的第三位)来控制。在多个设备的配置中，START 引脚被用于同步这些设备。(具体见多个设备配置(MULTIPLE-DEVICE CONFIGURATION)部分)。

8.4.1.1.1 建立时间

建立时间 t_{SETTLE} 是指转换器在 START 信号被拉高之后输出整个数据所需要的时间。

当 START 引脚被拉高，或者当 START 命令被发送，设备的 ADC 开始对输入信号进行转换，同时$\overline{\text{DRDY}}$被拉高。$\overline{\text{DRDY}}$的下一个下降沿表示数据已准备好。Figure 51 所示为时序图。Table 28 所示为不同数据率对应的建立时间。建立时间由 f_{CLK} 和抽取倍数(由 CONFIG1 的 DR(2:0))决定。

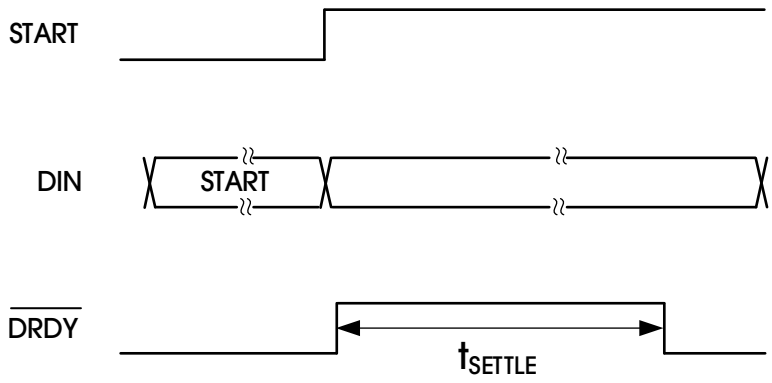


Figure 51. Settling Time for Initial Conversion

Table 28. Settling Times for Different Data Rates (t_{SETTLE})

DR(2:0)	SETTLING TIME (t_{CLK} PERIODS)	
	HIGH-RESOLUTION MODE	LOW-POWER MODE
000	258	515
001	515	1029
010	1029	2057
011	2057	4114
100	4114	8228
101	8228	16456
110	16456	32912

当 START 引脚被拉高，且输入信号有一个阶跃跳变，则滤波器对一个新的值建立稳定需要花 3 × t_{DR} 周期，如 Figure 52 所示。稳定的数据在第四个DRDY脉冲有效。该建立时间在尝试对窄速度脉冲(narrow pace pulse)进行速度检测时必须考虑。数据在DRDY的每一个下降沿有效，但可以将其忽略。

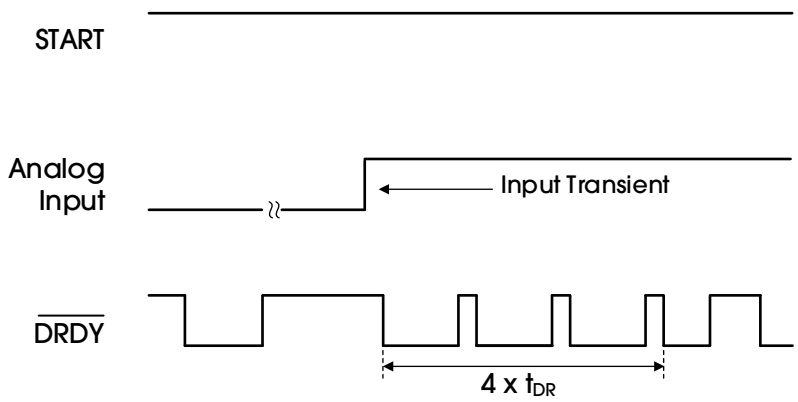


Figure 52. Settling Time for Input Transient

8.4.1.2 数据准备引脚(DRDY)

DRDY是一个输出信号。当DRDY转换为低时，新的转换数据准备好了。CS信号对数据准备信号没有作用。不用管CS信号的状态，SCLK 的上升沿就可以拉高DRDY。所以，当通过 SPI 总线使用多个设备时，用CS信号控制 SCLK。DRDY的行为由设备是否工作在 RDATAC mode 或者 RDATA 命令是否用于按需读取数据决定。详情见 RDATAC: RDATAC: READ DATA CONTINUOUS 和 RDATA: READ DATA 部分。

当在 RDATA 命令下读取数据时，读操作可以在不损坏数据的情况下重叠下一个DRDY的发生。

使用 START 引脚或 START 命令来设置设备处于正常数据获取模式或脉冲数据获取模式。

Figure 53 所示为在数据回读时DRDY、DOUT、SCLK 之间的关系(在 AFE95x 具有提供 24 位分辨率的选定数据速率的情况下)。DOUT 在 SCLK 的上升沿锁存。无论数据是否正在回读还是一个命令刚从 DIN 引脚发送，设备都在 SCLK 的第一个上升沿拉高DRDY。数据从状态的高位开始，然后按顺序接 ADC 通道的数据(通道 1，通道 2……)。被关闭电源的通道在数据流里仍然有位置，但是这些数据是无效的，可以被忽略。

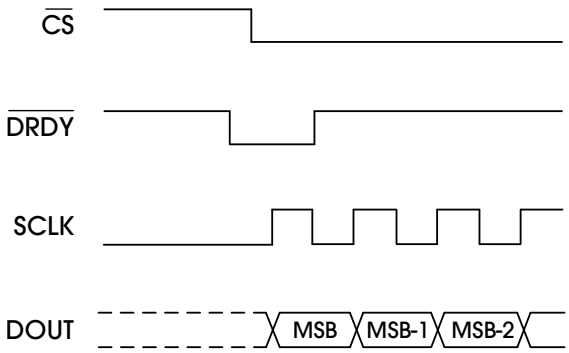


Figure 53. DRDY with Data Retrieval (CS = 0)

不管CS的状态如何，DRDY信号在 SCLK 的第一个下降沿被清除。即使是没有数据输出，DRDY依旧被清除。当 SPI 总线被用于连接其他设备时需考虑该情况。

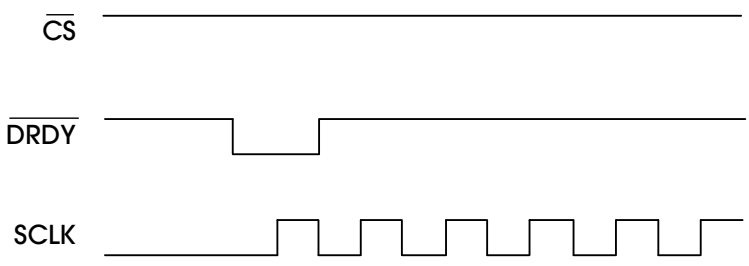


Figure 54. DRDY and SCLK Behavior for SPI Bus Multiplexing

8.4.1.3 数据检索

数据检索是由两种方法中的一个完成的。

1. RDATAC：连续读数据的指令是设置设备处于不用发送指令就可以连续读取数据的模式。有关更多详细信息，请参阅 RDATAC: READ DATA CONTINUOUS 部分。
2. RDATA：读数据模式只从设备读取一个数据输出。有关更多详细信息，请参阅 RDATAC: READ DATA CONTINUOUS 部分。

转换的数据是通过 DOUT 输出的数据读取的。DOUT 输出的最高位的数据是在 SCLK 的上升沿输出的。在 SCLK 的第一个下降沿，DRDY返回高值。在整个读操作中，保持 DIN 为低。

8.4.1.3.1 状态字

AFE95x 的数据回读是由一个提供 ADC 状态信息的状态词引领的。该状态位码为 24 位长，包含 LOFF_STATP, LOFF_STATN, and part of the GPIO 的值。数据队列如 Figure 55 所示。

24 位状态有两种格式，与 RLD_LOFF_FORMAT 寄存器位设置有关。

1. 当 RLD_LOFF_FORMAT 为 0 时，{1100, LOFF_STATP(7:0), LOFF_STATN(7:0), GPIO(7), GPIO(6), GPIO(5), GPIO(4)}。
2. 当 RLD_LOFF_FORMAT 为 1 时，{1100, LOFF_STATP(7:0), LOFF_STATN(7:0), LOFF_RLDP, LOFF_RLDN, GPIO(5), GPIO(4)}。

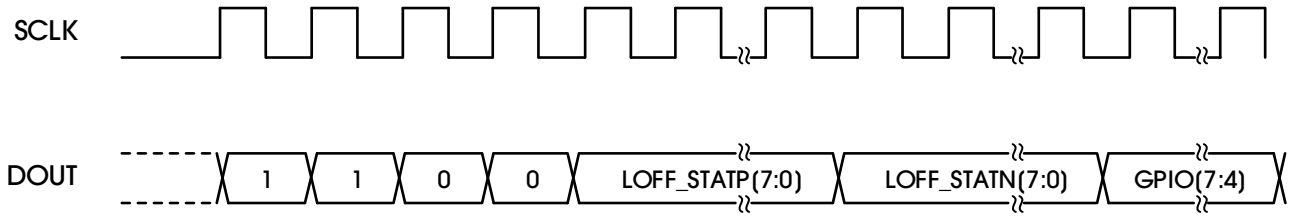


Figure 55. Status Word Content

8.4.1.3.2 回读长度

输出的数据位由通道个数和每个通道的位数决定的，每个通道的数据格式为双补码和高位优先。对于 32kSPS 和 64kSPS 数据率的 AFE95x，数据位数为 24 位的状态位 + 16 位(每个通道) × 8 (通道) = 152 位。对于其它数据率，数据位数为 24 位的状态位 + 24 位(每个通道)× 8 (通道) = 216 位。当通道被通过用户寄存器设置为关闭时，相对应的通道输出为 0。然而通道输出的顺序保留不变。AFE954 输出 4 通道数据流，而 AFE956 输出 6 通道的数据。

AFE95x 同时提供了一个多回读的特性。设置寄存器 CONFIG1 的 DAISY_IN 位来获取多个回读。简单地提供额外的 SCLK 来多次读取数据。在读取最后之后，最高位的数据将重复。

8.4.1.3.3 数据格式

AFE95x 的每个通道输出 24 位的二进制双补码格式，高位优先的数据。低位有一个 V_{REF} / (2^{23} – 1)的权重。一个正的满量程输入的输出码为 7FFFFFh，负的满量程输入产生的输出码为 800000h。当信号超过满量程时，输出信号会在这些码出现截止。Table 29 总结了不同输入信号的理想输出码。当 DR(2:0) = 000 和 001 时，设备分别只有 17 和 19 位的分辨率。最后 7 位或 5 位数据可以被忽略。

Table 29. Ideal Output Code vs. Input Signal(1)

INPUT SIGNAL, V_{IN} (InxP – InxN)	IDEAL OUTPUT CODE(2)
≥ V_{REF}	7FFFFFh
V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / (2^{23} – 1))	800000h

注 1：仅对 24 位分辨率数据速率有效，且增益 = 1。
注 2：不包括噪声、线性度、失调和增益误差的影响。

8.4.1.4 单次模式

通过设置 CONFIG4 寄存器的 SINGLE_SHOT 位为 1 可以使能单次获取模式。在单次获取模式中，AFE95x 在 START 引脚被拉高或者一个 START 指令被发送时进行单次转换。如 Figure 56 所示，当一个转换完成时，$\overline{DRDY}$变为低，然后停止转换。不管转换数据有没有被读取，$\overline{DRDY}$保持为低。如果要开始新的转换，拉低 START 引脚，然后重新拉高并持续 2 个 t_{CLK} 的时间，或者重新发送 START 指令。当要从连续读取数据模式切换到单次获取模式，要确保 START 信号是脉冲的(pulsed)，或者发出一个 STOP 指令，紧接着再发送一个开始指令。

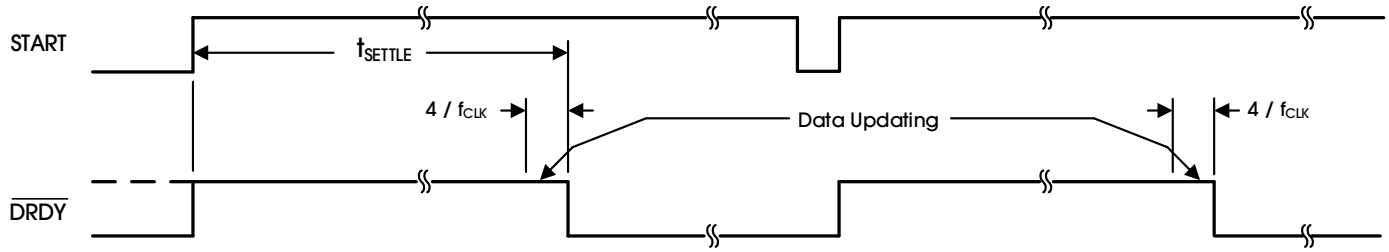
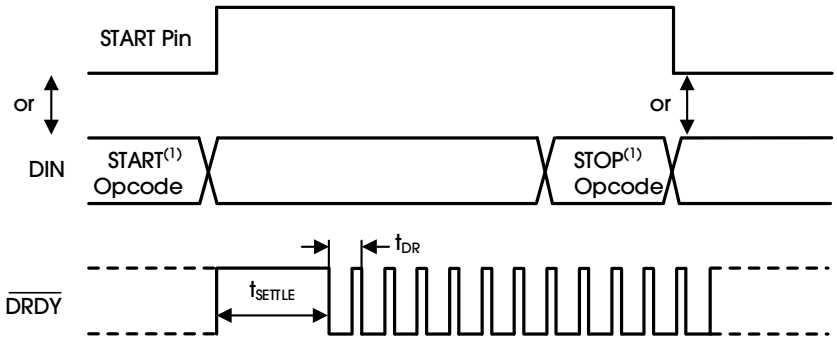


Figure 56. $\overline{DRDY}$ With No Data Retrieval in Single-Shot Mode

单次转换模式提供了一个不需要标准和连续数据率的应用。发出一个 START 指令，或者拉高 START 引脚来复位数字滤波器，有效的将数据率降低 4 倍。这个给模式使得系统更容易受到混叠的影响，因此需要更复杂的模拟和数字滤波。主处理器的负载会增加，因为它必须切换 START 引脚或发送 START 指令来启动新的转换周期。

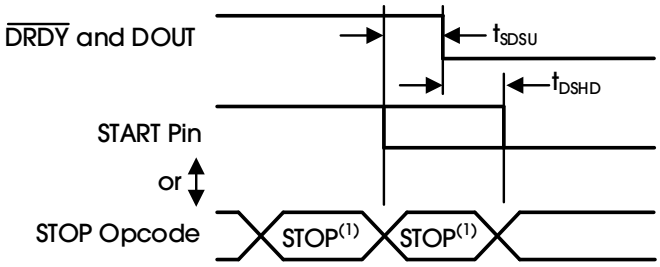
8.4.1.5 连续转换模式

当 START 引脚被持续拉高至少 2 t_{CLK} 或 START 指令被发送时，转换就开始了。如 Figure 57 所示，当转换开始时$\overline{DRDY}$变高，当数据准备好时变低。转换将无限连续，直到 START 引脚被拉低或者 STOP 指令被发送。当 START 引脚被拉低或者 STOP 指令被发送，正在处理的转换允许完成。Figure 58 和 Table 30 所示为在该模式下控制转换要求的$\overline{DRDY}$相对于 START 引脚和 START 指令和 STOP 指令的时序。为了保持转换器持续工作，把 START 引脚永久拉高。当要切换单次获取模式到连续转换模式时，使 START 信号产生脉冲信号(pulse the START signal)或者发送一个 STOP 指令紧接着一个 START 指令。该转换模式非常适用于需要连续转换数据流的应用。



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 57. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 58. START to $\overline{DRDY}$ Timing

Table 30. Timing Requirements for Figure 58

PARAMETER	SYMBOL	MIN	MAX	UNITS
START Pin Low or STOP Opcode to $\overline{DRDY}$ Setup Time to Halt Further Conversions	t_{SDSU}	16		t_{CLK}
START Pin Low or STOP Opcode to Complete Current Conversion	t_{DSHD}	16		t_{CLK}

注：START 和 STOP 命令在操作码传输结束时的第七个 SCLK 下降沿生效。

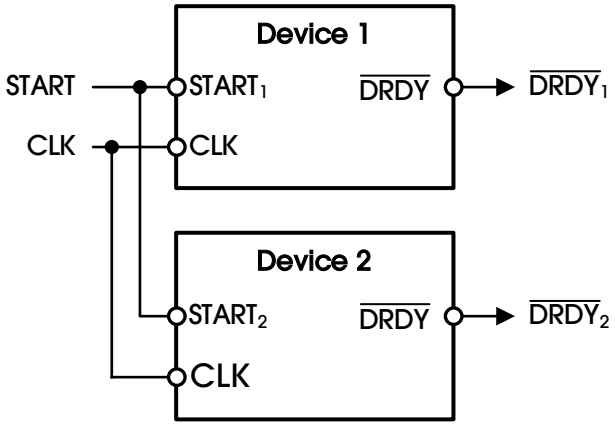
8.4.2 多设备配置

当系统中连接多个器件时，AFE95x 可提供配置灵活性。串行接口通常需要四个信号：DIN、DOUT、SCLK 和$\overline{CS}$。通过在每个器件上添加一个额外的片选信号，可以将多个器件连接在一起。连接 n 个器件所需的信号数量为 3 + n。

如 RLD CONFIGURATION WITH MULTIPLE DEVICES 部分中所述以菊花链方式连接 RLD 放大器。要以菊花链配置使用内部振荡器，将其中一个器件设置为时钟源的主器件并启用内部振荡器(CLKSEL 引脚 = 1)，并通过将CLK_EN寄存器位设置为 1 从器件获取内部振荡器时钟。使用该主器件时钟作为其他器件的外部时钟源。

在使用多个器件时，将这些器件与 START 信号同步。从 START 信号到$\overline{DRDY}$信号的延迟对于一定数据速率是固定的(有关建立时间的更多详细信息，请参阅 START MODE 部分)。作为一个例子，Figure 59 显示了两个器件与 START 信号同步时的行为。

可使用两种配置以最佳接口引脚数来连接多个器件：级联或菊花链。



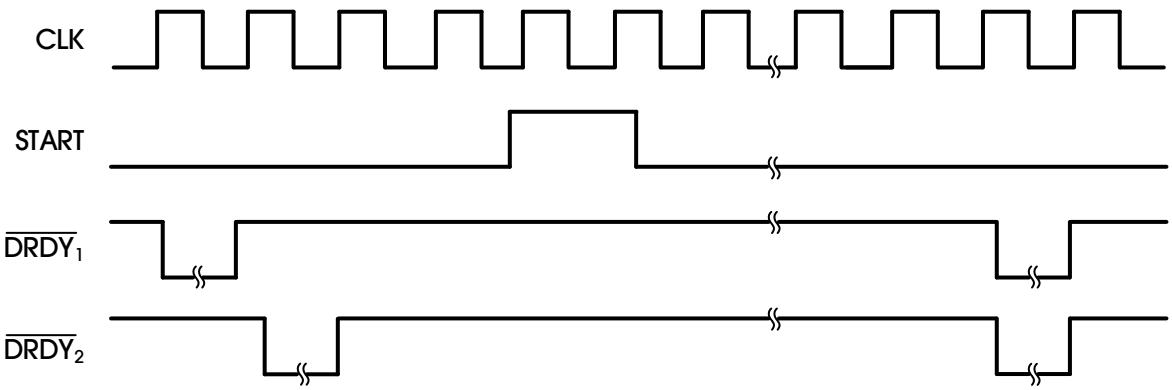


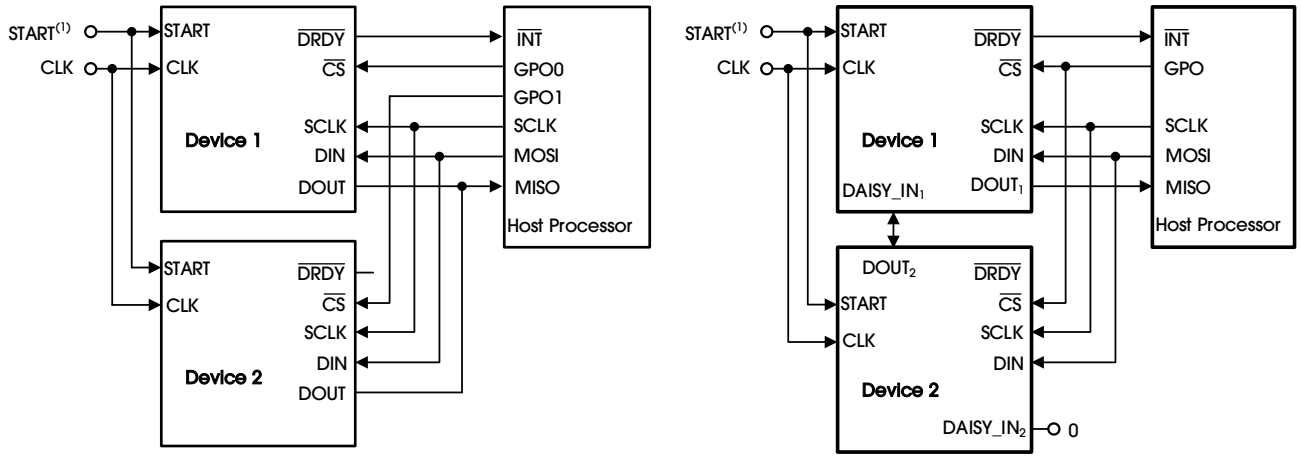
Figure 59. Synchronizing Multiple Converters

8.4.2.1 级联配置

Figure 60(a)展示了两个器件级联在一起的配置。其中一个器件是 AFE958 (八个通道)，另一个器件是 AFE954 (四个通道)。它们一起创建了一个具有 12 个通道的系统。DOUT、SCLK 和 DIN 是共享的。每个器件都具有自己的片选引脚。如果没有选择某个器件(通过将相应的$\overline{CS}$驱动为逻辑 1)，则该器件的 DOUT 处于高阻抗。该结构允许其他器件控制 DOUT 总线。该配置方法适用于大多数应用。

8.4.2.2 菊花链配置

可通过设置 CONFIG1 寄存器中的$\overline{DAISY_EN}$位来启用菊花链模式。Figure 60 (b)显示了菊花链配置。在该配置中，SCLK、DIN 和$\overline{CS}$在在多个器件之间共享。将第一个器件的 DOUT 引脚连接到下一个器件的 DAISY_IN 引脚，从而创建一个链。在每个数据集之间发出一个额外的 SCLK。请注意，在使用菊花链模式时，多读回功能不可用。如果不使用 DAISY_IN 引脚，则将其与数字接地短接。Figure 3 和 Figure 4 介绍了 Figure 61 所示的 AFE958 所需的时序。来自 AFE958 的数据首先出现在 DOUT 上，然后是不相关的位，最后是来自 AFE954 的状态字和数据字。



a) Cascaded Configuration

b) Daisy-Chain Configuration

(1) To reduce pin count, set the START pin low and use the START opcode command to synchronize and start conversions.

Figure 60. Multiple Device Configurations

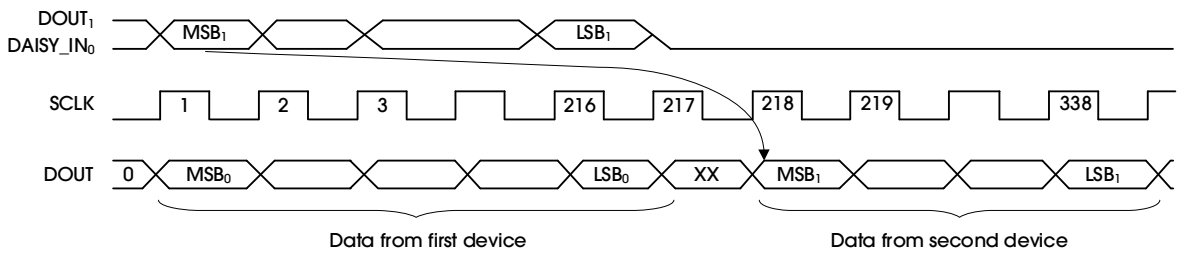


Figure 61. Daisy-Chain Timing for Figure 60(b) with DAISY_ONE_BIT = 1

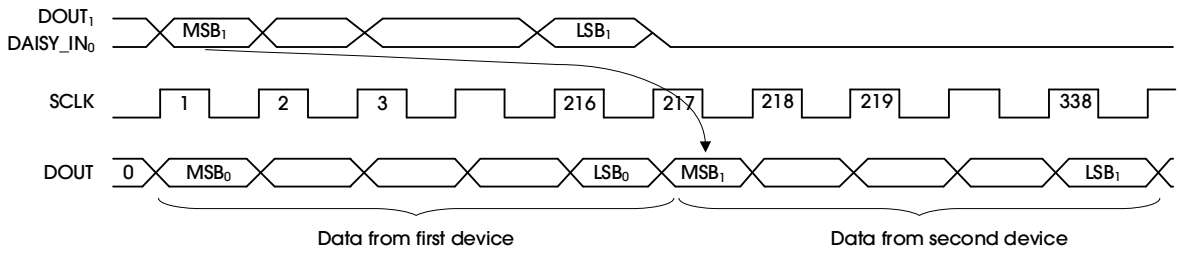


Figure 62. Daisy-Chain Timing for Figure 60(b) with DAISY_ONE_BIT = 0

使用菊花链模式时的重要提醒：

1. 在每个数据集之间发出一个额外的 SCLK (请参阅 Figure 61)。
2. 所有器件都配置为相同的寄存器值，因为$\overline{CS}$是共享的。
3. 器件寄存器读回(RREG)仅对菊花链中的器件 0 有效。只能将转换数据从器件 1 读取到器件 N 中，其中 N 是链中的最后一个器件；无法读取寄存器数据。

如果链中的所有器件都在相同的寄存器设置下运行，则可以共享 DIN，从而将 SPI 通信信号数量减少为 4，无论器件数量如何都是如此。不过，无法对单个器件进行编程；因此，无法在多个器件之间共享 RLD 驱动程序。此外，必须使用外部时钟。

如 Figure 3 和 Figure 4 所示，SCLK 上升沿会在 DOUT 上将数据从 AFE958 移出。SCLK 上升沿还用于将数据锁存到链中的器件 DAISY_IN 引脚。该架构可实现更快的 SCLK 速率，但它也使接口对板级信号延迟非常敏感。链中的器件越多，遵守启动和保持时间就越具有挑战性。SCLK 与所有器件的星型连接(可最大程度地减小 DOUT 的长度)和其他 PCB 布局技术会有所帮助。在 DOUT 和 DAISY_IN 之间放置缓冲器等延迟电路是另一种应对该挑战的方法。另一种选择是在 DOUT 和 DAISY_IN 之间插入一个 D 触发器，该触发器在反相 SCLK 上计时。此外，请注意，菊花链模式需要一些软件开销来重新组合跨字节边界的数据位。

菊花链设备的最大数量取决于设备运行的数据速率。可以使用 Equation 6 估算最大设备数量：

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24} \tag{6}$$

其中：

- N_{BITS} = 设备分辨率(取决于数据速率)
- $N_{CHANNELS}$ = 设备中的通道数(4、6 或 8)

例如，当 AFE958 (8 通道，24 位版本)以 2kSPS 数据速率和 4MHz f_{SCLK} 运行时，最多能够以菊花链方式连接 10 个器件。

8.4.3 电源模式

AFE959 有四种工作模式：

1. 高速模式，数据速率高达 64kSPS
2. 高分辨率模式，数据速率高达 32kSPS
3. 低功耗模式，数据速率高达 16kSPS
4. 超低功耗模式，数据速率高达 8kSPS

按照 Table 31 配置电源模式。

Table 31. Power Mode Configuration for Figure 58

WMODE	HR	HS_MODE	LP2_MODE	MODCLK(1:0)	f_{MOD}	DR(2:0) and ODR
High Speed	1	1	0	2'b10	1.024MHz	DR = 0; ODR = 64kSPS
High Resolution	1	0	0	2'b00	512kHz	DR = 0; ODR = 32kSPS
Low power	0	0	0	2'b00	256kHz	DR = 0; ODR = 16kSPS
Ultra Low Power	0	0	1	2'b11	128kHz	DR = 0; ODR = 8kSPS

8.5 编程

8.5.1 SPI 接口

SPI 兼容串行接口由四个信号组成：$\overline{CS}$、SCLK、DIN、DOUT。该接口可以读转换数据，读写寄存器，和控制 AFE95x 的操作。$\overline{DRDY}$输出是用作提示当数据准备好的状态信号。当新的数据可用时，$\overline{DRDY}$变为低。

8.5.1.1 芯片选择引脚($\overline{CS}$)

片选引脚($\overline{CS}$)选择 AFE95x 设备进行 SPI 通信。当$\overline{CS}$为低时，串行接口为激活状态。整个串行通信中，$\overline{CS}$必须保持低电平。当串行通信完成时，通常等待 4 或者更多个 t_{CLK} 周期再拉高$\overline{CS}$。当$\overline{CS}$被拉高时，串行接口被复位。SCLK,DIN 被忽略，DOUT 输出高阻抗状态。无论$\overline{CS}$的状态为高还是低，$\overline{DRDY}$决定数据何时转换完成(assert)。

当 AFE95x 被选择时，设备尝试每八个串行时钟进行解码和执行指令。如果设备停止执行串行指令，则可能是外部时钟脉冲出现使得串行接口进入一个未知状态。如果要复位串行接口到一个已知状态，把$\overline{CS}$拉高再重新拉低。

8.5.1.2 串行时钟(SCLK)

SCLK 是 SPI 的串行时钟。它用于从设备中转移命令和数据。串行时钟 SCLK 具有一个 Schmitt 触发的输入,使数据按照时钟周期从 DIN 和 DOUT 引脚移入和移出 AFE95x。即使输入有迟滞现象，也要尽可能保持 SCLK 的纯净，以防止因干扰而意外强制执行时钟事件。SCLK 的绝对最大限制时序在 TIMING REQUIREMENTS: SERIAL INTERFACE 中给出。

当 AFE95x 被选择($\overline{CS}$为低)，设备尝试每八个串行时钟进行解码和执行指令。所以，要保持接口在正常的模式下工作，每个串行传输都必须存在八个 SCLK 的倍数的时钟。如果接口因为外部串行时钟而终止，可以通过拉高$\overline{CS}$再拉低来复位。

对于单个设备，SCLK 要求的最低速率由通道个数，通道位数，和输出数据率决定。对于多个级联的设备，查看 CASCADE CONFIGURATION 部分获得具体信息。Equation 7 所示为最小 SCLK 速度的计算。

$$T_{SCLK} < (t_{DR} - 4t_{CLK}) / (N_{BITS} \times N_{CHANNELS} + 24) \quad (7)$$

例如，如果 AFE95x 是工作在 500SPS (八通道，24 位分辨率，)则最小 SCLK 速率为 110kHz。

通过设置设备处于 RDATAC 模式或者发送 RDATA 指令来读取数据。Equation 7 表现的 SCLK 速率限制也同样适用于 RDATAC。对于 RDATA 指令，如果数据必须在两个相连的$\overline{DRDY}$信号之间读取的话，则该限制也适用。Equation 7 是在假定数据获取之间没有其它指令的情况下满足的公式。

8.5.1.2.1 SCLK 时钟方法

有两种不同的 SCLK 计时方法来满足 Figure 2 所示的多字节命令的解码时序要求。

对于 SCLK 的速度要满足图 2 所示的 $t_{SDECODE}$ 的要求。当$\overline{CS}$为低时，连续传输 SCLK。这种方法不能与自由运行的 SCLK 混淆，后者在$\overline{CS}$为高时进行。本设备不支持自由运行的 SCLK。

对于不满足图一所示 $t_{SDECODE}$ 时序要求的更快速的 SCLK，SCLK 是在八位突发模式(burst)中进行传输，传输之间有延迟。在 TIMING REQUIREMENTS: SERIAL INTERFACE 表中规定了绝对最大的 SCLK 限制。Figure 63 所示为本设备的两种不同 SCLK 方法的不同。

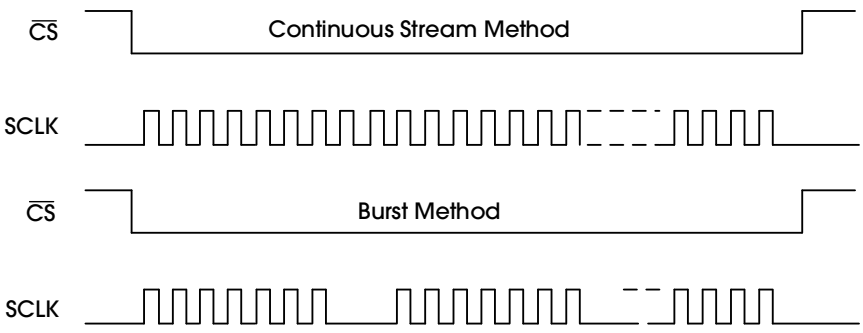


Figure 63. SCLK Clocking Methods

8.5.1.3 数据输入引脚(DIN)

数据输入引脚(DIN)与 SCLK 一起用于 AFE95x (操作码和寄存器数据)通信。该设备将 DIN 的数据锁定在 SCLK 的下降沿上。

8.5.1.4 数据输出引脚(DOUT)

数据输出引脚 DOUT 与 SCLK 一起用于从 AFE95x 在读取转换和寄存器上的数据。DOUT 上的数据在 SCLK 的上升沿移出。当$\overline{CS}$为高时，DOUT 进入高阻抗状态。在连续读数据模式下，DOUT 的输出行还指示何时有新数据可用。使用此功能可以最小化设备与系统控制器之间的连接数量。

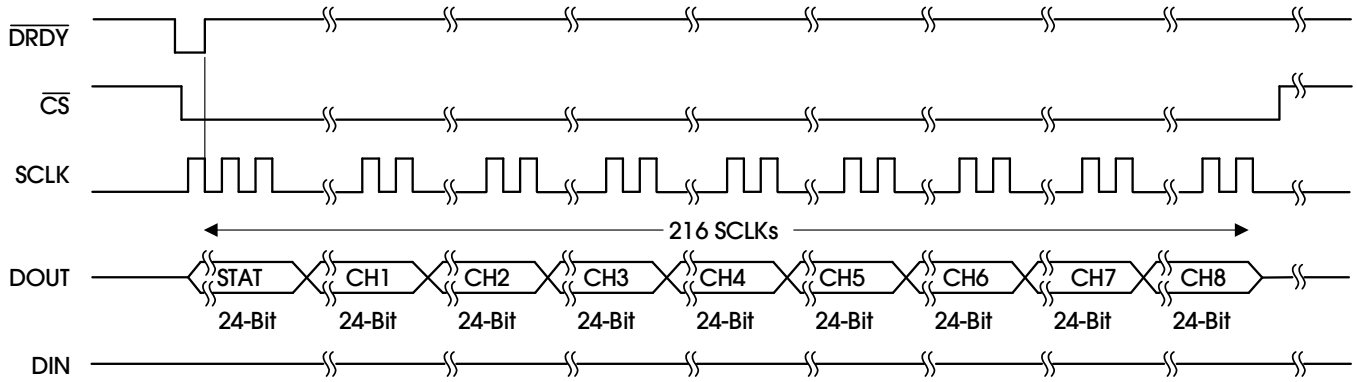


Figure 64. SPI Bus Data Output for the AFE958/AFE959 (Eight Channels)

8.5.2 SPI 命令定义

AFE95x 提供了灵活的配置控制。Table 32 总结的指令命令控制和配置 AFE95x 的操作。除了需要第二个命令字节和数据的寄存器读写操作，其它。其它指令命令都是单独的。在指令之间时，CS可以被拉高或者保持低，但对于整个指令操作(特别是对于多字节命令时)，CS必须保持低。系统指令和 RDATA 指令在第七个 SCLK 的下降沿被 AFE95x 解码。寄存器的读写操作在第八个 SCLK 的下降沿被解码。在发出指令后拉高CS时，确保依据 SPI 的时序要求。

Table 32. Opcode Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE	Third BYTE
SYSTEM COMMANDS				
WAKEUP	Wake up from standby mode	0000 0010 (02h)	—	—
STANDBY	Enter standby mode	0000 0100 (04h)	—	—
RESET	Reset the device	0000 0110 (06h)	—	—
START	Start/restart (synchronize) conversions	0000 1000 (08h)	—	—
STOP	Stop conversion	0000 1010 (0Ah)	—	—
DATA READ COMMANDS				
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	—	—
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	—	—
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	—	—
OFFSETCAL	Offset calibration command. Support ADC channel calibration.	0001 1010 (1Ah)	—	—
REGISTER READ COMMANDS				
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000n nnnn(2)	—
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000n nnnn(2)	—
RREGX	Read *nnnnnnn* registers starting at address *rrr rrrr*	11100100 (E4h)	0rrr rrrr	0nnn nnnn
WREGX	Write *nnnnnnn* registers starting at address *rrrrrrr*	11101000 (E8h)	0rrr rrrr	0nnn nnnn

注 1：当处于 RDATAC 模式时，RREG 命令被忽略。
注 2：n nnnn = 要读取/写入的寄存器数量 – 1。例如，要读取/写入三个寄存器，请设置 n nnnn = 0 (0010)。r rrrr = 读/写操作码的起始寄存器地址。

8.5.2.1 WAKEUP：退出待机模式

WAKEUP 指令退出低功耗待机模式。具体查看 STANDBY: ENTER STANDBY MODE 部分。退出待机模式需要时间。详情见 ELECTRICAL CHARACTERISTICS 部分。在这个命令下，SCLK 的速率没有限制。可以在任何时间发出该指令，但是任何节接下去的指令都必须在 4 个 t_{CLK} 之后送出。

8.5.2.2 STANDBY：进入待机模式

STANDBY 指令进入低功耗待机模式。除了参考部分的其它电路的所有部分全部关闭。待机模式功率消耗在 ELECTRICAL CHARACTERISTICS 部分说明。在这个命令下，SCLK 的速率没有限制。发送 WAKEUP 命令以使设备恢复正常操作。串行接口处于激活状态，所以，在此模式下寄存器的读写是允许的。

8.5.2.3 RESET：复位寄存器到默认值

RESET 指令复位数字滤波器周期(cycle)，并将所有寄存器返回至各自的默认值。详情见 RESET (RESET PIN AND RESET COMMAND)部分。在这个命令下，SCLK 的速率没有限制。可以在任何时间发出该指令。执行复位命令需要 18 个 t_{CLK} 周期的时间。在此段时间内，不要发送任何命令。

8.5.2.4 START：开启转换

该操作码启动数据转换。将 START 引脚拉低以通过命令控制转换。如果转换正在进行中，则此命令无效。STOP 操作码命令用于停止转换。如果 START 命令后紧跟着 STOP 命令，则两个命令之间必须有 4 个 t_{CLK} 周期的间隙。当 START 操作码发送到器件时，保持 START 引脚为低电平，直到发出 STOP 命令。(有关更多详细信息，请参阅 START MODE 部分。)此命令的 SCLK 速率没有限制，可以随时发出。

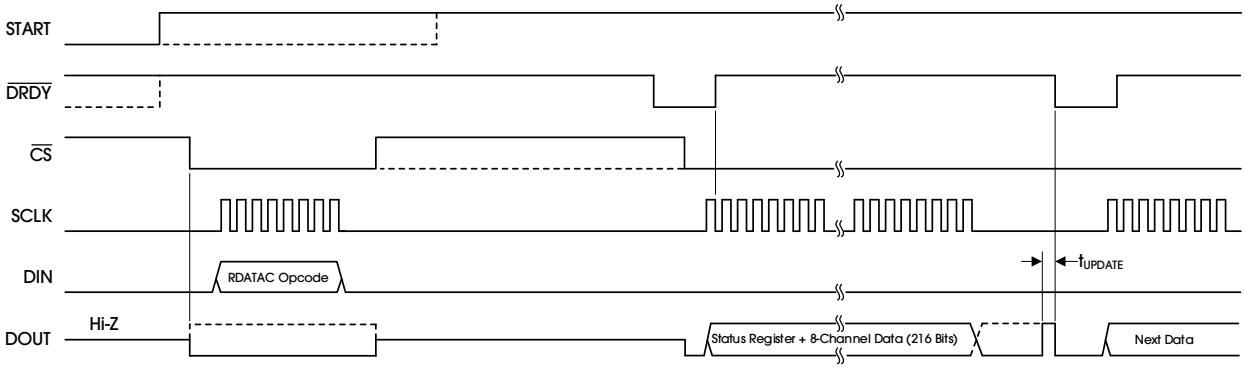
8.5.2.5 STOP：停止转换

STOP 指令停止转换。把 START 引脚拉低，以通过指令控制转换。当 STOP 指令被发送，正在进行的转换完成后，进一步的转换被停止。如果转换已经停止，则此命令没有效果。该命令下对 SCLK 的速率没有限制。可以在任何时间发出该指令。

8.5.2.6 RDATAC：连续读数据

RDATAC 指令支持在每个$\overline{DRDY}$上输出转换数据，而不需要发送后续的读数据指令。该指令将转换数据放在可以将其直接移出(shift out)的输出寄存器中。连续读取数据模式是设备的默认模式。设备在开机和复位时默认为该模式。

RDATAC 模式由停止连续读取数据(SDATAC)指令取消。如果设备处于 RDATA 模式，SDATA 指令必须在任何其它指令之前发送到设备。该命令对 SCLK 的速率没有限制，但是随后的串行数据回读 SCLKs 或 SDATAC 指令必须等待只是 4 t_{CLK}。如 Figure 65 所示，RDATAC 的时序展示了在$\overline{DRDY}$脉冲周围的不能发出该指令的 4 个 t_{CLK} 的保持区。如果没有从设备中回读到数据，DOUT 和$\overline{DRDY}$在此模式下的行为类似。为了在发送 RDATA 指令之后从设备中回读数据，确保 START 引脚为高，或者 START 指令被发送。Figure 65 所示为使用 RDATAC 指令的推荐方法。RDATAC 非常适用于数据记录器或录音机等应用程序，在这些应用程序中，寄存器只设置一次，不需要重新配置。



(1) t_{UPDATE} = 4 / f_{CLK} (where f_{CLK} = 1 / t_{CLK}). Do not read data during this time.

Figure 65. RDATAC Usage

8.5.2.7 SDATAC：停止连续读数据

SDATAC 指令取消连续读取数据模式(RDATAC)。该指令对 SCLK 速率没有限制，但是下一个指令必须等至少 4 t_{CLK} 周期。

8.5.2.8 RDATA：读数据

在$\overline{DRDY}$变为低后，发送 RDATA 指令来读取转换结果(在 SDATAC 模式下)。该指令对 SCLK 没有限制。对下一个指令或者数据回读 SCLKs 也不需要等待时间。在 RDATA 指令发出之后，要从设备中回读数据，需要确保 START 引脚为高或者 START 命令被发送。当用 RDATA 指令读取数据，读操作可以与下一个$\overline{DRDY}$的出现重叠，且不损害数据。Figure 66 所示为使用 RDATA 模式的推荐方法。RDATA 非常适用于心电图和心电图类型的系统，这些应用中，转换的过程中，寄存器必须经常读取或者改变。

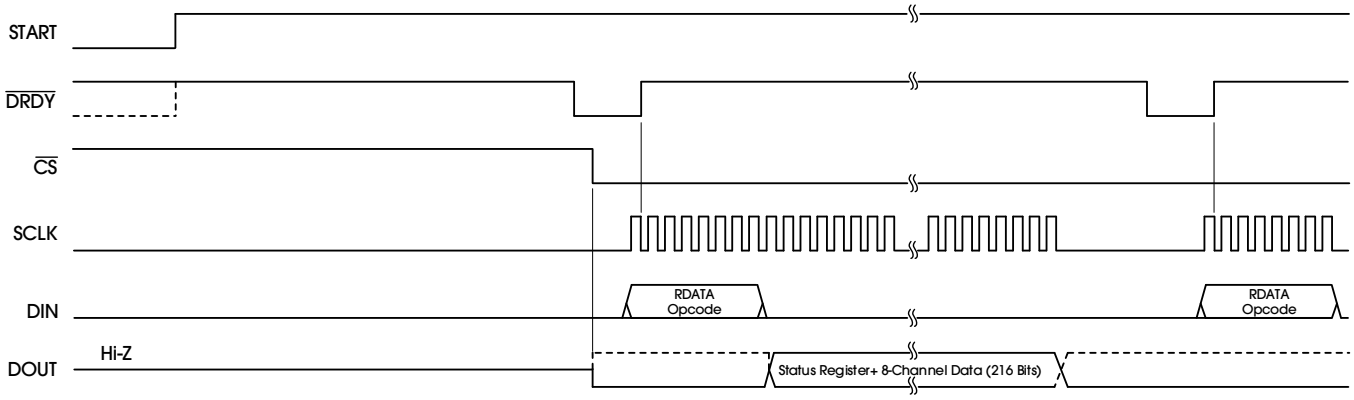


Figure 66. RDATA Usage

8.5.2.9 OFFSETCAL：通道偏移校准

此命令用于取消通道偏移。偏移校准仅适用于 ADC 通道，每次 PGA 增益设置发生变化时都必须执行 OFFSETCAL。最大偏移值不能超过 1/8 × V_{REF} 电压。

8.5.2.10 发送多字节指令

AFE95x 串行接口以字节来解码命令。需要 4 个 t_{CLK} 周期来解码和执行。所以，当发送多字节指令时，需要 4tCLK 周期将一个字节的结束与下一个字节的结束分开。

比如，如果 CLK 是 2.048MHz，则 $t_{SDECODE}$ (4 t_{CLK})是 1.96 微秒。当 SCLK 是 16MHz，一个字节的最大传输速度是 500 纳秒。该字节传输时间不符合 $t_{SDECODE}$ 规范，所以必须插入时间延迟，来保证第二个字节的末端在 1.46 微秒之后到达。而如果 SCLK 是 4MHz，一个字节的传输时间是 2 微秒，因为传输时间超过了 $t_{SDECODE}$ 规范，处理器可以不需要延迟，直接发送下一个字节。在第二种情况下，可以将串行端口编程为多字节传输，而不是满足第一种情况的时序的单个字节传输。

8.5.2.11 RREG：从寄存器读取

RREG 指令读取寄存器数据。RREG 命令是一个 2 字节的指令，跟在后面的为寄存器数据的输出。第一个字节包括命令指令和寄存器地址。操作码的第二个字节指定要读的寄存器数量减一。如果用户想要访问具有上述 0x1F 地址的寄存器，则设置具有固定 0x20h 地址偏移的 ADDR_OFFSET_EN 位，并且在访问完成后，设置 ADDR_OFFSET _DIS 位以清除 0x20h 偏移。

1. 指令的第一个字节：001r rrrr，其中 r rrrr 是起始寄存器的地址。
2. 指令的第二个字节：000n nnnn，其中 n nnnn 是要读的寄存器数减一。

如 Figure 67 所示，操作的第 17 个 SCLK 的上升沿输出第一个寄存器的 MSB。当设备处于连续读取数据模式，在发送 RREG 指令之前需要发送一个 SDATAC 指令。PREG 可以在任何时候发出。然而，因为该指令是一个多字节指令，根据发出 SCLK 的方式，对 SCLK 的速率有一些限制。详情见 SERIAL CLOCK (SCLK)部分。在整个命令过程中，$\overline{CS}$必须保持为低。

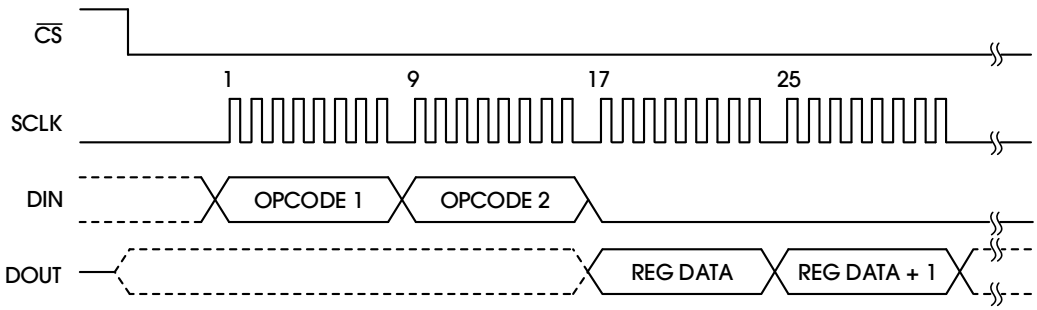


Figure 67. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

8.5.2.12 WREG：写入寄存器

WREG 指令向寄存器写数据。WREG 指令是一个 2 字节指令，跟在其后的寄存器数据输入。第一个字节包含指令操作码和寄存器地址，第二个指令指定要写的寄存器数减 1。如果用户想要访问具有上述 0x1F 地址的寄存器，则设置具有固定 0x20h 地址偏移的 ADDR_OFFSET_EN 位，并且在访问完成后，设置 ADDR_OFFSET _DIS 位以清除 0x20h 偏移。

1. 指令的第一个字节：010r rrrr，其中 r rrrr 是起始寄存器的地址。
2. 指令的第二个字节：010n nnnn，其中 n nnnn 是要读的寄存器数减一。

在操作码字节之后，寄存器数据跟在其后(MSB 格式)。如 Figure 68 所示。WREG 指令可以在任何时候发出，然而，因为该指令为多字节指令，对 SCLK 的速率有一些限制。详情见 SERIAL CLOCK (SCLK)部分。在整个命令过程中，$\overline{CS}$必须保持为低。

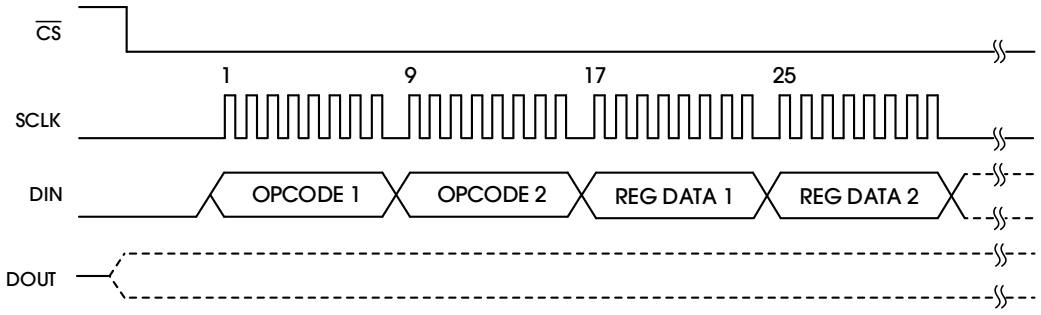


Figure 68. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

8.5.2.13 RREGX：从寄存器读取

RREGX 指令读取寄存器数据。RREG 命令是一个 2 字节的指令，跟在后面的为寄存器数据的输出。第一个字节包括命令指令和寄存器地址。操作码的第二个字节指定要读的寄存器数量减一。

1. 第一个指令字节：11100100 为读取扩展命令寄存器。
2. 第二个指令字节：0rr rrrrr 为起始寄存器地址。
3. 第三个指令字节：0nnn-nnnn 是要读取的寄存器数 – 1。

操作的第 25 个 SCLK 上升沿将第一个寄存器的 MSB 输出，如 Figure 69 所示。当设备处于读取数据连续模式时，有必要在发出 RREGX 命令之前发出 SDTAC 命令。RREGX 命令可以在任何时候发出。但是，由于此命令是一个多字节命令，因此 SCLK 速率受到限制，具体取决于 SCLK 的发布方式。有关更多详细信息，请参阅 SERIAL CLOCK (SCLK)部分。对于整个命令，$\overline{CS}$必须为低。

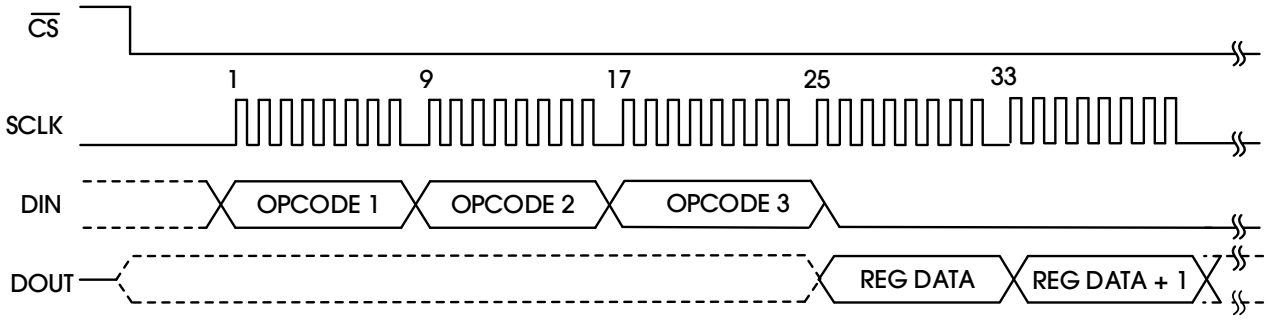


Figure 69. RREGX Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 111000100, OPCODE 2 = 0000 0000, OPCODE 3 = 0000 0001)

8.5.2.14 WREGX：写入寄存器

WREGX 操作码命令写入寄存器数据。WREGX 命令是一个两字节的操作码，后面跟着寄存器数据的输入。第一个字节包含命令操作码和寄存器地址。操作码的第二个字节指定要写入的寄存器数–1。

1. 第一个指令字节：11101000，其中 rrrr 是起始寄存器地址。
2. 第二个指令字节：0rr-rrr 是起始寄存器地址。
3. 第二个操作码字节：0nnn-nnnn 是要写入的寄存器数 – 1。

在操作码字节之后，接下来是寄存器数据(以 MSB 第一格式)，如 Figure 70 所示。WREGX 命令可以在任何时候发出。但是，由于此命令是一个多字节命令，因此 SCLK 速率受到限制，具体取决于 SCLK 的发布方式。有关更多详细信息，请参阅 SERIAL CLOCK (SCLK)部分。对于整个命令，$\overline{CS}$必须为低。

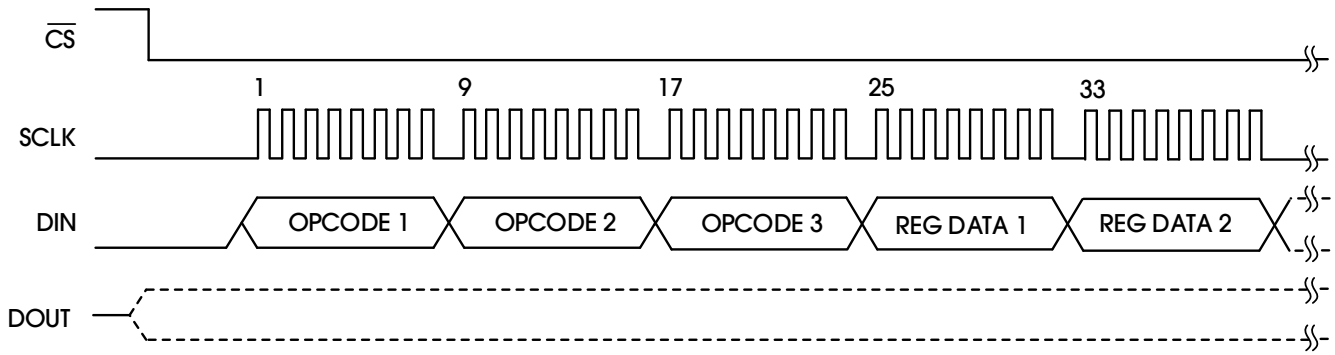


Figure 70. WREGX Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 1110 1000, OPCODE 2 = 0000 0000, OPCODE 3 = 0000 0001)

9. REGISTER MAPS

Table 33 lists the various AFE95x registers.

Table 33. Register Assignments

ADDRESS	REGISTER	RESET (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (READ-ONLY REGISTERS)										
00h	ID	xx	DEV_ID7	DEV_ID6	DEV_ID5	DEV_ID4	DEV_ID3	DEV_ID2	DEV_ID1	DEV_ID0
GLOBAL SETTINGS ACROSS CHANNELS										
01h	CONFIG1	06	HR	$\overline{\text{DAISY\_EN}}$	CLK_EN	MODCLK1	MODCLK0	DR2	DR1	DR0
02h	CONFIG2	40	0	0	WCT_CHOP	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	$\overline{\text{PD\_REFBUF}}$	1	VREF_4V	RSV	RLDREF_INT	$\overline{\text{PD\_RLD}}$	RLD_LOFF_SENS	RLD_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	RSV	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0
CHANNEL-SPECIFIC SETTINGS										
05h	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUX12	MUX11	MUX10
06h	CH2SET	00	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	00	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	00	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET(1)	00	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET(1)	00	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET(1)	00	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET(1)	00	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
0Dh	RLD_SENSP(2)	00	RLD8P(1)	RLD7P(1)	RLD6P(1)	RLD5P(1)	RLD4P	RLD3P	RLD2P	RLD1P
0Eh	RLD_SENSN(2)	00	RLD8N(1)	RLD7N(1)	RLD6N(1)	RLD5N(1)	RLD4N	RLD3N	RLD2N	RLD1N
0Fh	LOFF_SENSP(2)	00	LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
10h	LOFF_SENSN(2)	00	LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
LEAD-OFF STATUS REGISTERS (READ-ONLY REGISTERS)										
12h	LOFF_STATP	00	IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00	IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
GPIO AND OTHER REGISTERS										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1
15h	PACE	00	0	0	0	PACEE1	PACEE0	PACEO1	PACEO0	$\overline{\text{PD\_PACE}}$
16h	RESP	00	RESP_DEMOD_EN1	RESP_MOD_EN1	1	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0
17h	CONFIG4	00	0	0	0	0	SINGLE_ SHOT	WCT_TO_ RLD	$\overline{\text{PD\_LOFF\_ COMP}}$	RESP_43K_FREQ
18h	WCT1	00	aVF_CH6	aVL_CH5	aVR_CH7	avR_CH4	$\overline{\text{PD\_WCTA}}$	WCTA2	WCTA1	WCTA0
19h	WCT2	00	$\overline{\text{PD\_WCTC}}$	$\overline{\text{PD\_WCTB}}$	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0
ENHANCE FEATURE REGISTERS										
1Ah	WCT3	00	WCT_SW7	WCT_SW6	WCT_SW5	WCT_SW4	WCT_SW4_EN	WCT_BUF_LP	0	WCT_BYPASS_BUFB
1Ch	CONFIG5	00	OSC_FSEL1	OSC_FSEL0	0	0	DAISY_ONE_BIT	LOFF_SENS_DEC	HS_MODE	LP2_MODE
1Dh	CONFIG6	32	0	IO_DRV	IO_SLEW	DOUT_DRV	SRB1_INMUX_SW	SRB1_BUFOUT_SW	RLDREF_CTRL3	P5VREF_ON
1Eh	CONFIG7	00	RLD_LOCAL_FB	RLD_INMUX_SW	RESP_CHOP_EN	RESP_PH3	RESP_DR2	RESP_DR1	RESP_DR0	RESP_DR_EN
1Fh	CONFIG8	00	ADDR_OFFSET_EN	GAIN_SET2	GAIN_SET1	GAIN_SET0	SRB2_INMUX_SW	RLV6_INMUX_SW	VDAC_RLDAMP_SW	VDAC_BUFOUT_SW
20h	CONFIG9	40	ACLO_EN	PDB_VREFCM	0	PDB_VDAC_BUF	RLD_LOFF_FORMAT	RLDIN_TOREF_ON	VFEF_4P5V	RLD_RES
21h	LOFF_CFG1	00	RLD_COMP_EN	CUR_LEVEL	ISTEP5	ISTEP4	ISTEP3	ISTEP2	ISTEP1	ISTEP0
22h	LOFF_CFG2	00	AC_EXCT_IMAG2	AC_EXCT_IMAG1	AC_EXCT_IMAG0	RLD_COMP_TH2	RLD_COMP_TH1	RLD_COMP_TH0	DEBOUNCE1	DEBOUNCE0
23h	LOFF_ACLO1	00	ACLO_EN8	ACLO_EN7	ACLO_EN6	ACLO_EN5	ACLO_EN4	ACLO_EN3	ACLO_EN2	ACLO_EN1
24h	LOFF_ACLO2	45	SQUARE_WAVE	ACDIV_FACTOR	IDAC_OFFSET_EN	RLD_DAC_ACEN	ACDIV_FRQ3	ACDIV_FRQ2	ACDIV_FRQ1	ACDIV_FRQ0
25h	REDR2P	00	AC_EXCT_VMAG2	AC_EXCT_VMAG1	AC_EXCT_VMAG0	0	0	WCT_CHOP2	WCT_CHOP1	WCT_CHOP0
26h	CHMUX_MSB	00	CH8_MUX_MSB	CH7_MUX_MSB	CH6_MUX_MSB	CH5_MUX_MSB	CH4_MUX_MSB	CH3_MUX_MSB	CH2_MUX_MSB	CH1_MUX_MSB
27h	LOFF_CMP_FLIP	00	LOFF_CMP_FLIP8	LOFF_CMP_FLIP7	LOFF_CMP_FLIP6	LOFF_CMP_FLIP5	LOFF_CMP_FLIP4	LOFF_CMP_FLIP3	LOFF_CMP_FLIP2	LOFF_CMP_FLIP1
28h	LOFF_SENSN1	00	LOFF8N1	LOFF7N1	LOFF6N1	LOFF5N1	LOFF4N1	LOFF3N1	LOFF2N1	LOFF1N1
29h	LOFF_SENSP1	00	LOFF8P1	LOFF7P1	LOFF6P1	LOFF5P1	LOFF4P1	LOFF3P1	LOFF2P1	LOFF1P1
2Ah	SRB1_COFIG	00	SRB1_SW8	SRB1_SW7	SRB1_SW6	SRB1_SW5	SRB1_SW4	SRB1_SW3	SRB1_SW2	SRB1_SW1

ADDRESS	REGISTER	RESET (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2Bh	RLD_DAC	20	RLD_DACEN	RLD_VREF_SEL	RLD_DAC5	RLD_DAC4	RLD_DAC3	RLD_DAC2	RLD_DAC1	RLD_DAC0
2Ch	XOSC_CFG	04	XOSC_EN	XOSC_DRIVE	CHOP_COMP_MASK	VOTACM_SEL1	VOTACM_SEL0	XOSC_ALCEN	XOSC_DIV1	XOSC_DIV0
34h	MISC_ANA	F0	ADDR_OFFSET_DIS	1	1	1	0	0	RIN_LOFF_EN	LOFF_CMP_FLIPN
35h	MOD_STAT	00	RLD_LOFF_P	RLD_LOFF_N	0	SDC_MODE	STOP	STARNDBY	EFU_UERR	EFU_CERR
36h	CMD_STAT	00	0	OFFSET_CAL_CMD	RDATAC_CMD	RDATA_CMD	REGXRD_CMD	REGXWR_CMD	REG_RD_CMD	REG_WR_CMD
37h	PGAP_OOR_STAT	00	PGA8P_OOR	PGA7P_OOR	PGA6P_OOR	PGA5P_OOR	PGA4P_OOR	PGA3P_OOR	PGA2P_OOR	PGA1P_OOR
38h	PGAN_OOR_STAT	00	PGA8N_OOR	PGA7N_OOR	PGA6N_OOR	PGA5N_OOR	PGA4N_OOR	PGA3N_OOR	PGA2N_OOR	PGA1N_OOR

Note 1: CH5SET and CH6SET are not available for the AFE954. The CH7SET and CH8SET registers are not available for the AFE956.

Note 2: The RLD_SENSP, PACE_SENSP, LOFF_SENSP, LOFF_SENSN, and LOFF_FLIP registers bits(5:4) are not available for the AFE954. Bits(7:6) are not available for the AFE956.

9.1 REGISTER DESCRIPTIONS

The read-only ID control register is programmed during device manufacture to indicate device characteristics.

9.1.1 ID: ID CONTROL REGISTER (ADDRESS = 00H) (RESET = XXH)

Return to the SUMMARY TABLE.

Table 34. ID Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	DEV_ID(7:6)	R	xh	Device revision ID These bits indicate the revision of the device and are subject to change without notice.
5:2	DEV_ID(3:0)	R	xh	Device identification These bits indicate the device. 0010: AFE95x ADC resolution 24 bit
1:0	NU_CH(1:0)	R	xh	Number of channels These bits indicate number of channels of the device identification. 00: 4-channel product 01: 6-channel product 10: 8-channel product 11: Reserved

9.1.2 CONFIG1: CONFIGURATION REGISTER 1 (ADDRESS = 01H) (RESET = 06H)

Table 35. Configuration Register 1 Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>TYPE</th><th>RESET</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>HR</td><td>R/W</td><td>0h</td><td>High-resolution or low-power mode
This bit determines whether the device runs in low-power or high-resolution mode.
0 = LP mode
1 = HR mode</td></tr>
<tr><td>6</td><td>$\overline{\text{DAISY\_EN}}$</td><td>R/W</td><td>0h</td><td>Daisy-chain or multiple readback mode
This bit determines which mode is enabled.
0 = Daisy-chain mode
1 = Multiple readback mode</td></tr>
<tr><td>5</td><td>CLK_EN</td><td>R/W</td><td>0h</td><td>CLK connection(1)
This bit determines whether the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1.
0 = Oscillator clock output disabled
1 = Oscillator clock output enabled</td></tr>
<tr><td>4:3</td><td>MODCLK(1:0)</td><td>R/W</td><td>0h</td><td>Modulator clock setting
00: f_{CLK} / 4 when HR = 1 and f_{CLK} / 8 when HR = 0 (default).
10: f_{CLK} / 2 when HR = 1 and HS_MODE = 1.
Others: Reserved.</td></tr>
<tr><td>2:0</td><td>DR(2:0)</td><td>R/W</td><td>6h</td><td>These bits determine the output data rate of the device.
<table>
<tr><th rowspan="2">BIT</th><th rowspan="2">OVERSAMPLING RATIO</th><th>HS Mode</th><th>HR Mode</th><th>LP Mode</th><th>ULP Mode</th></tr>
<tr><th>DATA RATE(1)</th><th>DATA RATE(1)</th><th>DATA RATE(1)</th><th>DATA RATE(1)</th></tr>
<tr><td>000</td><td>f_{MOD} / 16</td><td>64kSPS</td><td>32kSPS</td><td>16kSPS</td><td>8kSPS</td></tr>
<tr><td>001</td><td>f_{MOD} / 32</td><td>32kSPS</td><td>16kSPS</td><td>8kSPS</td><td>4kSPS</td></tr>
<tr><td>010</td><td>f_{MOD} / 64</td><td>16kSPS</td><td>8kSPS</td><td>4kSPS</td><td>2kSPS</td></tr>
<tr><td>011</td><td>f_{MOD} / 128</td><td>8kSPS</td><td>4kSPS</td><td>2kSPS</td><td>1kSPS</td></tr>
<tr><td>100</td><td>f_{MOD} / 256</td><td>4kSPS</td><td>2kSPS</td><td>1kSPS</td><td>500SPS</td></tr>
<tr><td>101</td><td>f_{MOD} / 512</td><td>2kSPS</td><td>1kSPS</td><td>500SPS</td><td>250SPS</td></tr>
<tr><td>110</td><td>f_{MOD} / 1024</td><td>1kSPS (default)</td><td>500SPS (default)</td><td>250SPS (default)</td><td>125SPS (default)</td></tr>
<tr><td>111</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
</table></td></tr>
</table>

Note: Additional power is consumed when driving external devices.

9.1.3 CONFIG2: CONFIGURATION REGISTER 2 (ADDRESS = 02H) (RESET = 40H)

Table 36. Configuration Register 2 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	1h	Reserved
5	WCT_CHOP	R/W	0h	WCT chopping scheme This bit determines whether the chopping frequency of WCT amplifiers is variable or fixed. 0 = Chopping frequency varies. See Table 23. 1 = Chopping frequency constant at f_{MOD} / 16
4	INT_TEST	R/W	0h	Test source This bit determines the source for the test signal. 0 = Test signals are driven externally. 1 = Test signals are generated internally.
3:2	TEST_AMP(1:0)	R/W	0h	Test signal amplitude These bits determine the calibration signal amplitude. 00 = 1 × (±(VREFP – VREFN)) / 2400V 01 = 2 × (±(VREFP – VREFN)) / 2400V 10 = 10 × (±(VREFP – VREFN)) / 2400V 11 = Reserved
1:0	TEST_FREQ(1:0)	R/W	0h	Test signal frequency These bits determine the calibration signal frequency. 00 = Pulsed at f_{CLK} / 2^{21} 01 = Pulsed at f_{CLK} / 2^{20} 10 = Not used 11 = At dc

9.1.4 CONFIG3: CONFIGURATION REGISTER 3 (ADDRESS = 03H) (RESET = 40H)

Configuration register 3 configures multireference and RLD operation. Return to the SUMMARY TABLE.

Table 37. Configuration Register 3 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	$\overline{\text{PD\_REFBUF}}$	R/W	0h	Power-down reference buffer This bit determines the power-down reference buffer state. 0 = Power-down internal reference buffer 1 = Enable internal reference buffer
6	RESERVED	R/W	1h	Reserved Always write 1h
5	VREF_4V	R/W	0h	Reference voltage This bit determines the reference voltage, VREFP. 0 = VREFP is set to 2.4V. 1 = VREFP is set to 4V (used only with a 5V analog supply).
4	RSV	R/W	0h	Reserved
3	RLDREF_INT	R/W	0h	RLDREF signal This bit determines the RLDREF signal source. 0 = RLDREF signal fed externally 1 = RLDREF signal (AVDD – AVSS) / 2 generated internally
2	$\overline{\text{PD\_RLD}}$	R/W	0h	RLD buffer power This bit determines the RLD buffer power state. 0 = RLD buffer is powered down. 1 = RLD buffer is enabled.
1	RLD_LOFF_SENS	R/W	0h	RLD sense function This bit enables the RLD sense function. 0 = RLD sense is disabled. 1 = RLD sense is enabled.
0	RLD_STAT	R	0h	RLD lead-off status This bit determines the RLD status. 0 = RLD is connected. 1 = RLD is not connected.

9.1.5 LOFF: LEAD-OFF CONTROL REGISTER (ADDRESS = 04H) (RESET = 00H)

The lead-off control register configures the lead-off detection operation. Return to the SUMMARY TABLE.

Table 38. Lead-Off Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	COMP_TH(2:0)	R/W	0h	Lead-off comparator threshold The threshold is used both for InxN/InxP and RLD if RLD_COMP_EN is 0. It is only valid for InxN/InxP if RLD_COMP_EN is 1. Comparator positive side 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4	RSV	R/W	0h	Reserved
3:2	ILEAD_OFF(1:0)	R/W	0h	Lead-off current magnitude It comes from ILEAD_OFF(1:0) when CUR_LEVEL is 0, and the lead-off current magnitude comes from ISTEP(5:0) when CUR_LEVEL is 1. These bits determine the magnitude of current for the current lead-off mode. 00 = 9nA 01 = 18nA 10 = 32nA 11 = 40nA
1:0	FLEAD_OFF(1:0)	R/W	0h	Lead-off frequency when ACLO_EN is 0. These bits determine the frequency of lead-off detect for each channel. 00 = When any bits of the LOFF_SENSP or LOFF_SENSN registers are turned on, make sure that FLEAD(1:0) are either set to 01 or 11. 01 = AC lead-off detection at f_{DR} / 4 10 = Do not use 11 = DC lead-off detection turned on Lead-off frequency is ACDIV_FRQ(3:0) when ACLO_EN is 1. These bits determine the frequency of lead-off detect for each channel. 00 = ACLO lead-off hardware enable. The lead-off frequency is decided by LOFF_ACLO2. 01 = Do not use 10 = Do not use 11 = ACLO lead-off software enable. The lead-off frequency is decided by LOFF_ACLO2.

9.1.6 CHNSET: INDIVIDUAL CHANNEL SETTINGS (N = 1 TO 8) (ADDRESS = 05H TO 0CH) (RESET = 00H)

The CH(1:8)SET control register configures the power mode, PGA gain, and multiplexer settings channels. See the INPUT MULTIPLEXER section for details. CH(2:8)SET are similar to CH1SET, corresponding to the respective channels. Return to the SUMMARY TABLE.

Table 39. Individual Channel Settings (n = 1 to 8) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PDn	R/W	0h	Power-down This bit determines the channel power mode for the corresponding channel. 0 = Normal operation 1 = Channel power-down When powering down a channel, it is recommended that the channel be set to input short by setting the appropriate MUXn(2:0) = 001 of the CHnSET register.
6:4	GAINn(2:0)	R/W	0h	PGA gain These bits determine the PGA gain setting. 000 = 6 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12 111 = 24
3	RESERVED	R/W	0h	Reserved Always write 0h
2:0	MUXn(2:0)	R/W	0h	Channel input These bits determine the channel input selection. Used together with CHMUX_MSB CHx_MUX_MSB to control the input. {CHx_MUX_MSB, MUXn} groups a 4 bits. 0000 = Normal electrode input 0001 = Input shorted (for offset or noise measurements) 010 = Used in conjunction with RLD_MEAS bit for RLD measurements. See the RIGHT LEG DRIVE (RLD) DC BIAS CIRCUIT section for more details. 0011 = MVDD for supply measurement 0100 = Temperature sensor 0101 = Test signal 0110 = RLD_DRP (positive electrode is the driver.) 0111 = RLD_DRN (negative electrode is the driver.) 1000 = RLD_DRPM (both positive and negative inputs are connected to RLDIN.) 1001 = RESP_P/RESP_M 1010 = AFE BYPASS Others = Reserved

9.1.7 RLD_SENSP: RLD POSITIVE SIGNAL DERIVATION REGISTER (ADDRESS = 0DH) (RESET = 00H)

This register controls the selection of the positive signals from each channel for right leg drive (RLD) derivation. See the RIGHT LEG DRIVE (RLD) DC BIAS CIRCUIT section for details. Return to the SUMMARY TABLE.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 40. RLD Positive Signal Derivation Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD8P	R/W	0h	IN8P to RLD Route channel 8 positive signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7P	R/W	0h	IN7P to RLD Route channel 7 positive signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6P	R/W	0h	IN6P to RLD Route channel 6 positive signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5P	R/W	0h	IN5P to RLD Route channel 5 positive signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4P	R/W	0h	IN4P to RLD Route channel 4 positive signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3P	R/W	0h	IN3P to RLD Route channel 3 positive signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2P	R/W	0h	IN2P to RLD Route channel 2 positive signal into RLD channel 0: Disabled 1: Enabled
0	RLD1P	R/W	0h	IN1P to RLD Route channel 1 positive signal into RLD channel 0: Disabled 1: Enabled

9.1.8 RLD_SENSN: RLD NEGATIVE SIGNAL DERIVATION REGISTER (ADDRESS = 0EH) (RESET = 00H)

This register controls the selection of the negative signals from each channel for right leg drive derivation. See the RIGHT LEG DRIVE (RLD) DC BIAS CIRCUIT section for details. Return to the SUMMARY TABLE.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 41. RLD Negative Signal Derivation Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD8N	R/W	0h	IN8N to RLD Route channel 8 negative signal into RLD derivation 0: Disabled 1: Enabled
6	RLD7N	R/W	0h	IN7N to RLD Route channel 7 negative signal into RLD derivation 0: Disabled 1: Enabled
5	RLD6N	R/W	0h	IN6N to RLD Route channel 6 negative signal into RLD derivation 0: Disabled 1: Enabled
4	RLD5N	R/W	0h	IN5N to RLD Route channel 5 negative signal into RLD derivation 0: Disabled 1: Enabled
3	RLD4N	R/W	0h	IN4N to RLD Route channel 4 negative signal into RLD derivation 0: Disabled 1: Enabled
2	RLD3N	R/W	0h	IN3N to RLD Route channel 3 negative signal into RLD derivation 0: Disabled 1: Enabled
1	RLD2N	R/W	0h	IN2N to RLD Route channel 2 negative signal into RLD derivation 0: Disabled 1: Enabled
0	RLD1N	R/W	0h	IN1N to RLD Route channel 1 negative signal into RLD derivation 0: Disabled 1: Enabled

9.1.9 LOFF_SENSP: POSITIVE SIGNAL LEAD-OFF DETECTION REGISTER (ADDRESS = 0FH) (RESET = 00H)

This register selects the positive side from each channel for lead-off detection. See the LEAD-OFF DETECTION section for details. The LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to 1. Return to the SUMMARY TABLE.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 42. Positive Signal Lead-Off Detection Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LOFF8P	R/W	0h	IN8P lead-off Enable lead-off detection on IN8P 0: Disabled 1: Enabled
6	LOFF7P	R/W	0h	IN7P lead-off Enable lead-off detection on IN7P 0: Disabled 1: Enabled
5	LOFF6P	R/W	0h	IN6P lead-off Enable lead-off detection on IN6P 0: Disabled 1: Enabled
4	LOFF5P	R/W	0h	IN5P lead-off Enable lead-off detection on IN5P 0: Disabled 1: Enabled
3	LOFF4P	R/W	0h	IN4P lead-off Enable lead-off detection on IN4P 0: Disabled 1: Enabled
2	LOFF3P	R/W	0h	IN3P lead-off Enable lead-off detection on IN3P 0: Disabled 1: Enabled
1	LOFF2P	R/W	0h	IN2P lead-off Enable lead-off detection on IN2P 0: Disabled 1: Enabled
0	LOFF1P	R/W	0h	IN1P lead-off Enable lead-off detection on IN1P 0: Disabled 1: Enabled

9.1.10 LOFF_SENSN: NEGATIVE SIGNAL LEAD-OFF DETECTION REGISTER (ADDRESS = 10H) (RESET = 00H)

This register selects the negative side from each channel for lead-off detection. See the LEAD-OFF DETECTION section for details. The LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to 1. Return to the SUMMARY TABLE.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 43. Negative Signal Lead-Off Detection Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LOFF8N	R/W	0h	IN8N lead-off Enable lead-off detection on IN8N 0: Disabled 1: Enabled
6	LOFF7N	R/W	0h	IN7N lead-off Enable lead-off detection on IN7N 0: Disabled 1: Enabled
5	LOFF6N	R/W	0h	IN6N lead-off Enable lead-off detection on IN6N 0: Disabled 1: Enabled
4	LOFF5N	R/W	0h	IN5N lead-off Enable lead-off detection on IN5N 0: Disabled 1: Enabled
3	LOFF4N	R/W	0h	IN4N lead-off Enable lead-off detection on IN4N 0: Disabled 1: Enabled
2	LOFF3N	R/W	0h	IN3N lead-off Enable lead-off detection on IN3N 0: Disabled 1: Enabled
1	LOFF2N	R/W	0h	IN2N lead-off Enable lead-off detection on IN2N 0: Disabled 1: Enabled
0	LOFF1N	R/W	0h	IN1N lead-off Enable lead-off detection on IN1N 0: Disabled 1: Enabled

9.1.11 LOFF_FLIP: LEAD-OFF FLIP REGISTER (ADDRESS = 11H) (RESET = 00H)

This register controls the direction of the current used for lead-off derivation. See the LEAD-OFF DETECTION section for details. Return to the SUMMARY TABLE.

Table 44. Lead-Off Flip Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOFF_FLIP8	R/W	0h	Channel 8 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 8 for lead-off derivation. 0: No Flip: IN8P is pulled to AVDD and IN8N pulled to AVSS. 1: Flipped: IN8P is pulled to AVSS and IN8N pulled to AVDD.
6	LOFF_FLIP7	R/W	0h	Channel 7 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 7 for lead-off derivation. 0: No Flip: IN7P is pulled to AVDD and IN7N pulled to AVSS. 1: Flipped: IN7P is pulled to AVSS and IN7N pulled to AVDD.
5	LOFF_FLIP6	R/W	0h	Channel 6 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 6 for lead-off derivation. 0: No Flip: IN6P is pulled to AVDD and IN6N pulled to AVSS. 1: Flipped: IN6P is pulled to AVSS and IN6N pulled to AVDD.
4	LOFF_FLIP5	R/W	0h	Channel 5 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 5 for lead-off derivation. 0: No Flip: IN5P is pulled to AVDD and IN5N pulled to AVSS. 1: Flipped: IN5P is pulled to AVSS and IN5N pulled to AVDD.
3	LOFF_FLIP4	R/W	0h	Channel 4 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 4 for lead-off derivation. 0: No Flip: IN4P is pulled to AVDD and IN4N pulled to AVSS. 1: Flipped: IN4P is pulled to AVSS and IN4N pulled to AVDD.
2	LOFF_FLIP3	R/W	0h	Channel 3 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 3 for lead-off derivation. 0: No Flip: IN3P is pulled to AVDD and IN3N pulled to AVSS. 1: Flipped: IN3P is pulled to AVSS and IN3N pulled to AVDD.
1	LOFF_FLIP2	R/W	0h	Channel 2 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 2 for lead-off derivation. 0: No Flip: IN2P is pulled to AVDD and IN2N pulled to AVSS. 1: Flipped: IN2P is pulled to AVSS and IN2N pulled to AVDD.
0	LOFF_FLIP1	R/W	0h	Channel 1 LOFF polarity flip Flip the pullup/pulldown polarity of the current source or resistor on channel 1 for lead-off derivation. 0: No Flip: IN1P is pulled to AVDD and IN1N pulled to AVSS. 1: Flipped: IN1P is pulled to AVSS and IN1N pulled to AVDD.

9.1.12 LOFF_STATP: LEAD-OFF POSITIVE SIGNAL STATUS REGISTER (ADDRESS = 12H) (RESET = 00H)

This register stores the status of whether the positive electrode on each channel is on or off. See the LEAD-OFF DETECTION section for details. Ignore the LOFF_STATP values if the corresponding LOFF_SENSP bits are NOT set to 1. Return to the SUMMARY TABLE.

When the LOFF_SENSEP bits are 0, the LOFF_STATP bits should be ignored.

Table 45. Lead-Off Positive Signal Status Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IN8P_OFF	R	0h	Channel 8 positive channel lead-off status Status of whether IN8P electrode is on or off 0: Electrode is on. 1: Electrode is off.
6	IN7P_OFF	R	0h	Channel 7 positive channel lead-off status Status of whether IN7P electrode is on or off 0: Electrode is on. 1: Electrode is off.
5	IN6P_OFF	R	0h	Channel 6 positive channel lead-off status Status of whether IN6P electrode is on or off 0: Electrode is on. 1: Electrode is off.
4	IN5P_OFF	R	0h	Channel 5 positive channel lead-off status Status of whether IN5P electrode is on or off 0: Electrode is on. 1: Electrode is off.
3	IN4P_OFF	R	0h	Channel 4 positive channel lead-off status Status of whether IN4P electrode is on or off 0: Electrode is on. 1: Electrode is off.
2	IN3P_OFF	R	0h	Channel 3 positive channel lead-off status Status of whether IN3P electrode is on or off 0: Electrode is on. 1: Electrode is off.
1	IN2P_OFF	R	0h	Channel 2 positive channel lead-off status Status of whether IN2P electrode is on or off 0: Electrode is on. 1: Electrode is off.
0	IN1P_OFF	R	0h	Channel 1 positive channel lead-off status Status of whether IN1P electrode is on or off 0: Electrode is on. 1: Electrode is off.

9.1.13 LOFF_STATN: LEAD-OFF NEGATIVE SIGNAL STATUS REGISTER (ADDRESS = 13H) (RESET = 00H)

This register stores the status of whether the negative electrode on each channel is on or off. See the LEAD-OFF DETECTION section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are NOT set to 1. Return to the SUMMARY TABLE.

When the LOFF_SENSEN bits are 0, the LOFF_STATN bits should be ignored.

Table 46. Lead-Off Negative Signal Status Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IN8N_OFF	R	0h	Channel 8 negative channel lead-off status Status of whether IN8N electrode is on or off 0: Electrode is on. 1: Electrode is off.
6	IN7N_OFF	R	0h	Channel 7 negative channel lead-off status Status of whether IN7N electrode is on or off 0: Electrode is on. 1: Electrode is off.
5	IN6N_OFF	R	0h	Channel 6 negative channel lead-off status Status of whether IN6N electrode is on or off 0: Electrode is on. 1: Electrode is off.
4	IN5N_OFF	R	0h	Channel 5 negative channel lead-off status Status of whether IN5N electrode is on or off 0: Electrode is on. 1: Electrode is off.
3	IN4N_OFF	R	0h	Channel 4 negative channel lead-off status Status of whether IN4N electrode is on or off 0: Electrode is on. 1: Electrode is off.
2	IN3N_OFF	R	0h	Channel 3 negative channel lead-off status Status of whether IN3N electrode is on or off 0: Electrode is on. 1: Electrode is off.
1	IN2N_OFF	R	0h	Channel 2 negative channel lead-off status Status of whether IN2N electrode is on or off 0: Electrode is on. 1: Electrode is off.
0	IN1N_OFF	R	0h	Channel 1 negative channel lead-off status Status of whether IN1N electrode is on or off 0: Electrode is on. 1: Electrode is off.

9.1.14 GPIO: GENERAL-PURPOSE I/O REGISTER (ADDRESS = 14H) (RESET = 0FH)

The general-purpose I/O register controls the action of the three GPIO pins. Return to the SUMMARY TABLE.

Table 47. General-Purpose I/O Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	GPIOD(4:1)	R/W	0h	GPIO data These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.
3:0	GPIOC(4:1)	R/W	Fh	GPIO control (corresponding GPIOD) These bits determine whether the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input

9.1.15 PACE: PACE DETECT REGISTER (ADDRESS = 15H) (RESET = 00H)

This register provides the pace controls that configure the channel signal used to feed the external pace detect circuitry. See the PACE DETECT section for details. Return to the SUMMARY TABLE.

Table 48. Pace Detect Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	0h	Reserved Always write 0h
5	SRB1_GLOBAL	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to all 4, 6, or 8 channels inverting inputs. If it is one, the SRB1_CONFIG configuration value will be ignored. 0: Switches are open. 1: Switches are closed.
4:3	PACEE(1:0)	R/W	0h	Pace even channels These bits control the selection of the even number channels available on TEST_PACE_OUT1. Only one channel may be selected at any time. 00 = Channel 2 01 = Channel 4 10 = Channel 6 (AFE956, AFE958, and AFE959) 11 = Channel 8 (AFE958 and AFE959)
2:1	PACEO(1:0)	R/W	0h	Pace odd channels These bits control the selection of the odd number channels available on TEST_PACE_OUT2. Only one channel may be selected at any time. 00 = Channel 1 01 = Channel 3 10 = Channel 5 (AFE956/AFE958 only) 11 = Channel 7 (AFE958 only)
0	$\overline{\text{PD\_PACE}}$	R/W	0h	Pace detect buffer This bit is used to enable/disable the pace detect buffer. 0 = Pace detect buffer turned off. 1 = Pace detect buffer turned on.

9.1.16 RESPIRATION CONTROL REGISTER (ADDRESS = 16H) (RESET = 00H)

This register provides the controls for the respiration circuitry.

Table 49. Respiration Control Register Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>TYPE</th><th>RESET</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>RESP_DEMOD_EN1</td><td>R/W</td><td>0h</td><td>Enable the respiration demodulation circuitry
This bit enables or disables the demodulation circuitry on channel 1.
0 = RESP demodulation circuitry turned off
1 = RESP demodulation circuitry turned on</td></tr>
<tr><td>6</td><td>RESP_MOD_EN1</td><td>R/W</td><td>0h</td><td>Enable the respiration modulation circuitry
This bit enables or disables the modulation circuitry on channel 1.
0 = RESP modulation circuitry turned off
1 = RESP modulation circuitry turned on</td></tr>
<tr><td>5</td><td>RESERVED</td><td>R/W</td><td>0h</td><td>Always write 1h</td></tr>
<tr><td>4:2</td><td>RESP_PH(2:0)</td><td>R/W</td><td>0h</td><td>Respiration phase(1)
RESP_PH(3) is RESP_PH_MSB.
<table>
<tr><th>RESP_PH(3:0)</th><th>RESP_FREQ(2:0) = 3’b001 and RESP_43K_FREQ = 1’b0 (32kHz)</th><th>RESP_FREQ(2:0) = 3’b001 and RESP_43K_FREQ = 1’b1 (43kHz)</th><th>RESP_FREQ(2:0) = 3’b000 and RESP_43K_FREQ = 1’b0 (64kHz)
RESP_43K_FREQ = 1’b1 (43kHz)</th></tr>
<tr><td>0000</td><td>0° (default)</td><td>0° (default)</td><td>0° (default)</td></tr>
<tr><td>0001</td><td>11.25°</td><td>7.5°</td><td>22.5°</td></tr>
<tr><td>0010</td><td>22.5°</td><td>22.5°</td><td>45°</td></tr>
<tr><td>0011</td><td>33.75°</td><td>30°</td><td>67.5°</td></tr>
<tr><td>0100</td><td>45°</td><td>45°</td><td>90°</td></tr>
<tr><td>0101</td><td>56.25°</td><td>52.5°</td><td>112.5°</td></tr>
<tr><td>0110</td><td>67.5°</td><td>67.5°</td><td>135°</td></tr>
<tr><td>0111</td><td>78.75°</td><td>75°</td><td>157.5°</td></tr>
<tr><td>1000</td><td>90°</td><td>90°</td><td>Not available</td></tr>
<tr><td>1001</td><td>101.25°</td><td>97.5°</td><td>Not available</td></tr>
<tr><td>1010</td><td>112.5°</td><td>112.5°</td><td>Not available</td></tr>
<tr><td>1011</td><td>123.75°</td><td>120°</td><td>Not available</td></tr>
<tr><td>1100</td><td>135°</td><td>135°</td><td>Not available</td></tr>
<tr><td>1101</td><td>146.25°</td><td>142.5°</td><td>Not available</td></tr>
<tr><td>1110</td><td>157.5°</td><td>157.5°</td><td>Not available</td></tr>
<tr><td>1111</td><td>168.75°</td><td>165°</td><td>Not available</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>RESP_CTRL(1:0)</td><td>R/W</td><td>0h</td><td>Respiration control
These bits set the mode of the respiration circuitry.
00 = No respiration
01 = External respiration
10 = Internal respiration with internal signals
11 = Internal respiration with user-generated signals</td></tr>
</table>

Note: The RESP_PH(3:0) phase control bits only for internal respiration (RESP_CTRL = 10) and external respiration (RESP_CTRL = 01) modes when the CONFIG4.RESP_FREQ(2:0) register bits are 000b or 001b.

9.1.17 CONFIG4: CONFIGURATION REGISTER 4 (ADDRESS = 17H) (RESET = 00H)

Return to the SUMMARY TABLE.

Table 50. Configuration Register 4 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	0	R/W	0h	Must write to 0
4	RESERVED	R/W	0h	Reserved Always write 0h
3	SINGLE_SHOT	R/W	0h	Single-shot conversion This bit sets the conversion mode. 0 = Continuous conversion mode 1 = Single-shot mode
2	WCT_TO_RLD	R/W	0h	Connect WCT to RLD This bit connects WCT to RLD. 0 = WCT to RLD connection off 1 = WCT to RLD connection on
1	PD_LOFF_COMPn	R/W	0h	Lead-off comparator power-down This bit powers down the lead-off comparators. 0 = Lead-off comparators disabled 1 = Lead-off comparators enabled
0	RESP_43K_FREQ	R/W	0h	Respiration excitation frequency (42.667kHz or not) 0 = The respiration excitation frequency is decided by RESP_FREQ(2:0). 1 = The respiration excitation frequency is 42.667kHz and RESP_FREQ(2:0) must be set to 3'b000 or 3'b001.

Note: These frequencies assume f_{CLK} = 2.048MHz.

9.1.18 WCT1: WILSON CENTRAL TERMINAL AND AUGMENTED LEAD CONTROL REGISTER (ADDRESS = 18H) (RESET = 00H)

The WCT1 control register configures the device WCT circuit channel selection and the augmented leads. Return to the SUMMARY TABLE.

Table 51. Wilson Central Terminal and Augmented Lead Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	aVF_CH6	R/W	0h	Enable (WCTA + WCTB) / 2 to the negative input of channel 6 (AFE956, AFE958, and AFE959) 0 = Disabled 1 = Enabled
6	aVL_CH5	R/W	0h	Enable (WCTA + WCTC) / 2 to the negative input of channel 5 (AFE956, AFE958, and AFE959) 0 = Disabled 1 = Enabled
5	aVR_CH7	R/W	0h	Enable (WCTB + WCTC) / 2 to the negative input of channel 7 (AFE958 and AFE959) 0 = Disabled 1 = Enabled
4	aVR_CH4	R/W	0h	Enable (WCTB + WCTC) / 2 to the negative input of channel 4 0 = Disabled 1 = Enabled
3	$\overline{\text{PD\_WCTA}}$	R/W	0h	Power down WCTA 0 = Powered down 1 = Powered on
2:0	WCTA(2:0)	R/W	0h	WCT Amplifier A channel selection, typically connected to RA electrode These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTA amplifier 001 = Channel 1 negative input connected to WCTA amplifier 010 = Channel 2 positive input connected to WCTA amplifier 011 = Channel 2 negative input connected to WCTA amplifier 100 = Channel 3 positive input connected to WCTA amplifier 101 = Channel 3 negative input connected to WCTA amplifier 110 = Channel 4 positive input connected to WCTA amplifier 111 = Channel 4 negative input connected to WCTA amplifier

9.1.19 WCT2: WILSON CENTRAL TERMINAL CONTROL REGISTER (ADDRESS = 19H) (RESET = 00H)

The WCT2 configuration register configures the device WCT circuit channel selection. Return to the SUMMARY TABLE.

Table 52. Wilson Central Terminal Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	$\overline{\text{PD\_WCTC}}$	R/W	0h	Power down WCTC 0 = Powered down 1 = Powered on
6	$\overline{\text{PD\_WCTB}}$	R/W	0h	Power down WCTB 0 = Powered down 1 = Powered on
5:3	WCTB(2:0)	R/W	0h	WCT amplifier B channel selection, typically connected to LA electrode. These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTB amplifier 001 = Channel 1 negative input connected to WCTB amplifier 010 = Channel 2 positive input connected to WCTB amplifier 011 = Channel 2 negative input connected to WCTB amplifier 100 = Channel 3 positive input connected to WCTB amplifier 101 = Channel 3 negative input connected to WCTB amplifier 110 = Channel 4 positive input connected to WCTB amplifier 111 = Channel 4 negative input connected to WCTB amplifier
2:0	WCTC(2:0)	R/W	0h	WCT amplifier C channel selection, typically connected to LL electrode. These bits select one of the eight electrode inputs of channels 1 to 4. 000 = Channel 1 positive input connected to WCTC amplifier 001 = Channel 1 negative input connected to WCTC amplifier 010 = Channel 2 positive input connected to WCTC amplifier 011 = Channel 2 negative input connected to WCTC amplifier 100 = Channel 3 positive input connected to WCTC amplifier 101 = Channel 3 negative input connected to WCTC amplifier 110 = Channel 4 positive input connected to WCTC amplifier 111 = Channel 4 negative input connected to WCTC amplifier

9.1.20 WCT3: WILSON CENTRAL TERMINAL CONTROL REGISTER (ADDRESS = 1AH) (RESET = 00H)

The WCT3 configuration register configures the device WCT circuit channel selection.

Table 53. Wilson Central Terminal Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	WCT_SW7	R/W	0h	WCT SW7 switch 0 = Switch is off. 1 = Switch is on.
6	WCT_SW6	R/W	0h	WCT SW6 switch 0 = Switch is off. 1 = Switch is on.
5	WCT_SW5	R/W	0h	WCT SW5 switch 0 = Switch is off. 1 = Switch is on.
4	WCT_SW4	R/W	0h	WCT SW4 switch 0 = Switch is off. 1 = Switch is on.
3	WCT_SW4_EN	R/W	0h	WCT SW4 switch enable 0: The WCT SW4 switch output is disabled. 1: The WCT SW4 switch output is enabled.
2	WCT_BUF_LP	R/W	0h	WCT buffer lower power mode 0: WCT A, B, C, O buffer high-power mode 1: WCT A, B, C, O buffer low-power mode
1	Reserved	R/W	0h	Must write 0
0	WCT_BYPASS_BUFB	R/W	0h	Bypass WCTB BUF output to WCT buffer switch 0 = Switch is off. 1 = Switch is on.

9.1.21 CONFIG5: CONFIGURATION REGISTER 5 (ADDRESS = 1CH) (RESET = 00H)

The CONFIG5 configuration register configures the device selection.

Table 54. Configuration Register 5 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	IOSC_FSEL	R/W	0h	Internal OSC frequency selection 00: 2.048MHz OSC 01: 1.024MHz OSC 10: 512kHz OSC 11: 256kHz OSC
5:4	Reserved	R/W	0	Must write 0
3	DAISY_ONE_BIT	R/W	0h	Daisy Chain has one additional bit control. 0: Daisy chain has no additional one dummy bit. 1: Daisy chain has additional one dummy bit.
2	LOFF_SENS_DEC	R/W	0h	LOFF SENS current switch standalone mode 0: The Lead-off current is controlled by LOFF_SENSP and LOFF_SENSN, legacy mode. 1: The Lead-off current is controlled by LOFF_SENSP, LOFF_SENSN, LOFF_SENSP1, and LOFF_SENSN1 to use four standalone switches.
1	HS_MODE	R/W	0h	High Speed enable 0: Disable high speed mode 1: Enable high speed mode and HR must configure to one.
0	LP2_MODE	R/W	0h	Low power mode2 enable 0: Disable low power mode2 1: Enable low power mode2 and HR must configure to zero.

9.1.22 CONFIG6: CONFIGURATION REGISTER 6 (ADDRESS = 1DH) (RESET = 32H)

The CONFIG6 configuration register configures the device selection.

Table 55. Configuration Register 6 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0h	Must write 0
6	IO_DRV	R/W	1h	I/O strong driver (3mA) mode enable except the DOUT pin 0 = Strong mode enable 1 = Strong mode disable
5	IO_SLEW	R/W	0h	I/O slew read mode enable 0 = IO slew rate boost mode disable 1 = IO slew rate boost mode enable
4	DOUT_DRV	R/W	0h	DOUT strong driver (3mA) mode enable 0 = Strong mode enable 1 = Strong mode disable
3	SRB1_INPUT_SW	R/W	0h	SRB1 PIN input to mux switch 0 = Switch is off. 1 = Switch is on.
2	SRB1_BUF_SW	R/W	0h	SRB1 output to buffer switch 0 = Switch is off. 1 = Switch is on.
1	RLDREF_CTRL3	R/W	1h	RLD AMP REF selection for RLDREF If RLDREF_INT is 1, this bit will be ignored. If RLDREF_INT is 0, this bit will be valid. 0: RLDREF for RLD_AMP source switch is off. 1: RLDREF for RLD_AMP source switch is on.
0	P5VREF_ON	R/W	0h	P5VERF_ON switch enable 0 = Switch is off. 1 = Switch is on.

9.1.23 CONFIG7: CONFIGURATION REGISTER 7 (ADDRESS = 1EH) (RESET = 00H)

The CONFIG7 configuration register configures the device selection.

Table 56. Configuration Register 7 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD_LOCAL_FB	R/W	0h	RLD local feed back function 0: RLD output route to input switch is off. 1: RLD output route to input switch is on.
6	RLD_INMUX_SW	R/W	0h	RLD reroute to channel INMUX switch 0: The switch is off. 1: The switch is on.
5	Reserved	R/W	0h	Must write 0
4	RESP_PH3	R/W	0h	RESP phase configuration setting to combine the RESP_PH(2:0) of RESP register Check the RESP register details.
3:1	RESP_DR(2:0)	R/W	0h	RESP channel 1 has dedicated DR configuration when RESP_DR_EN is enabled. The Respiration has better performance when using the dedicated ODR setting. Lower ODR has better performance, and the RESP channel 1 ODR must be less than ECG channel ODR. For High Speed and High Resolution modes 000: 16kSPS (f_{MOD} / 64) 001: 8kSPS (f_{MOD} / 128) 010: 4kSPS (f_{MOD} / 256) 011: 2kSPS (f_{MOD} / 512) 100: 1kSPS (f_{MOD} / 1024) 101: 500SPS (f_{MOD} / 2048) 110: 250SPS (f_{MOD} / 4096) For Low Power and Ultra Low power modes 000: 8kSPS (f_{MOD} / 64) 001: 4kSPS (f_{MOD} / 128) 010: 2kSPS (f_{MOD} / 256) 011: 1kSPS (f_{MOD} / 512) 100: 500SPS (f_{MOD} / 1024) 101: 250SPS (f_{MOD} / 2048) 110: 125SPS (f_{MOD} / 4096)
0	RESP_DR_EN	R/W	0h	RESP channel 1 dedicated ODR enable It is suggested to enable this bit when using the respiration function for better performance. 0: RESP channel 1 shares the ODR configuration with the CONFIG1 DR setting. 1: RESP channel 1 uses the dedicated ODR setting with RESP_DR.

9.1.24 CONFIG8: CONFIGURATION REGISTER 8 (ADDRESS = 1FH) (RESET = 00H)

The CONFIG8 configuration register configures the device selection.

Table 57. Configuration Register 8 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ADDR_OFFSET_EN	R/W	0h	SPI RREG and WREG command address adds 0x20h offset enable Software writes to 1 and hardware clears to 0. 0: 0x20h address offset disable 1: 0x20h address offset enabled for RREG and WREG, and it is cleared when ADDR_OFFSET_DIS is 0.
6:4	GAIN_SET(2:0)	R/W	0h	Gain setting with different gain configuration The gain error will increase with gain increase. When using big gain, increase the gain setting. When using small gain, reduce the gain setting. Gain_setting == 3'b000 ? fsc_base : gain_setting == 3'b001 ? (fsc_base <= 4'b1110 : (fsc_base + 4'h1) : 4'b1111) : gain_setting == 3'b010 ? (fsc_base <= 4'b1101 : (fsc_base + 4'h2) : 4'b1111) : gain_setting == 3'b011 ? (fsc_base <= 4'b1100 : (fsc_base + 4'h3) : 4'b1111) : gain_setting == 3'b100 ? (fsc_base >= 4'b0001 : (fsc_base – 4'h1) : 4'b0000) : gain_setting == 3'b101 ? (fsc_base >= 4'b0010 : (fsc_base – 4'h2) : 4'b0000) : gain_setting == 3'b110 ? (fsc_base >= 4'b0011 : (fsc_base – 4'h3) : 4'b0000) : gain_setting == 3'b111 ? 4'b0000;
3	SRB2_INMUX_SW	R/W	0h	SRB2 to input MUX switch enable 0: Switch is disabled. 1: Switch is enabled.
2	RLV6_INMUX_SW	R/W	0h	RLV6 to input MUX switch enable 0: Switch is disabled. 1: Switch is enabled.
1	VDAC_RLDAMP_SW	R/W	0h	VDAC to RLD AMP switch enable 0: Switch is disabled. 1: Switch is enabled.
0	VDAC_BUFOUT_SW	R/W	0h	VDAC to BUFOUT switch enable 0: Switch is disabled. 1: Switch is enabled.

9.1.25 CONFIG9: CONFIGURATION REGISTER 9 (ADDRESS = 20H) (RESET = 40H)

The configuration register configures the device selection.

Table 58. Configuration Register 9 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ACLO_EN	R/W	0h	AC Lead-off Enable control 0 = AC Lead-off disable 1 = AC lead-off enabled to generate the sine waveform
6	PDB_VREFCM	R/W	1h	Power-down VREFCM reference buffer This bit determines the power-down reference buffer state. 0 = Power-down internal reference buffer 1 = Enable internal reference buffer
5	Reserved	R/W	0h	Always write 0
4	PDB_VDAC_BUF	R/W	0h	Power-down VDAC buffer This bit determines the power-down buffer state. 0 = VDAC buffer is disabled. 1 = VDAC buffer is enabled.
3	RLD_LOFF_FORMAT	R/W	0h	RLD LOFF status output to data format enable 0: RLD LOFF status not output to 24 bit status format 1: RLD LOFF status output to 24 bit status format. The format is as below: {4'b1100, LOFF_STATP(7:0), LOFF_STATN(7:0), LOFF_RLDP, LOFF_RLDN, GPIO(5:4)}
2	RLDIN_TOREF_ON	R/W	0h	RLD route to VREF switch control 0: Switch is open. 1: Switch is closed.
1	VREF_4P5V	R/W	0h	Used to select 4.5V 0: The VREF reference is decied by the VREF_4V field. 1: The VREF reference is 4.5V.
0	RLD_RES	R/W	0h	RLD RES selection, PGA resistor to RLD selection 0: Half of resistor is in the path (200K). 1: All resistors are in the path (400K).

9.1.26 LOFF_CFG1: LEAD-OFF CONFIGURATION REGISTER (ADDRESS = 21H) (RESET = 00H)

The LOFF_CFG1 configuration register configures the device LOFF circuit channel selection.

Table 59. Lead-Off Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD_COMP_EN	R/W	0h	RLD dedicated lead-off threshold comparator enable 0 = RLD shares the threshold comparator with the InxP and InxN pins. 1 = RLD uses standalone comparator and needs configure RCOMP_TH(2:0) for threshold setting.
6	CUR_LEVEL	R/W	0h	Lead-off current level selection If this bit is 0, the lead-off IDAC current setting comes from the ILEAD_OFF(1:0) value. 0 = Disable ISTEP value configuration 1 = Enable ISTEP value configuration
5:0	ISTEP(5:0)	R/W	0h	Lead-off current magnitude These bits determine the magnitude of current for the current lead-off mode when CUR_LEVEL is 1; otherwise the current magnitude is decided by the ILEAD_OFF(1:0) fields. 000000 = 0nA and step = 5nA 000001 = 5nA … 111111 = 315A

9.1.27 LOFF_CFG2: LEAD-OFF CONFIGURATION REGISTER (ADDRESS = 22H) (RESET = 00H)

The LOFF_CFG2 configuration register configures the device LOFF circuit channel selection.

Table 60. Lead-Off Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	AC_EXCT_IMAG(7:5)	R/W	0h	AC excitation sine wave amplitude selection for IDAC AC_EXCT_MAG / SINE AC AMPLITUDE 000 (–80nA, 80nA) 001 (–40nA, 40nA) 010 (–20nA, 20nA) 011 (–10nA, 10nA) 100 (–5nA, 5nA) 101 Reserved Reserved Reserved
4:2	RLD_COMP_TH(2:0)	R/W	0h	RLD lead-off comparator threshold These bits determine the lead-off comparator threshold. See the LEAD-OFF DETECTION section for a detailed description. Comparator positive side 000 = 95% (default) 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% (default) 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
1:0	DEBOUNCE(1:0)	R/W	0h	ECG channel lead-off output debounce time 00 = Debounce disable 01 = Debounce time 117ms 10 = Debounce time 117ms 11 = Debounce time 117ms

9.1.28 LOFF_ACLO1: AC LEAD-OFF CONFIGURATION REGISTER (ADDRESS = 23H) (RESET = 00H)

The LOFF_ACLO1 configuration register configures the device LOFF circuit channel selection.

Table 61. AC Lead-Off Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ACLO_EN8	R/W	0h	Channel 8 hardware AC lead-off enable 0 = Channel 8 AC lead-off disable 1 = Channel 8 AC lead-off enable
6	ACLO_EN7	R/W	0h	Channel 7 hardware AC lead-off enable 0 = Channel 7 AC lead-off disable 1 = Channel 7 AC lead-off enable
5	ACLO_EN6	R/W	0h	Channel 6 hardware AC lead-off enable 0 = Channel 6 AC lead-off disable 1 = Channel 6 AC lead-off enable
4	ACLO_EN5	R/W	0h	Channel 5 hardware AC lead-off enable 0 = Channel 5 AC lead-off disable 1 = Channel 5 AC lead-off enable
3	ACLO_EN4	R/W	0h	Channel 4 hardware AC lead-off enable 0 = Channel 4 AC lead-off disable 1 = Channel 4 AC lead-off enable
2	ACLO_EN3	R/W	0h	Channel 3 hardware AC lead-off enable 0 = Channel 3 AC lead-off disable 1 = Channel 3 AC lead-off enable
1	ACLO_EN2	R/W	0h	Channel 2 hardware AC lead-off enable 0 = Channel 2 AC lead-off disable 1 = Channel 2 AC lead-off enable
0	ACLO_EN1	R/W	0h	Channel 1 hardware AC lead-off enable 0 = Channel 1 AC lead-off disable 1 = Channel 1 AC lead-off enable

9.1.29 LOFF_ACLO2: AC LEAD-OFF CONFIGURATION REGISTER (ADDRESS = 24H) (RESET = 45H)

The LOFF_ACLO2 configuration register configures the device LOFF circuit channel selection.

Table 62. AC Lead-Off Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	SQUARE_WAVE	R/W	0h	Square or sine wave for IDAC and VDAC 0: Sine wave and sine magnitude is decided by AC_EXCT_IMAG and AC_EXCT_VMAG. 1: Square wave and square magnitude is decided by ISTEP(5:0) and RLD_DAC(5:0).
6	ACDIV_FACTOR	R/W	1h	AC lead-off test frequency division factor 0: Clock divider factor K = 1 1: Clock divider factor K = 6
5	IDAC_OFFSET_EN	R/W	0h	IDAC_OFFSET_EN is used to generate AC excitation current with a 32*2.5nA offset. 0: No offset for AC excitation current 1: Offset for AC excitation current
4	RLD_DAC_ACEN	R/W	0h	RLD DAC uses sine exaction generated by internal DDS. 0: RLD DAC AC source is disabled. 1: RLD DAC AC source is enabled.
3:0	ACDIV_FRQ(3:0)	R/W	05h	AC signal frequency setting

ACDIV_FRQ	ACDIV_FACTOR = 0	ACDIV_FACTOR = 1
0000	32000Hz AC signal	5333.3Hz AC signal
0001	16000Hz AC signal	2666.6Hz AC signal
0010	8000Hz AC signal	1333.3Hz AC signal
0011	4000Hz AC signal	666.6Hz AC signal
0100	2000Hz AC signal	333.3Hz AC signal
0101	1000Hz AC signal	166.6Hz AC signal
0110	500Hz AC signal	83.3Hz AC signal
0111	250Hz AC signal	41.6Hz AC signal
1000	125Hz AC signal	20.8Hz AC signal
1001	62.5Hz AC signal	10.4Hz AC signal
1010	31.2Hz AC signal	5.2Hz AC signal
1011	15.6HZ AC signal	2.6Hz AC signal
1100	7.8Hz AC signal	1.3Hz AC signal
1101	3.9Hz AC signal	0.6Hz AC signal
Reserved	Reserved	Reserved

9.1.30 REDR2P: RED ROUTE TO CHANNEL POSITIVE REGISTER (ADDRESS = 25H) (RESET = 00H)

The REDR2P configuration register configures the device route channel selection.

Table 63. Red Route to Channel Positive Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	AC_EXCT_VMAG	R/W	0h	AC excitation sine wave amplitude selection for IDAC The AVDD, VREFP source is decided by RLD_VREFH_SELINT. AC_EXCT_VMAG / SINE AC AMPLITUDE 000 / (0V, AVDD or VREFP) 001 / (0V, (AVDD or VREFP) / 2) 010 / (0V, (AVDD or VREFP) / 4) 011 / (0V, (AVDD or VREFP) / 8) 100 / (0V, (AVDD or VREFP) / 16) 101 / (0V, (AVDD or VREFP) / 32) 110 / (0V, (AVDD or VREFP) / 64) 111 / (0V, (AVDD or VREFP) / 128)
4:3	RESERVED	R/W	0h	Must write 0
2:0	WCT_CHOP	R/W	0h	WCT CHOP frequency setting 000: WCT chop frequency f_{MOD} / 16 001: WCT chop frequency f_{MOD} / 2 010: WCT chop frequency f_{MOD} / 4 011: WCT chop frequency f_{MOD} / 8 100: WCT chop frequency f_{MOD} / 32 101: WCT chop frequency f_{MOD} / 64 110: WCT chop frequency f_{MOD} / 128 111: WCT chop frequency is 0.

9.1.31 CHMUX_MSB: CHANNEL MUX MSB CONFIGURATION REGISTER (ADDRESS = 26H) (RESET = 00H)

The channel MUX MSB register configures the device route channel selection.

Table 64. Channel Mux MSB Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CH8_MUX_MSB	R/W	0h	Check CHxSET for the CH8_MUX_MSB function.
6	CH7_MUX_MSB	R/W	0h	Check CHxSET for the CH7_MUX_MSB function.
5	CH6_MUX_MSB	R/W	0h	Check CHxSET for the CH6_MUX_MSB function.
4	CH5_MUX_MSB	R/W	0h	Check CHxSET for the CH5_MUX_MSB function.
3	CH4_MUX_MSB	R/W	0h	Check CHxSET for the CH4_MUX_MSB function.
2	CH3_MUX_MSB	R/W	0h	Check CHxSET for the CH3_MUX_MSB function.
1	CH2_MUX_MSB	R/W	0h	Check CHxSET for the CH2_MUX_MSB function.
0	CH1_MUX_MSB	R/W	0h	Check CHxSET for the CH1_MUX_MSB function.

9.1.32 LOFF_CMP_FLIP: LOFF COMPARATOR FLIP CONTROL REGISTER (ADDRESS = 27H) (RESET = 00H)

Table 65. LOFF Comparator Flip Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LOFF_CMP_FLIP8	R/W	0h	Channel 8 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
6	LOFF_CMP_FLIP7	R/W	0h	Channel 7 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
5	LOFF_CMP_FLIP6	R/W	0h	Channel 6 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
4	LOFF_CMP_FLIP5	R/W	0h	Channel 5 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
3	LOFF_CMP_FLIP4	R/W	0h	Channel 4 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
2	LOFF_CMP_FLIP3	R/W	0h	Channel 3 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
1	LOFF_CMP_FLIP2	R/W	0h	Channel 2 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.
0	LOFF_CMP_FLIP1	R/W	0h	Channel 1 comparator polarity selection This bit controls the direction of the comparator used for lead-off derivation of channel 1. 0 = ECGP connects to comparator positive side, and ECGN connects to comparator negative side (default). 1 = ECGN connects to comparator positive side, and ECGP connects to comparator negative side.

9.1.33 LOFF_SENSN1: NEGATIVE SIGNAL LEAD-OFF DETECTION REGISTER (ADDRESS = 28H) (RESET = 00H)

This register selects the negative side from each channel for lead-off detection. See the LEAD-OFF DETECTION section for details.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 66. Negative Signal Lead-Off Detection Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LOFF8N	R/W	0h	When LOFF_SENS_DEC is 1, channel 8 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
6	LOFF7N	R/W	0h	When LOFF_SENS_DEC is 1, channel 7 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
5	LOFF6N	R/W	0h	When LOFF_SENS_DEC is 1, channel 6 negative switch controller The LOFF_SENSN.LOFFxN is used to contro LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
4	LOFF5N	R/W	0h	When LOFF_SENS_DEC is 1, channel 5 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
3	LOFF4N	R/W	0h	When LOFF_SENS_DEC is 1, channel 4 negative switch controller The LOFF_SENSN.LOFFxN is used to controller LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
2	LOFF3N	R/W	0h	When LOFF_SENS_DEC is 1, channel 3 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
1	LOFF2N	R/W	0h	When LOFF_SENS_DEC is 1, channel 2 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.
0	LOFF1N	R/W	0h	When LOFF_SENS_DEC is 1, channel 1 negative switch controller The LOFF_SENSN.LOFFxN is used to control LOFF_SENSN. The LOFF_SENSN1.LOFFxN is used to control LOFF_SENSN1. 0: Switch is open. 1: Switch is closed.

9.1.34 LOFF_SENSP1: POSITIVE SIGNAL LEAD-OFF DETECTION REGISTER (ADDRESS = 29H) (RESET = 00H)

This register selects the positive side from each channel for lead-off detection. See the LEAD-OFF DETECTION section for details. The LOFF_STATP register bits are only valid if the corresponding LOFF_SENP and LOFF_SENSP1 bits are set to 1.

Registers bits(5:4) are not available for the AFE956, AFE958, or AFE959. Bits(7:6) are not available for the AFE958, or AFE959.

Table 67. Positive Signal Lead-Off Detection Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LOFF8P	R/W	0h	When LOFF_SENS_DEC is 1, channel 8 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
6	LOFF7P	R/W	0h	When LOFF_SENS_DEC is 1, channel 7 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
5	LOFF6P	R/W	0h	When LOFF_SENS_DEC is 1, channel 6 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
4	LOFF5P	R/W	0h	When LOFF_SENS_DEC is 1, channel 5 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
3	LOFF4P	R/W	0h	When LOFF_SENS_DEC is 1, channel 4 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
2	LOFF3P	R/W	0h	When LOFF_SENS_DEC is 1, channel 3 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
1	LOFF2P	R/W	0h	When LOFF_SENS_DEC is 1, channel 2 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.
0	LOFF1P	R/W	0h	When LOFF_SENS_DEC is 1, channel 1 positive switch controller The LOFF_SENSP.LOFFxP is used to control LOFF_SENSP. The LOFF_SENSP1.LOFFxP is used to control LOFF_SENSP1. 0: Switch is open. 1: Switch is closed.

9.1.35 SRB1_CONFIG: SHARE BIAS CONTROLLER REGISTER (ADDRESS = 2AH) (RESET = 00H)

This register selects the 8 channels common negative side. It is valid only when PACE.SRB1_GLOBAL is 0.

Table 68. Share Bias Controller Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	SRB1_SW8	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 8 inverting input. 0: Switches are open. 1: Switches are closed.
6	SRB1_SW7	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 7 inverting input. 0: Switches are open. 1: Switches are closed.
5	SRB1_SW6	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 6 inverting input. 0: Switches are open. 1: Switches are closed.
4	SRB1_SW5	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 5 inverting input. 0: Switches are open. 1: Switches are closed.
3	SRB1_SW4	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 4 inverting input. 0: Switches are open. 1: Switches are closed.
2	SRB1_SW3	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 3 inverting input. 0: Switches are open. 1: Switches are closed.
1	SRB1_SW2	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 2 inverting input. 0: Switches are open. 1: Switches are closed.
0	SRB1_SW1	R/W	0h	Stimulus, reference, and bias 1 This bit connects the SRB1 to channel 1 inverting input. 0: Switches are open. 1: Switches are closed.

9.1.36 RLD_DAC: RLD DAC CONTROLLER REGISTER (ADDRESS = 2BH) (RESET = 20H)

This register is used to control the RLD DAC function.

Table 69. RLD DAC Controller Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD_DACEN	R/W	0h	RLD DAC function enable 0: Disable the RLD DAC path 1: Enable the RLD DAC path
6	RLD_VERF_SEL	R/W	0h	RLD reference selection 0: AVDD is the reference. 1: VREFP is the reference.
5:0	RLD_DAC(5:0)	R/W	0h	RLD DAC voltage setting The voltage source VDAC_SRC is AVDD or VREFP based on the RLD_VREF_SEL bit. 000000: Voltage is VDAC_SRC × 1 / 64. 000001: Voltage is VDAC_SRC × 2 / 64. … 100000: Voltage is VDAC_SRC × 32 / 64 based (default). 111111: Voltage is VDAC_SRC × 63 / 64.

9.1.37 XOSC_CFG: CONFIGURATION REGISTER 12 (ADDRESS = 2CH) (RESET = 00H)

The XOSC_CFG configuration register configures the device selection.

Table 70. Configuration Register 12 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	XOSC_EN	R/W	0h	XOSC active enable 0: XOSC is disabled. 1: XOSC is enabled.
6	XOSC_DRIVE	R/W	0h	XOSC drive level register configuration 0: XOSC Drive level is disabled. 1: XOSC Drive level is enabled.
5	CHOP_COMP_MASK	R/W	0h	PGA Chop bypass function 0: Chop bypass function is enabled, and the chop auto gated function is also enabled when PGA input out of range. 1: Chop bypass function is disabled, and the chop auto gated function is disabled when PGA input out of range.
4:3	VOTACM_SEL(1:0)	R/W	0h	Modulator common-mode voltage selection 00: 2.6V (default) 01: 2.65V 10: 2.5V 11: 2.55V
2	XOSC_ALCEN	R/W	1h	XOSC ALCEN configuration (not used) 0: XOSC ALCEN disable 1: XOSC ALCEN enable
1:0	XOSC_DIV(1:0)	R/W	00	XOSC output frequency when XOSC_EN is set. 00: No XOSC clock output 01: XOSC output frequency is 2.048MHz. 10: XOSC output frequency is 1.024MHz. 11: XOSC output frequency is 512kHz.

9.1.38 MISC_ANA: SPARE FUNCTION REGISTER (ADDRESS = 34H) (RESET = 0FH)

Spare function register for metal fix

Table 71. Spare Function Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ADDR_OFFSET_DIS	R/W	1h	SPI RREG and WREG command address no 0x20h offset Software writes to 1 and hardware clears to 0. 0: Has 0x20h address offset disable for RREG and WREG access. 1: No 0x20h address offset for RREG and WREG access.
6:4	Reserved	R/W	7h	Always write 7h
3:2	Reserved	R/W	0h	Always write 0h
1	RIN_LOFF_EN	R /W	0h	RLD IN lead-off detection enable It controls the RLDIN and RLDOUT lead-off detection. 0: RLD IN lead-off detection is disabled. 1: RLD IN lead-off detection is enabled.
0	LOFF_CMP_FLIPN	R /W	0h	All InxN path lead-off comparator do voltages compare flip function. 0: The flip function is disabled. 1: The flip function is enabled. If the bit is 1, both InxP and InxN DC lead-off must be configured to the source current mode.

9.1.39 MOD_STAT: MOD STATUS REGISTER (ADDRESS = 35H) (RESET = 00H)

Device module internal status register, read only

Table 72. MOD Status Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RLD_LOFF_P	R	0	RLD positive lead-off status 0: No RLD positive lead-off 1: RLD positive lead-off is enabled.
6	RLD_LOFF_N	R	0	RLD negative lead-off status 0: No RLD negative lead-off 1: RLD negative lead-off is enabled.
5	Reserved	R	0	Reserved
4	SDC_MODE	R	0	Device is in STOPC mode. 0: Device is in RDATAC mode. 1: Device is in STOPC mode.
3	STOP	R	0	Device is in stop status when the STOP command is executed, and in start status when the START command is executed. 0: Device is in START status. 1: Device is in STOP status.
2	STANDBY	R	0	Device is in STANDBY status or not. 0: Device is in wakeup status. 1: Device is in standby status.
1	EFU_UERR	R	X	Device initial fault status 0: Device has no fault status. 1: Device has fault status.
0	EFU_CERR	R	X	Device initial warning status 0: Device has no warning status. 1: Device has warning status.

9.1.40 CMD_STAT: COMMAND STATUS REGISTER (ADDRESS = 36H) (RESET = 00H)

Device command status register, read only

Table 73. Command Status Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0	Reserved
6	OFFSET_CAL_CMD	R/W	0	OFFSET Calibration command execute status Software writes 0 to clear it. 0: No OFFSET calibration command is executed. 1: OFFSET calibration command is executed.
5	RDATAC_CMD	R/W	0	RDATAC command execute status Software writes 0 to clear it. 0: No RDATAC command is executed. 1: RDATAC command is executed.
4	RDATA_CMD	R/W	0	RDATA command execute status Software writes 0 to clear it. 0: No RDATA command is executed. 1: RDATA command is executed.
3	REGX_RD_CMD	R/W	0	WREGX command execute status Software writes 0 to clear it. 0: No WREGX command is executed. 1: WREGX command is executed.
2	REGX_WR_CMD	R/W	0	RREGX command execute status Software writes 0 to clear it. 0: No RREGX command is executed. 1: RREG command is executed.
1	REG_RD_CMD	R/W	0	WREG command execute status Software writes 0 to clear it. 0: No WREG command is executed. 1: WREG command is executed.
0	REG_WR_CMD	R/W	0	RREG command execute status Software writes 0 to clear it. 0: No RREG command is executed. 1: RREG command is executed.

9.1.41 PGAP_OOR_STAT: PGA POSITIVE OOR STATUS REGISTER (ADDRESS = 37H) (RESET = 00H)

PGAP out of range status

Table 74. PGA Positive OOR Status Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PGA8P_OOR	R/W	0	Channel 8 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
6	PGA7P_OOR	R/W	0	Channel 7 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
5	PGA6P_OOR	R/W	0	Channel 6 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
4	PGA5P_OOR	R/W	0	Channel 5 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
3	PGA4P_OOR	R/W	0	Channel 4 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
2	PGA3P_OOR	R/W	0	Channel 3 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
1	PGA2P_OOR	R/W	0	Channel 2 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
0	PGA1P_OOR	R/W	0	Channel 1 PGA positive out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range

9.1.42 PGAN_OOR_STAT: PGA NEGATIVE OOR STATUS REGISTER (ADDRESS = 38H) (RESET = 00H)

PGAN out of range status register

Table 75. PGA Negative OOR Status Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	PGA8N_OOR	R/W	0	Channel 8 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
6	PGA7N_OOR	R/W	0	Channel 7 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
5	PGA6N_OOR	R/W	0	Channel 6 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
4	PGA5N_OOR	R/W	0	Channel 5 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
3	PGA4N_OOR	R/W	0	Channel 4 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
2	PGA3N_OOR	R/W	0	Channel 3 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
1	PGA2P_OOR	R/W	0	Channel 2 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range
0	PGA1P_OOR	R/W	0	Channel 1 PGA negative out of range status Software writes 0 to clear it. 0 = Not out of range 1 = Out of range

10. 应用与实现

注

以下应用部分中的信息不是公司组件规范的一部分，公司不保证其准确性或完整性。公司的客户有责任确定组件是否适合他们的用途。客户应验证和测试他们的设计实施以确认系统功能。

10.1 应用信息

10.1.1 设置设备进行基本数据采集

Figure 71 概述了在基本状态下配置器件和采集数据的流程。该流程将器件置于与 SPECIFICATIONS 部分中列出的参数匹配的配置中，以检查器件是否在用户系统中正常工作。请在开始时遵循此流程，直到熟悉器件设置。验证此流程后，可以根据需要配置器件。有关命令时序的详细信息，请参阅数据表中的相应章节。为 ECG 专用功能添加了示例编程代码。

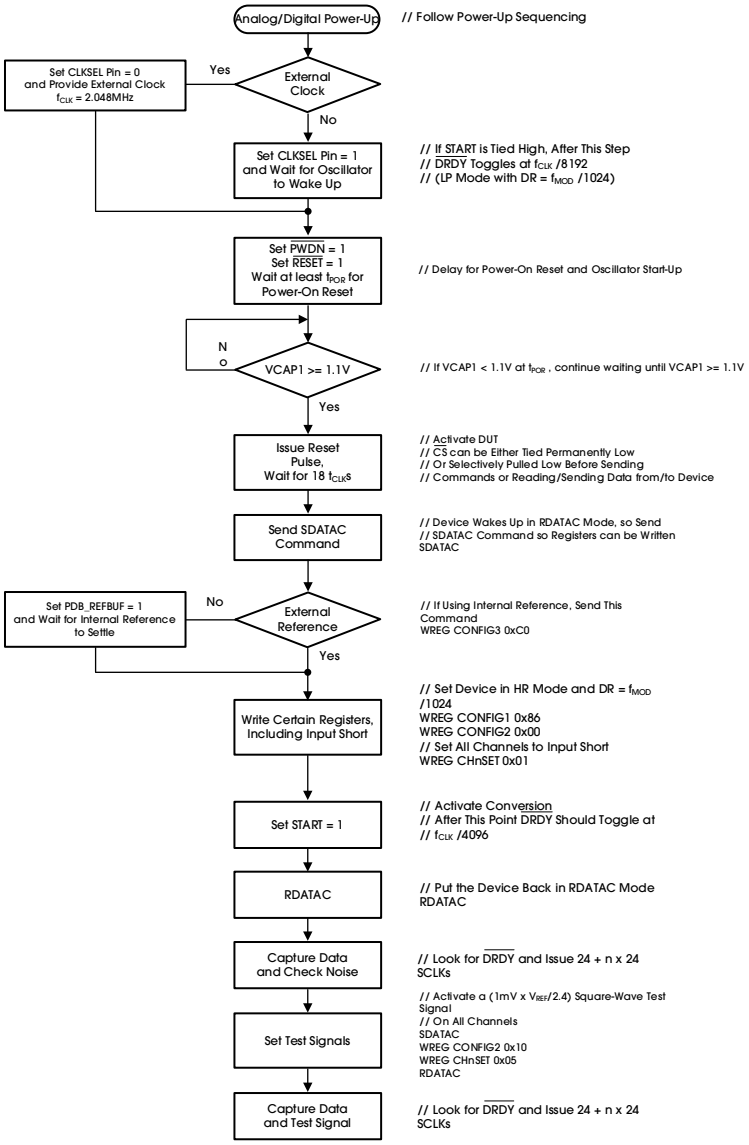


Figure 71. Initial Flow at Power-Up

10.1.1.1 导联脱落

在所有通道上使用上拉或下拉电阻设置直流导联关闭的示例代码：

```
WREG LOFF 0x13          // Comparator threshold at 95% and 5%, pullup or pulldown resistor
// dc lead-off
WREG CONFIG4 0x02       // Turn on dc lead-off comparators
WREG LOFF_SENSP 0xFF    // Turn on the P-side of all channels for lead-off sensing
WREG LOFF_SENSN 0xFF    // Turn on the N-side of all channels for lead-off sensing
```

观察输出数据流的状态位以监控导联脱落状态。

10.1.1.2 右腿驱动

选择 RLD 作为前三个通道的平均值的示例代码。

```
WREG RLD_SENSP 0x07     // Select channel 1-3 P-side for RLD sensing
WREG RLD_SENSN 0x07     // Select channel 1-3 N-side for RLD sensing
WREG CONFIG3 b'x1xx 1100    // Turn on RLD amplifier, set internal RLDREF voltage
```

通过通道 4N 侧路由 RLD_OUT 信号并使用通道 5 测量 RLD 的示例代码。确保芯片 RLDOUT 的外侧连接到 RLDIN。

```
WREG CONFIG3 b'xxx1 1100    // Turn on RLD amp, set internal RLDREF voltage, set RLD measurement bit
WREG CH4SET b'1xxx 0111 // Route RLDIN to channel 4 N-side
WREG CH5SET b'1xxx 0010 // Route RLDIN to be measured at channel 5 w.r.t RLDREF
```

10.1.1.3 起搏检测

选择速度通道 5 和 6 输出的示例代码：

```
WREG PACE b'0001 0101   // Power-up pace amplifier and select channel 5 and 6 for pace out
```

10.1.2 建立输入共模

AFE95x 测量全差分信号，其中共模电压点是正负模拟输入的中点。由于操作所需的裕量，内部 PGA 限制了共模输入范围。人体容易发生共模漂移，因为与天线相类似，噪声很容易耦合到人体上。这些共模漂移可能会将 AFE95x 输入共模电压推出 ADC 的可测量范围。

如果系统使用患者驱动电极，AFE95x 包含一个连接到患者驱动电极的片上右腿驱动(RLD)放大器。RLD 放大器功能是对患者进行偏置，以将其他电极共模电压维持在有效范围内。上电后，放大器使用模拟中间电源电压或 RLDREF 引脚上的电压作为基准输入，以稳定接近于该电压的输出。

AFE95x 提供了使用输入电极电压作为放大器反馈的选项，通过设置 RLD_SENSP 和 RLD_SENSN 寄存器中的相应位，更有效地稳定到放大器基准电压的输出。有关利用此技术的三电极系统的示例，请参阅 Figure 72。

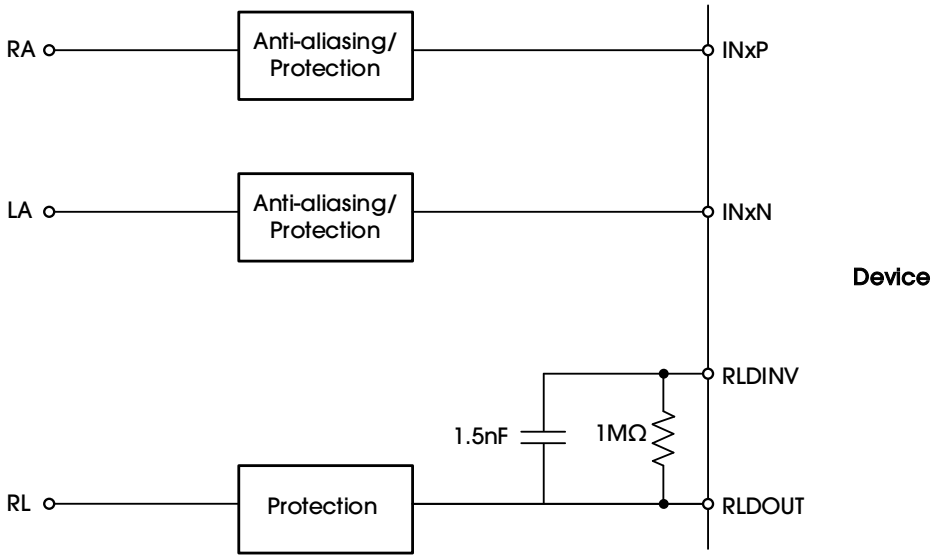


Figure 72. Setting Common-Mode Using RLD Electrode

保持有效共模电压的第二种策略是对模拟输入进行交流耦合，这在未使用患者驱动电极时尤其有用。直流阻断电容器与模拟电源之间的分压器或上拉电阻器相结合，可将直流偏置设置为已知点，从而有效地确保直流共模电压不会漂移。不使用患者驱动电极的应用仍然可以使用 AFE95x 上的 RLD 放大器作为经缓冲的中间电源电压来偏置输入。选择无源元件时要小心，因为电容器和电阻器会形成 RC 高通滤波器。如果不正确地选择无源元件，则滤波器会使信号频带下端的频率不合期望地衰减。Figure 73 显示了该配置的示例。

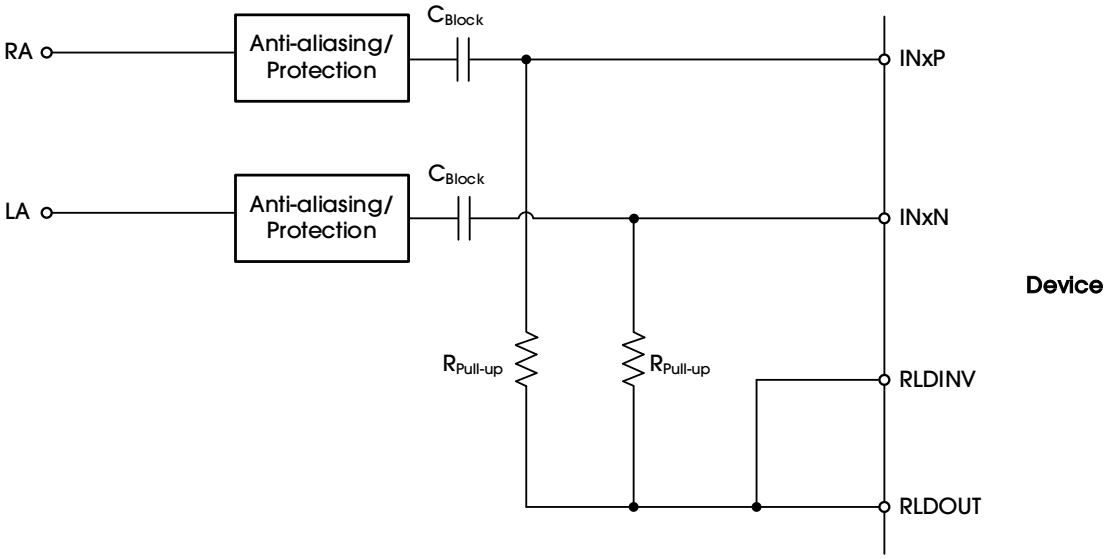


Figure 73. Setting Common-Mode Without Using RLD Electrode

10.1.3 抗锯齿

与所有模数系统一样，应注意防止意外的混叠效应。AFE95x 调制器以 256、512 或 1024kHz 的频率对输入进行采样，具体分别取决于器件处于低功耗(LP)模式还是高分辨率(HR)模式。与所有数字滤波器的情况一样，AFE95x 上的片上数字抽取滤波器的响应以调制器频率的整数倍重复。使用 Δ-Σ 架构的好处是数字抽取滤波器会使信号频带与调制器频率附近信号频带的混叠之间的频率显著地衰减。这种衰减与 PGA 的有限带宽(请参阅 Table 21)相结合，使对模拟抗混叠滤波器响应的陡度要求不那么严格。在许多情况下，调制器频率的可接受衰减由单极或双极 RC 低通滤波器提供。

选择抗混叠组件时也要小心。由于元件不匹配(包括抗混叠元件)，共模到差模的转换会导致共模抑制性能下降。Figure 74 显示了典型的前端配置。

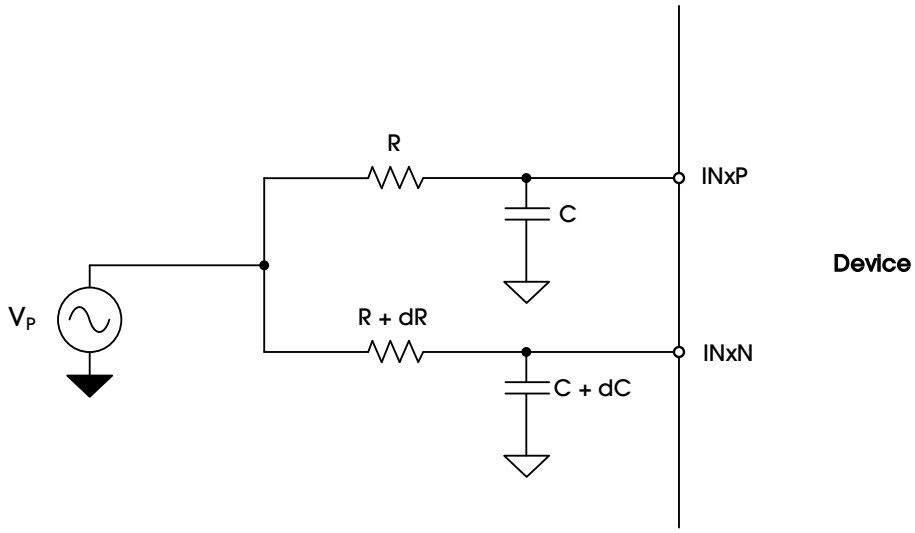


Figure 74. Typical Front-End Configuration

V_P 是系统的共模信号。如果在差分信号中建模的 R 和 C 的值完全匹配，则系统表现出非常大的 CMR。如果电阻器 R 和电容器 C 中的 δR 和 δC 分别不匹配，则整个系统的 CMR 近似 Equation 8。

$$CMR = 20\log\left(\frac{\delta R}{R} + \frac{\delta C}{C}\right) + 20\log\left(\frac{f}{f_C}\right) \quad (8)$$

其中：

- f_C 是 RC 滤波器的–3dB 频率。

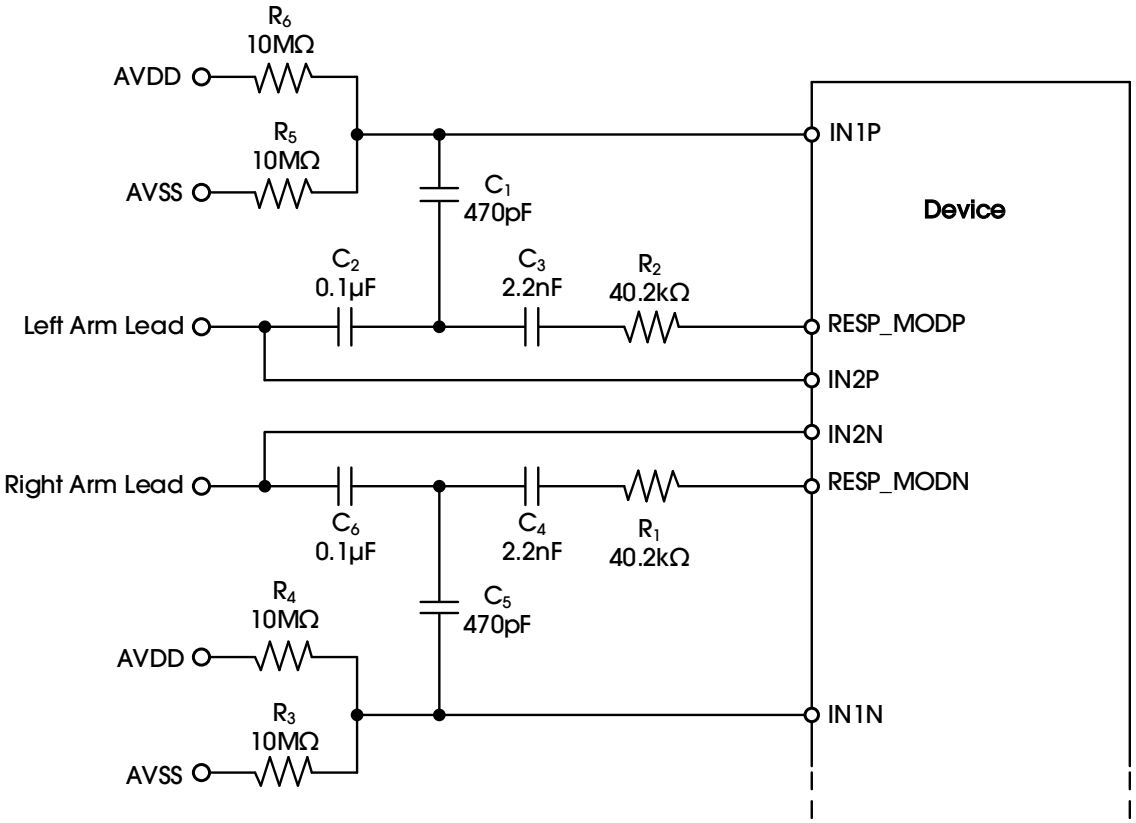
如果使用 1%精度的外部元件并且 RC 滤波器的带宽约为 6kHz，则系统在 60Hz 时仅具有 74dB 的 CMR。在现实世界中，ECG 的前端不仅包含一阶 RC 滤波器，还包括电极、电缆和二阶或三阶 RC 滤波器。考虑到所有这些组件，不匹配很容易累积，因此会贡献高达 20%或更多的信号。在频率为 60Hz 时，这种不匹配程度会使系统的 CMR 降低到 60dB 以下。因此，必须考虑采用不同的技术来改善 CMR。

在调制器前面放置抗混叠滤波器的带宽时存在折衷。考虑到分立元件之间的不匹配，最好选择较大的带宽；带宽的上限由调制器的采样频率决定。

10.2 典型应用

10.2.1 使用内部调制电路的 AFE95x 呼吸测量

AFE95x 上的呼吸测量电路采用带外幅度调制和解调来测量与呼吸相对应的胸阻抗变化。当呼吸模式启用时，通道 1 不能用于采集 ECG 信号，因为内部解调电路是该通道所独有的。如果它们也连接到另一个通道，则仍然可以使用用于呼吸测量的相同电极来采集心电图信号。请注意 Figure 75 中所示的配置。



NOTE: Patient and input protection circuitry not shown.

Figure 75. Typical Respiration Circuitry

10.2.1.1 设计要求

Table 76 显示了 Figure 75 中所示组件的设计要求。

Table 76. Respiration Design Requirements

DESIGN PARAMETER	VALUE
Modulation Frequency	32kHz, 42.677kHz, or 64kHz
Input High-Pass Filter Cutoff	≈ 68Hz
ADC Reference Voltage	2.4V
Maximum AC Body Current	100µA
Minimum Resistance R1 + R2	24kΩ

10.2.1.2 详细设计程序

要将 AFE95x 配置为使用其内部调制电路，请设置 RESP 寄存器位(6:7)以启用内部调制和解调电路。RESP 寄存器位(4:2)决定解调阻塞信号的相位。要将器件配置为使用内部生成的信号进行内部呼吸测量，请将 RESP 寄存器位(1:0)配置为 10b。

当配置为使用内部电路时，RESP_MODP 和 RESP_MODN 引脚会根据 CONFIG4 寄存器位(7:5)产生 32kHz、42.667kHz 或 64kHz 方波。REP_MODP 和 RESP_MODN 引脚电压以指定频率以相反相位在 VREFP 和 VREFN 之间切换。

选择 R_1 和 R_2 需要首先认识到该电路的理想行为。理想情况下，所有串联电容器都对高频调制信号表现为短路，并且电路中任何地方都不存在非理想并联电容。Figure 76 显示了代表这些假设的等效电路。

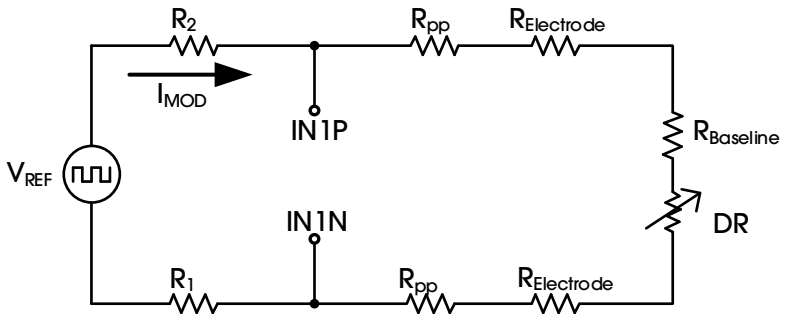


Figure 76. Ideal Behavior of the Respiration Modulation Circuit

通道 1 输入处出现的电压由电路中电阻器形成的分压器设置。电阻器 R_{PP} 代表电缆中的任何患者保护电阻；$R_{Electrode}$ 代表电极与身体的界面电阻；$R_{Baseline}$ 表示基线身体阻抗；ΔR 是呼吸引起的胸阻抗的变化。假设 R_1 和 R_2 明显大于电路中的所有其他电阻，然后根据 Equation 9 将 RESP_MOD 引脚近似为幅度为 I_{MOD} 的交流电流源的端子：

$$I_{MOD} \approx \frac{V_{REF}}{R_1 + R_2} \tag{9}$$

其中：

- V_{RE} 是在 RESP_MOD 引脚处产生的幅度为 VREFP – VREFN 的方波。

根据 IEC60601，频率为 32kHz 的患者电流必须限制在 100μA 以下；该限制对 R_1 和 R_2 的组合施加了最小值。

为了获得最佳性能，AFE95x 的输入必须进行交流耦合并偏置到中间电源。执行此功能的组件对应于 Figure 75 中的 C1、C5、R3、R4、R5 和 R6。ECG 干扰有可能耦合到通道 1 中。由于这种可能性，建议将高这些组件的通滤波器截止足够大，足以显着衰减 ECG 带宽。相反，如果截止设置为高，则载波信号可能会衰减。

通道 1 输入处出现的信号由 PGA 放大，然后馈送到内部解调模块。解调模块从输入中删除方波，仅留下与呼吸引起的 ΔR 相对应的极低频波形，以及 R_{PP}、$R_{Electrode}$ 和 $R_{Baseline}$ 引起的偏移。Equation 10 描述了与身体阻抗变化相对应的调制器输出电压。

$$V_{RESP} = I_{MOD} \times \Delta R \times G_{PGA} \tag{10}$$

通过使用 V_{RESP} 由于 ΔR 而振荡的周期来测量呼吸速率。确保 VRESP 的幅度始终大于 AFE95x 的无噪声分辨率。这一幅度对 R_1 和 R_2 的尺寸以及电缆阻抗 R_{PP} 施加了上限，并且要求电极与身体的连接质量很高。

寄生并联电容往往会衰减高频，并且 PGA 的输出受到放大器带宽的限制。结果是载体的方形边缘被倒圆。为了解决此错误，AFE95x 允许配置 RESP 寄存器中的 RESP_PH(2:0)位。这些位控制解调相位，解调相位在调制和解调时钟之间引入相位延迟，以解决电路中低通元件引入的延迟。

选择最佳相位取决于系统特性。由输入路径中的电阻和电缆电容引入的时间常数是影响最佳呼吸率测量所需的相位量的系统级特性的示例。

Figure 77 显示了呼吸测试电路。Figure 78 和 Figure 79 绘制了扫描基线阻抗、增益和相位时 AFE95x 通道 1 上的噪声。X 轴是基线阻抗，标准化为 29µA 调制电流(参见 Equation 11)。

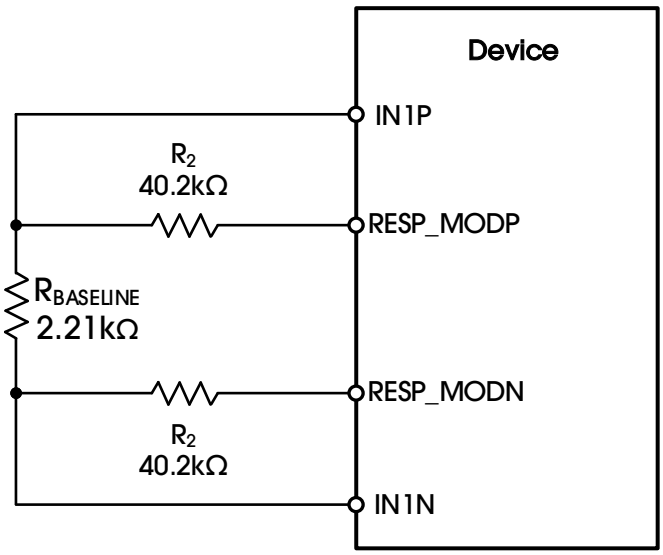


Figure 77. Respiration-Noise Test Circuit

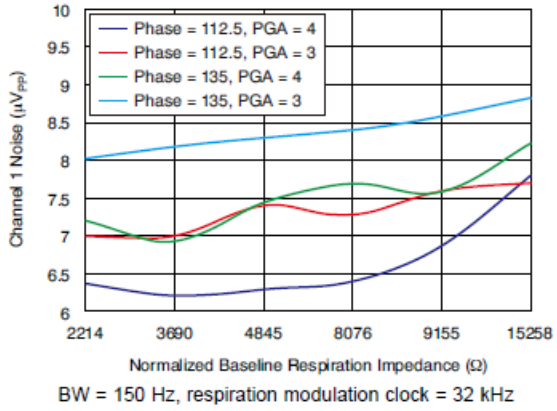


Figure 78. Channel-1 Noise vs. Impedance for 32kHz Modulation Clock and Phase

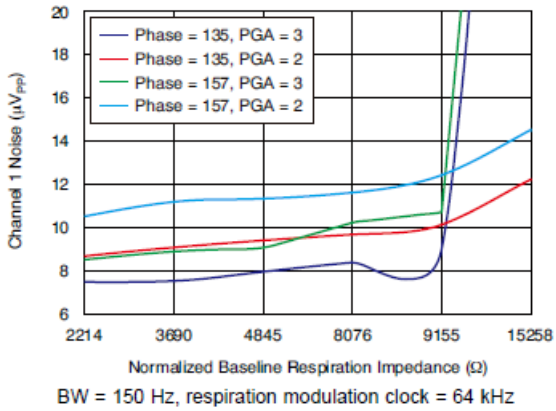


Figure 79. Channel-1 Noise vs. Impedance for 64kHz Modulation Clock and Phase

$$R_{NORMALIZED} = \frac{R_{ACTUAL} \times I_{ACTUAL}}{29\mu A} \quad (11)$$

其中：

- R_{ACTUAL} 是基线身体阻抗。
- I_{ACTUAL} 调制电流，计算公式为(VREFP – VREFN) 除以调制电路的阻抗。

例如，假设：

- 调制频率 = 32kHz
- R_{ACTUAL} = 3kΩ
- I_{ACTUAL} = 50µA
- $R_{NORMALIZED}$ = (3kΩ × 50µA) / 29µA = 5.1kΩ

参考 Figure 78 和 Figure 79，增益 = 4 且相位 =112.5°可在 6.4μV_{PP} 下产生最佳性能。使用高阶 2Hz 截止值对该信号进行低通滤波，将噪声降低至 600nV_{PP} 以下。阻抗分辨率为 600nV_{PP} / 29µA = 20mΩ。当调制频率为 32kHz 时，使用增益 3 和 4，以及相位 112.5°和 135°以获得最佳性能。当调制频率为 64kHz 时，使用 2 和 3 的增益以及 135°和 157°的相位以获得最佳性能。

10.2.1.3 应用曲线

Figure 80 显示使用 Fluke medSim 300b 通过 AFE95x ECG FE-PDK 获取的呼吸数据。然后对数据进行低通滤 a 波，以衰减感兴趣频带之外的噪声。使用 32kHz 的调制频率、3 的 PGA 增益和 112.5°的 RESP_PH 设置。

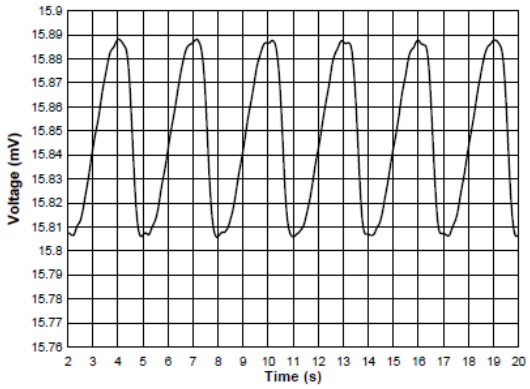


Figure 80. Respiration Impedance Taken with AFE95x

10.2.2 使用 AFE95x 上的 PACEOUT 引脚进行基于软件的人工起搏器检测

由人工起搏器产生的电脉冲用于调节心脏的跳动，并且在其他生物电势信号量表上测量时具有非常小的持续时间(宽度)。根据 AAMI EC11 中列出的标准，医疗仪器必须能够捕获持续时间窄至 0.5ms 的起搏器脉冲。AFE95x 能够以 64kSPS 的速率捕获数据；理想情况下，该速率足以捕获最窄的脉冲。不过，AFE95x 上的数据速率设置是所有通道的全局设置。使用 AFE95x 以足够快的速度对输入通道进行数字化，以便进行稳定可靠的起搏器检测，这意味着所有通道必须尽快转换；可能不合需要的条件。

替代拓扑是使用 AFE95x 内部起搏信号缓冲器将任何特定通道输入的单端版本向外路由到快速采样 SAR ADC，以单独对检测通道信号进行数字化。然后在数字域中执行起搏器脉冲检测。有关该架构的基本方框图，请参阅 Figure 81。示例采用了 OPA 和 SAR ADC 的组合。OPA 用于驱动 SAR ADC 的输入采样结构，但提供了必然的灵活性，可在起搏信号输出数字化之前添加另一个增益级和有源抗混叠滤波。

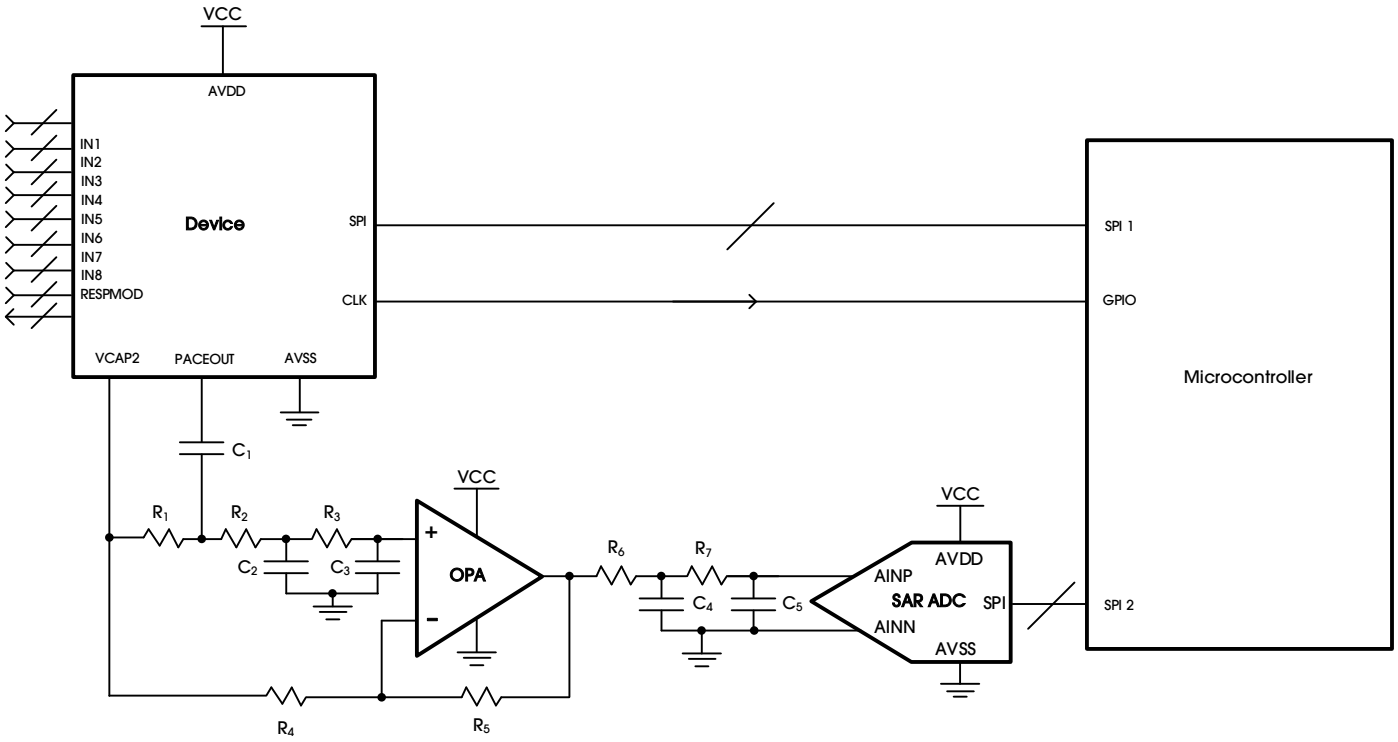


Figure 81. Block Diagram of the Software Pacemaker Detection Topology

10.2.2.1 设计要求

Table 77 显示了 Figure 81 中所示组件的设计要求。

Table 77. Software Pace Design Requirements

DESIGN PARAMETER	VALUE
Analog Supply Voltage	3.3V
Minimum Pacemaker Signal Bandwidth	0.5ms
Minimum Pacemaker Signal Amplitude	2mV
Feedback Network R_4 + R_5 (Nonunity Gain)	≈ 100kΩ

10.2.2.2 详细设计程序

AFE95x 上的起搏信号放大器提供差分到单端的转换，任何电压的 0.4V/V 振幅会显示在用于路由起搏信号放大器的通道 PGA 的输出端。选择将哪些通道连接到起搏信号放大器是在 AFE95x 的起搏信号检测寄存器中执行的。显示在起搏信号放大器输出端的电压将相对于模拟中间电源得出。

在 AFE95x 转换信号之前，信号必须由高速运算放大器进行缓冲，因为 AFE95x 的输入代表开关电容器类型的负载。由于低输入偏置电流和 20MHz 单位增益带宽，OPA 非常适用于执行该功能。运算放大器还可以灵活地在 SAR ADC 之前提供额外的增益级，隔离滤波器级或提供简单的缓冲。C_1 和 R_1 的作用是提供与起搏器检测信号的交流耦合。这种耦合可能是必要的，因为电极偏移和起搏器脉冲在某些情况下都可能高达几百毫伏。

需要使用主动驱动的信号接地将运算放大器的直流偏置设置在中间电源。可以使用在 AFE95x 上的 VCAP2 上提供的电压作为经缓冲的中间电源电压。VCAP2 引脚上的电压可能有噪声，但使用它来驱动运算放大器的反相和同相输入的共模电压会导致运算放大器显著地消除该噪声，因为它是两个输入所共用的。

运算放大器反馈电阻器 R_4 和 R_5 设置 OPA 的增益。该配置的传递函数 Equation 12 中所示的同相运算放大器配置的传递函数。

$$V_o = V_i \left(1 + \frac{R_3}{R_2}\right) \tag{12}$$

选择了电阻器 R_4 和 R_5 来设置所需的增益。串联组合约为 100kΩ，因此反馈电流均限制在 AFE95x VCAP2 内部稳压器驱动强度范围内，并且电阻器的约翰逊-奈奎斯特噪声仍然可以忽略不计。

如果 OPA320 仅用作缓冲器，则移除 R_4 以提供单位增益。如果不需要交流耦合，为了获得最佳性能，应使用 0Ω 电阻器代替 C_1 并取消装配 R_1。

包含 R_2、C_2、R_3、C_3、R_6、C_4、R_7 和 C_5 的 RC 网络形成了 SAR ADC 的隔离式双极 RC 抗混叠滤波器。该滤波器的元件值设置为在 ADC 采样频率下提供显著的衰减，但仍提供足够的带宽来检测起搏器脉冲。大于 2kHz 的带宽足以捕获 0.5ms 的窄起搏器脉冲。

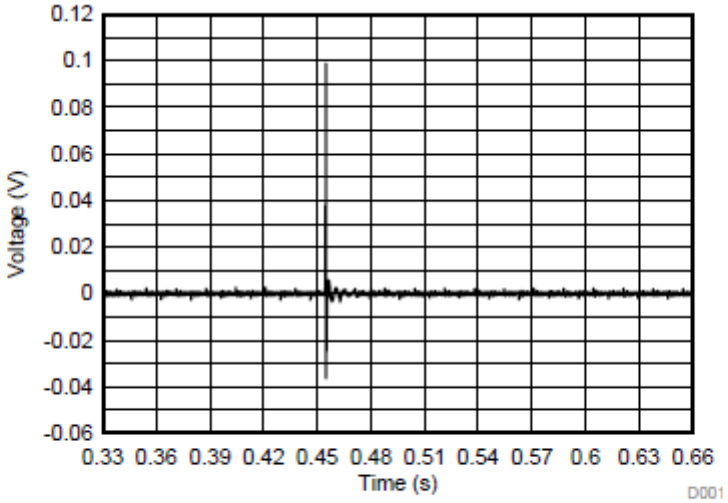
在实时系统中，必须通过每个传入样本为起搏器收集和分析数据。对通过 AFE95x 收集的数据进行数字滤波，以消除带外噪声。与 Δ-Σ 转换器不同，SAR 转换器在将数据发送到主机之前不会对数据应用过滤器。有许多因素推动了数字滤波器实施决策。其中一些因素包括响应的陡度、相位线性度和抽头数量。将此采用 AFE95x 器件的拓扑与呼吸测量电路同时使用时，请特别注意消除呼吸调制电路产生的噪声。

检测起搏器脉冲的关键是检测输入电压的急剧转变。要测量输入电压转换的幅度，请应用数字微分器算法。该算法测量跨几个样本的电压幅度变化，并将该变化与触发检测所需的阈值进行比较。以下伪代码举例说明了使用该拓扑时所需的一些处理步骤：

```
newDataPoint = collectFromAFE95x ( );  // Collect data from the AFE95x
// Apply combined low-pass filter and differentiator
inputRateOfChange = LPFandDifferentiator( newDataPoint );
if( abs( inputRateOfChange ) > thresholdValue ) // Check if a quick edge occurred
{
pacemakerFlag = true;                          // Edge detected
}
```

10.2.2.3 应用曲线

Figure 82 显示了通过 AFE95x 的 PACEOUT 引脚(使用 OPA 和 AFE95x)进行收集，然后进行滤波的数据。可以清楚地识别起搏器脉冲。



NOTE: For illustration purposes, plot data were not processed in real time. As a result of the lack of shielding in this particular configuration, data were also high-pass filtered to attenuate the utility noise.

Figure 82. Filtered AFE95x Output Data with Pacemaker Pulse

11. 电源供电建议

AFE95x 具有三个电源：AVDD、AVDD1 和 DVDD。为了获得最佳性能，AVDD 和 AVDD1 的噪声必须尽可能低。AVDD1 为电荷泵模块提供电源，并具有频率为 f_{CLK} 的瞬变。因此，应以星型方式将 AVDD1 和 AVSS1 连接到 AVDD 和 AVSS。消除来自 AVDD 和 AVDD1 (与 AFE95x 的运行不同步)的噪声非常重要。使用 1μF 和 0.1μF 固态陶瓷电容器绕过每个 AFE95x 电源。为了获得最佳性能，请将数字电路(DSP、微控制器、FPGA 等)放置到系统中，以使这些器件上的返回电流不会穿过 AFE95x 的模拟返回路径。使用单极或双极电源为 AFE95x 供电。

使用表面贴装、低成本、薄型、多层陶瓷型电容器进行去耦。在大多数情况下，VCAP1 电容器也是多层陶瓷；但是，在电路板受到高频或低频振动的系统中，应安装非铁电电容器，如钽电容器或 1 类电容器(C0G 或 NPO)。EIA2 类和 3 类电介质(如 X7R、X5R、X8R 等)是铁电型的。这些电容器的压电特性可以表现为来自电容器的电噪声。使用内部基准时，VCAP1 节点上的噪声会导致性能下降。

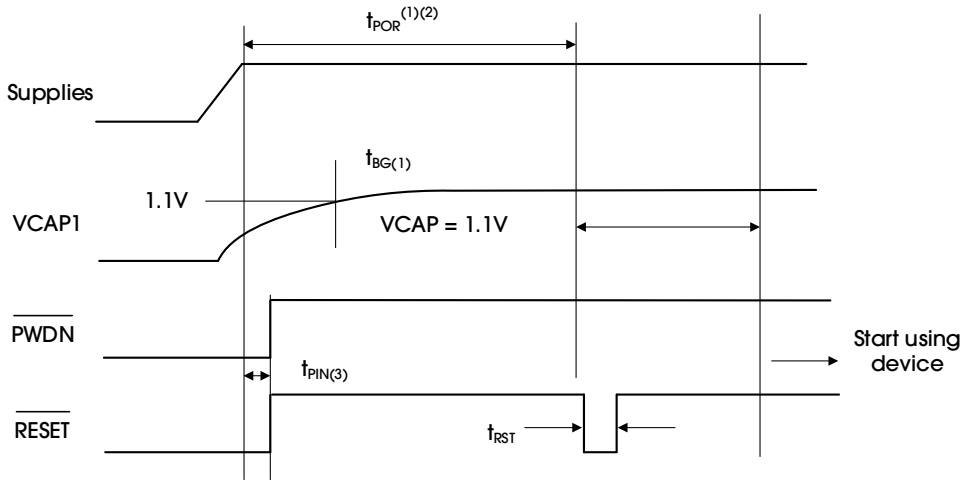
11.1 上电测序

在器件上电之前，所有数字和模拟输入必须处于低电平。上电时，将所有这些信号保持在低电平，直到电源稳定为止，如 Figure 83 所示。

留出时间让电源电压达到其最终值，然后开始向 CLK 引脚提供主时钟信号。等待时间 t_{POR}，然后使用$\overline{RESET}$引脚或复位指令发送复位脉冲，以初始化芯片的数字部分。在 t_{POR} 之后或 VCAP1 电压大于 1.1V 之后(以较长的时间为准)发出复位命令。注意：

- Table 78 中介绍了 t_{POR}。
- VCAP1 引脚充电时间由 RC 时间常数设置；请参阅 Figure 27。

释放$\overline{RESET}$引脚后，对配置寄存器进行编程；有关详细信息，请参阅 CONFIG1: CONFIGURATION REGISTER 1 (ADDRESS = 01H) (RESET = 06H)部分。Table77 中显示了上电序列时序。



(1) Timing to reset pulse is t_{POR} or after t_{BG}, whichever is longer.
(2) When using an external clock, t_{POR} timing does not start until CLK is valid.
(3) Timing to release PWDN and RESET is t_{PIN} after both AVDD and DVDD supplies are ready.

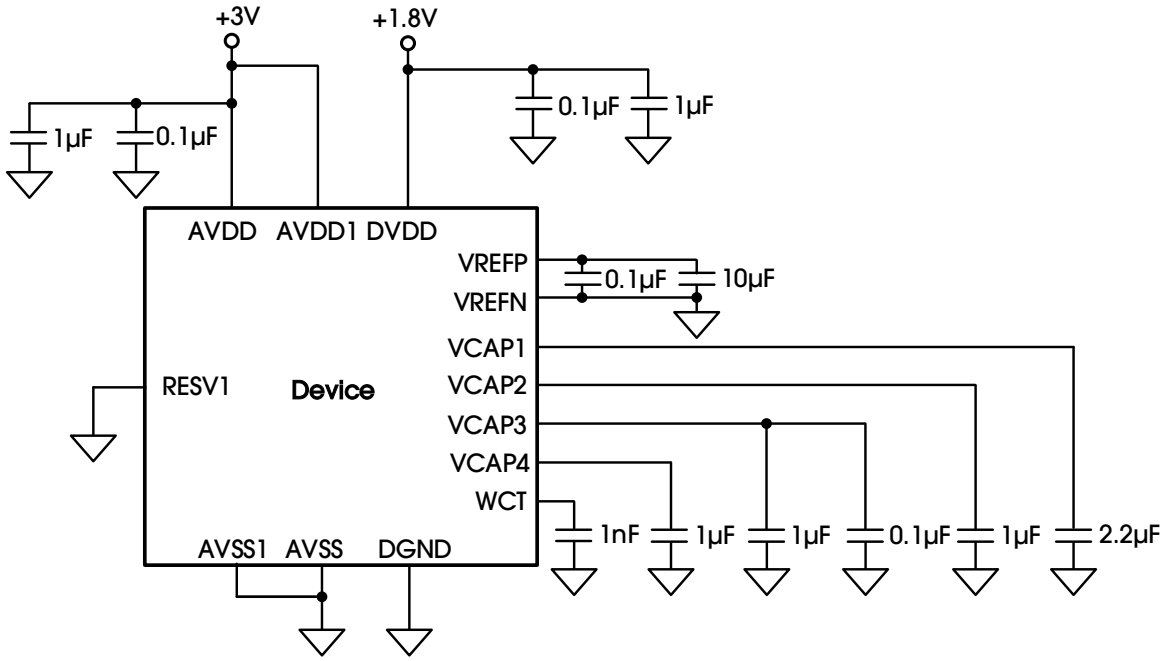
Figure 83. Power-Up Timing Diagram

Table 78. Timing Requirements for Figure 83

PARAMETER	SYMBOL	MIN	MAX	UNITS
Wait after Power-up until Reset	t_{POR}	2^{18}		t_{CLK}
Reset Low Duration	t_{RST}	2		t_{CLK}
Power Down and Reset Pin Release	t_{PIN}	0		t_{CLK}

11.1.1 连接到单极(3V 或 1.8V)电源

Figure 84 说明了连接到单极电源的 AFE95x。在该示例中，模拟电源(AVDD)以模拟接地(AVSS)为基准，数字电源(DVDD)以数字接地(DGND)为基准。

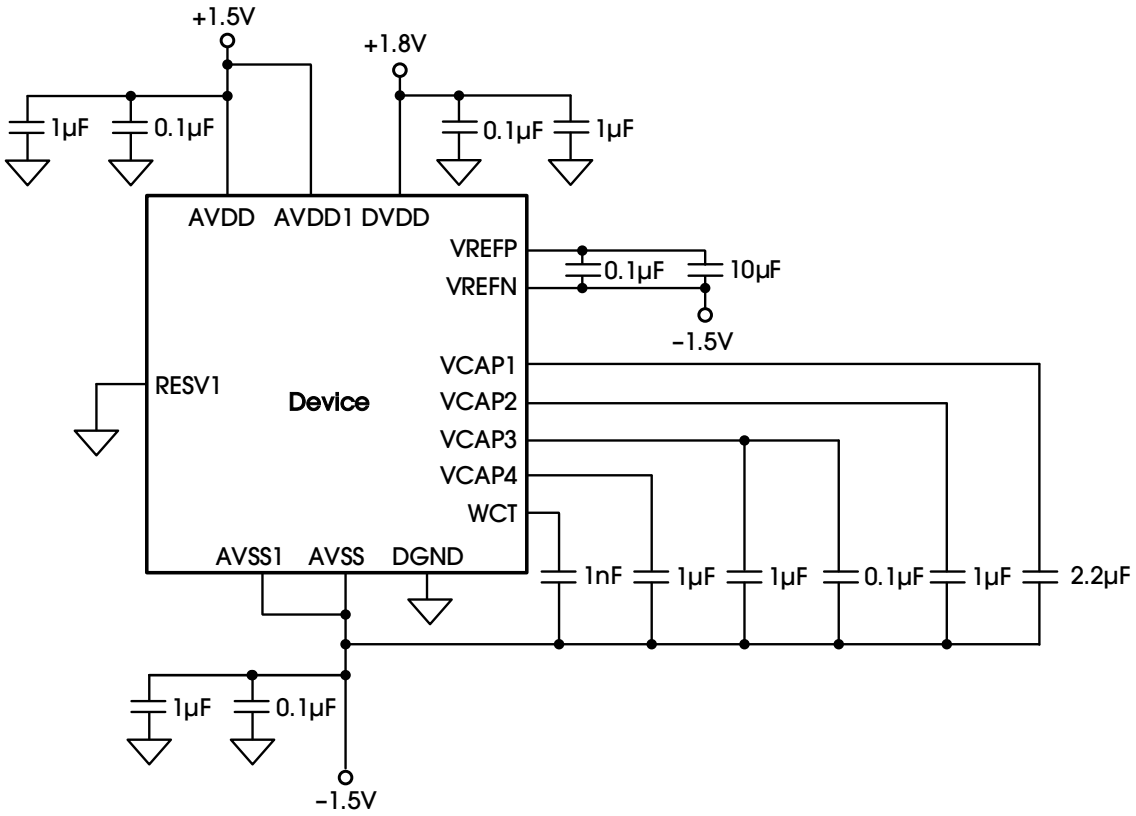


NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 84. Single-Supply Operation

11.1.2 连接到双极(±1.5V 或±1.8V)电源

Figure 85 说明了连接到双极电源的 AFE95x。在该示例中，模拟电源连接到器件模拟电源(AVDD)。该电源以器件模拟回路(AVSS)为基准，数字电源(DVDD)以器件数字接地回路(DGND)为基准。



NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 85. Bipolar Supply Operation

12. 布局

12.1 布局指南

针对接地使用低阻抗连接，以便返回电流不受干扰地流回到各自的源。为了获得最佳性能，请将一个完整的 PCB 层专用于接地平面，在该层上不布任何其他信号迹线。保持与接地平面的连接尽可能短且直。使用通孔连接到接地层时，请使用多个平行的通孔，以减少接地阻抗。

混合信号布局有时包含在一个位置连接在一起的独立模拟和数字接地平面；但是，当正确放置模拟、数字和电源组件后，不需要分离接地平面。正确放置元件可将模拟、数字和电源电路划分为不同的 PCB 区域，以防止数字返回电流耦合到敏感的模拟电路中。如果需要进行接地平面分离，则在 ADC 处进行连接。在多个位置连接各个接地层会产生接地环路，因此不建议这样做。模拟和数字的单个接地平面可避免接地环路。

使用低 ESR 陶瓷电容器旁路电源引脚。必须使用短且直的迹线将旁路电容器尽可能靠近电源引脚放置。为获得最佳性能，旁路电容器的接地侧连接也必须是低阻抗连接。电源电流首先流过旁路电容器引脚，然后流到电源引脚，使旁路最有效(也称为开尔文连接)。如果多个 ADC 位于同一 PCB 上，请使用宽电源迹线或专用的电源平面，以最大限度地降低 ADC 之间发生串扰的可能性。

如果将外部滤波用于模拟输入，请尽可能使用 C0G 型陶瓷电容器。C0G 电容器具有稳定的特性和低噪声特性。理想情况下，将差分信号组成多个对，以最大程度地减小迹线之间的环路面积。布线数字电路(如时钟信号)时使其远离所有模拟引脚。请注意，内部基准输出回路与 AVSS 电源共用相同的引脚。为了最大限度地减少电源迹线和基准回路迹线之间的耦合，请分别布置两条迹线；理想情况下，在 AVSS 引脚处采用星型连接。

必须在模拟输入线上进行短且直的互连，并避免杂散布线电容，尤其是在模拟输入引脚和 AVSS 之间。这些模拟输入引脚具有高阻抗，对外部噪声非常敏感。将 AVSS 引脚视为敏感的模拟信号，并通过适当的屏蔽直接连接到电源接地。如果未实现屏蔽，PCB 迹线之间的泄漏电流可能会超过 AFE95x 的输入偏置电流。尽可能使数字信号远离 PCB 上的模拟输入信号。

串行接口的 SCLK 输入应该没有噪声和干扰，这一点很重要。即使采用相对慢的 SCLK 频率，短数字信号上升和下降时间也可能导致过度振铃和噪声。为了获得最佳性能，请根据需要使用终端电阻器来保持数字信号迹线短路，并确保所有数字信号都直接在接地平面上方路由，而使用最少的通孔。

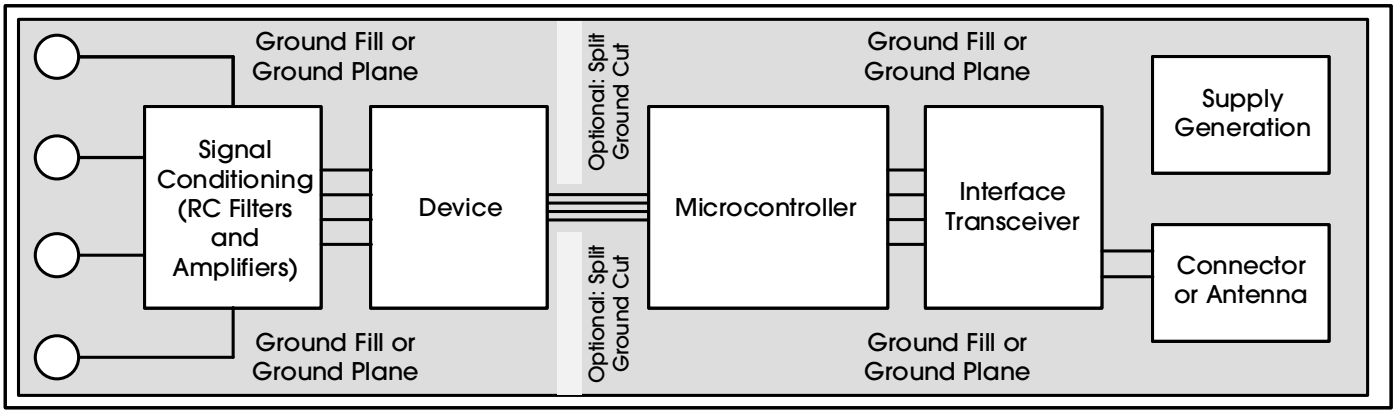


Figure 86. System Component Placement

12.2 布局示例

请参考 EVM 或者咨询公司销售支持。

13. PACKAGE INFORMATION

The AFE95x is available in the BGA-64 package. Figure 87 shows the package view.

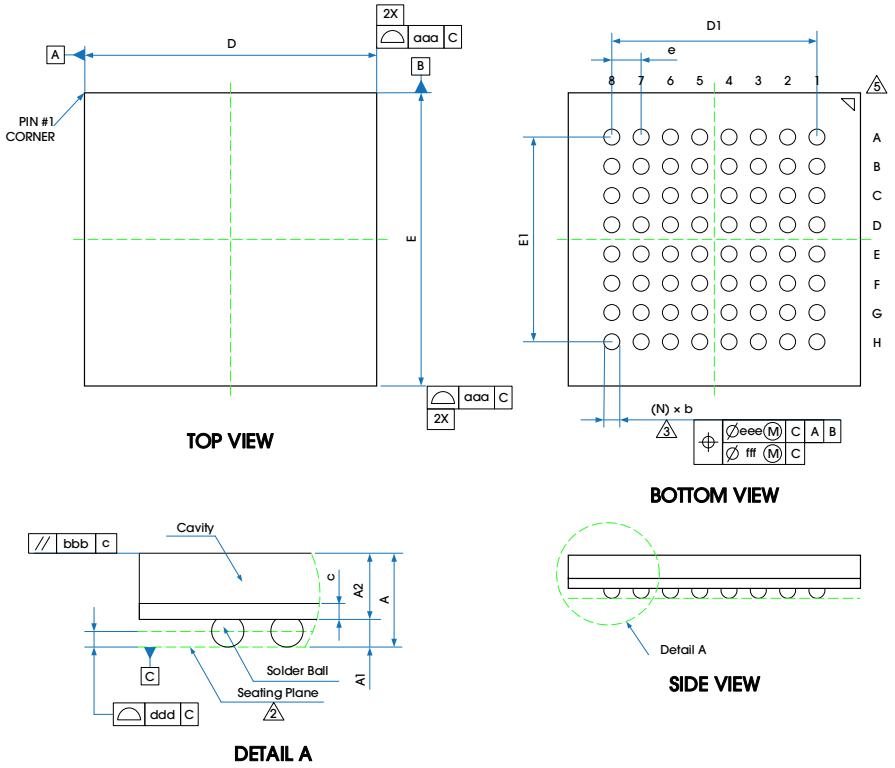


Figure 87. Package View

Table 79 provides detailed information about the dimensions.

Table 79. Dimensions

SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.360	—	—	0.054
A1	0.300	0.350	0.400	0.012	0.014	0.016
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.180	0.210	0.240	0.007	0.008	0.009
D	7.900	8.000	8.100	0.311	0.315	0.319
E	7.900	8.000	8.100	0.311	0.315	0.319
D1	—	5.600	—	—	0.220	—
E1	—	5.600	—	—	0.220	—
e	—	0.800	—	—	0.031	—
b	0.400	0.450	0.500	0.016	0.018	0.020
aaa		0.150			0.006	
bbb		0.200			0.008	
ddd		0.200			0.008	
eee		0.150			0.006	
fff		0.080			0.003	
Bail Diam		0.450			0.018	
N		64			64	
MD/ME		8/8			8/8	

14. TAPE AND REEL INFORMATION

Figure 88 illustrates the carrier tape.

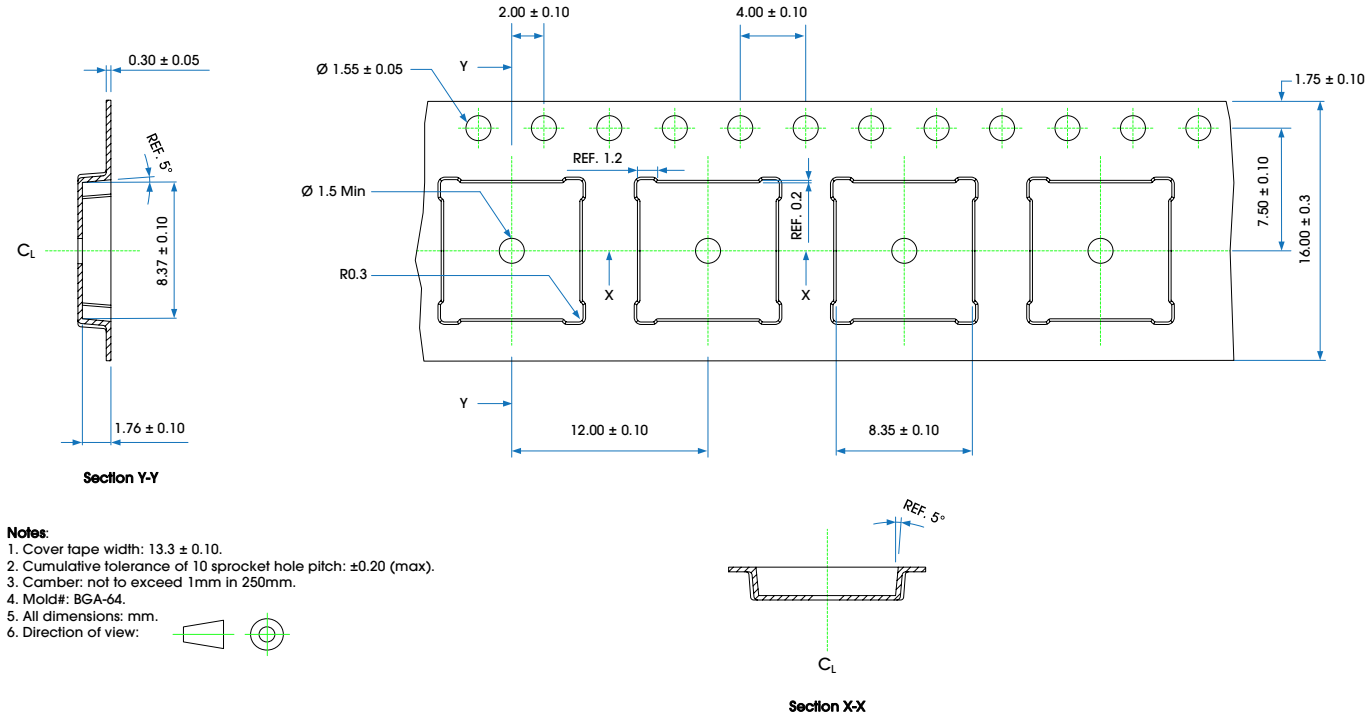


Figure 88. Carrier Tape Drawing

Table 80 provides information about tape and reel.

Table 80. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
BGA-64	13”	1000	1	8	8000	358*340*50	430*380*390

Figure 89 shows the product loading orientation— pin 1 is assigned at Q1.

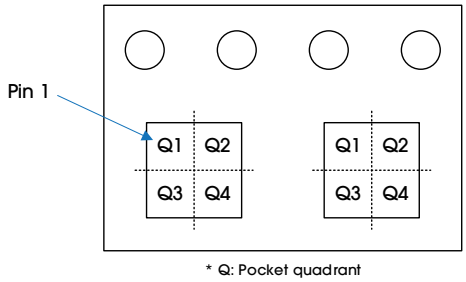


Figure 89. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rel 1.1	20 September 2023	Preliminary release.
Rel 1.2	21 December 2023	Updated the TYPICAL CHARACTERISTICS section.
Rel 1.3	14 November 2024	Updated Page 1, order information, Table 7, Table 8, and Section 7.1.