74AHC1G08; 74AHCT1G08

Single 2-input AND gate

Product datasheet, Rev. 1.0 Aug 8, 2024

1.General Description

The 74AHC1G08 and 74AHCT1G08 are single 2-input AND gates. Inputs are overvoltage tolerant.This feature allows the use of these devices as translators in mixed voltage environments.

2.Features and Benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 200 mA
- Symmetrical output impedance
- Balanced propagation delays
- Input levels:
  - For 74AHC1G08: CMOS level
  - For 74AHCT1G08: TTL level
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 7000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74AHC1G08GV	SOT23-5L	SOT23 package, 5 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
74AHCT1G08GV			
74AHC1G08GW	SOT353	SOT353 package, 5 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
74AHCT1G08GW			
74AHC1G08DRL	SOT553	SOT553 package, 5 pins 1.6 mm × 1.2 mm; 0.6 mm (Max) height	3000
74AHCT1G08DRL			

4. Function Diagram

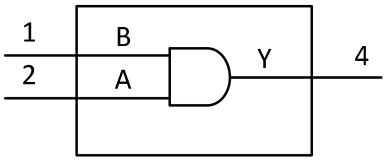


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

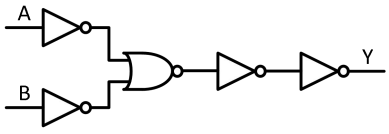


Fig. 3. Logic diagram

5. Pinning Information

5.1. Pinning

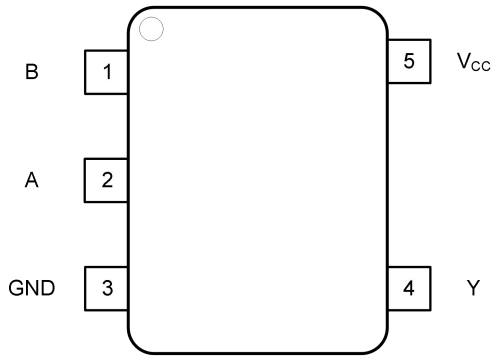


Fig. 4. Top view pin configuration SOT23-5L, SOT353 and SOT553

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
B	1	Data input
A	2	Data input
GND	3	Ground (0V)
Y	4	Data output
V_{CC}	5	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
V_I	input voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-20		mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]		±20	mA
I_O	output current	$-0.5\ V < V_O < V_{CC} + 0.5\ V$		±25	mA
I_{CC}	supply current			75	mA
I_{GND}	ground current		-75		mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. MDD does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	74AHC1G08			74AHCT1G08			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	2.0	5.0	5.5	V
V_I	input voltage		0		5.5	0		5.5	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	25	125	-40	25	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V			100			100	ns/V
		V_{CC} = 5.0 V ± 0.5 V			20			20	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74AHC1G08								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5			1.5		V
		V_{CC} = 3.0 V	2.1			2.1		V
		V_{CC} = 5.5 V	3.85			3.85		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.5		0.5	V
		V_{CC} = 3.0 V			0.9		0.9	V
		V_{CC} = 5.5 V			1.65		1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0		1.9		V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0		2.9		V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5		4.4		V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.48	2.93		2.40		V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.80	4.39		3.70		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 50 µA; V_{CC} = 2.0 V		0	0.1		0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V		0	0.1		0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V		0	0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		0.05	0.44		0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V		0.07	0.44		0.55	V
I_I	input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V		±0.01	±1.0		±2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V		0.01	10		40	µA
C_I	input capacitance			3.5				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74AHCT1G08								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.0			1.0		V
		V_{CC} = 3.3 V	1.5			1.5		V
		V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V			0.3		0.3	V
		V_{CC} = 3.3 V			0.55		0.55	V
		V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or $V_{IL;}$						
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0		1.9		V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0		2.9		V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5		4.4		V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.48	2.93		2.4		V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.80	4.39		3.70		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL};						
		I_O = 50 µA; V_{CC} = 2.0 V		0	0.1		0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V		0	0.1		0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V		0	0.1		0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		0.05	0.44		0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V		0.07	0.44		0.55	V
I_I	input leakage current	V_I = 5.5 V or GND ; V_{CC} = 0 V to 5.5 V		±0.01	±1.0		±2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V		0.01	10		40	µA
ΔI_{CC}	additional supply current	per input pin ; V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V		0.23	1.35		1.35	mA
C_I	input capacitance			3.5				pF

[1]All typical values are measured at T_{amb} = 25°C.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74AHC1G08								
t_{pd}	propagation delay	A and B to Y; see Fig. 5 [2]						
		V_{CC} = 3.0 V to 3.6 V, C_L = 15 pF	1.0	4.3	9.5	1.0	10.0	ns
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0	3.1	6.5	1.0	7.0	ns
C_{PD}	power dissipation capacitance	C_L = 15 pF ; f = 1MHz ; V_I = GND to V_{CC} ; [3]		26				pF
74AHCT1G08								
t_{pd}	propagation delay	A and B to Y; see Fig. 5 [2]						
		V_{CC} = 2.0 V, C_L = 15 pF		46.5				
		V_{CC} = 3.3 V, C_L = 15 pF	3.0	9.3	12.5	3.0	13.0	
		V_{CC} = 4.5 V to 5.5 V, C_L = 15 pF	1.0	4.3	8.0	1.0	8.5	ns
C_{PD}	power dissipation capacitance	C_L = 15 pF ; f = 1MHz ; V_I = GND to V_{CC} ; [3]		22				pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} =2.0 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

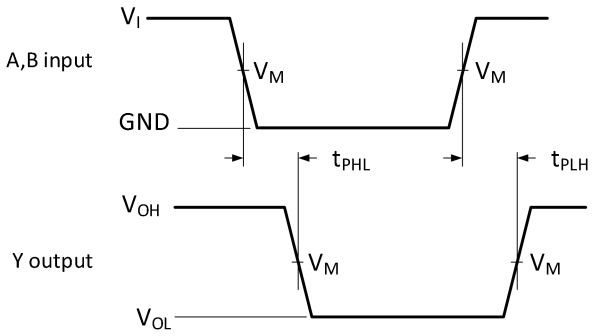
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

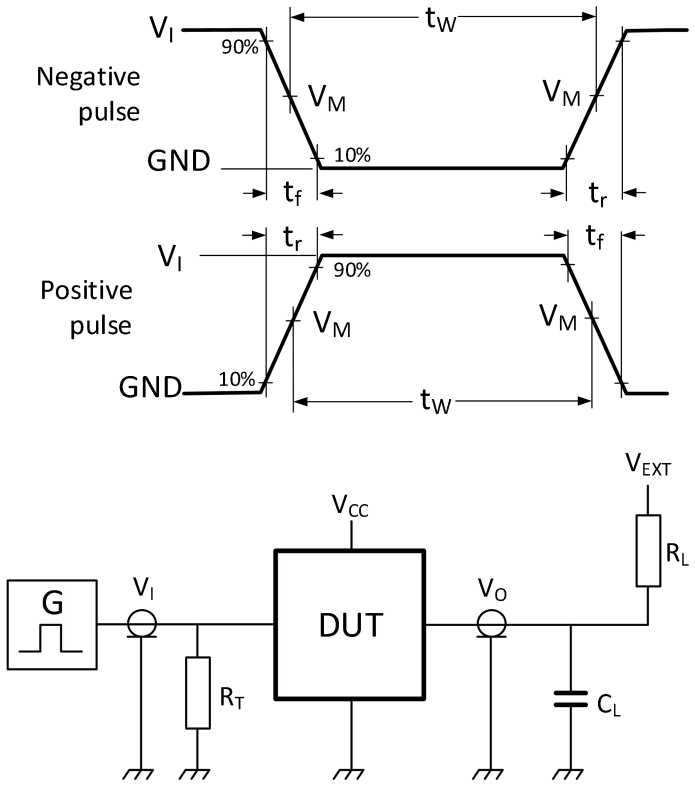


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input A, B to output Y propagation delays

Table 8. Measurement points

Type	Supply Voltage	Input		Output
	V_{CC}	V_I	V_M	V_M
74AHC1G08	3.0 V ~ 5.5 V	GND to V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
74AHCT1G08	2.0 V	GND to V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}
	3.3 V	GND to 3.0 V	1.5 V	0.5 x V_{CC}
	4.5 V ~ 5.5 V	GND to 3.0 V	1.5 V	0.5 x V_{CC}



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

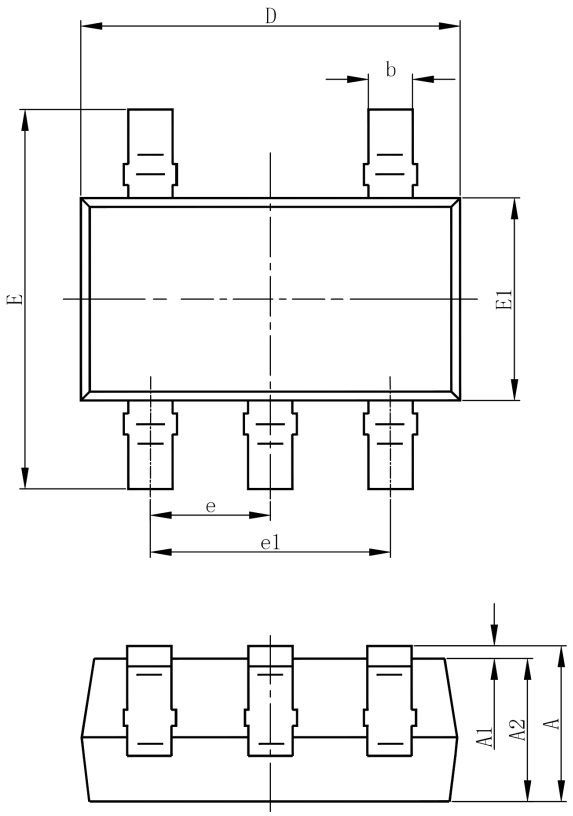
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	**Input**	**Load**	**V_{EXT}**
	$t_r = t_f$	**C_L**	**t_{PLH}, t_{PHL}**
74AHC1G08	≤ 2.5 ns	15 pF	open
74AHCT1G08	≤ 2.5 ns	15 pF	open

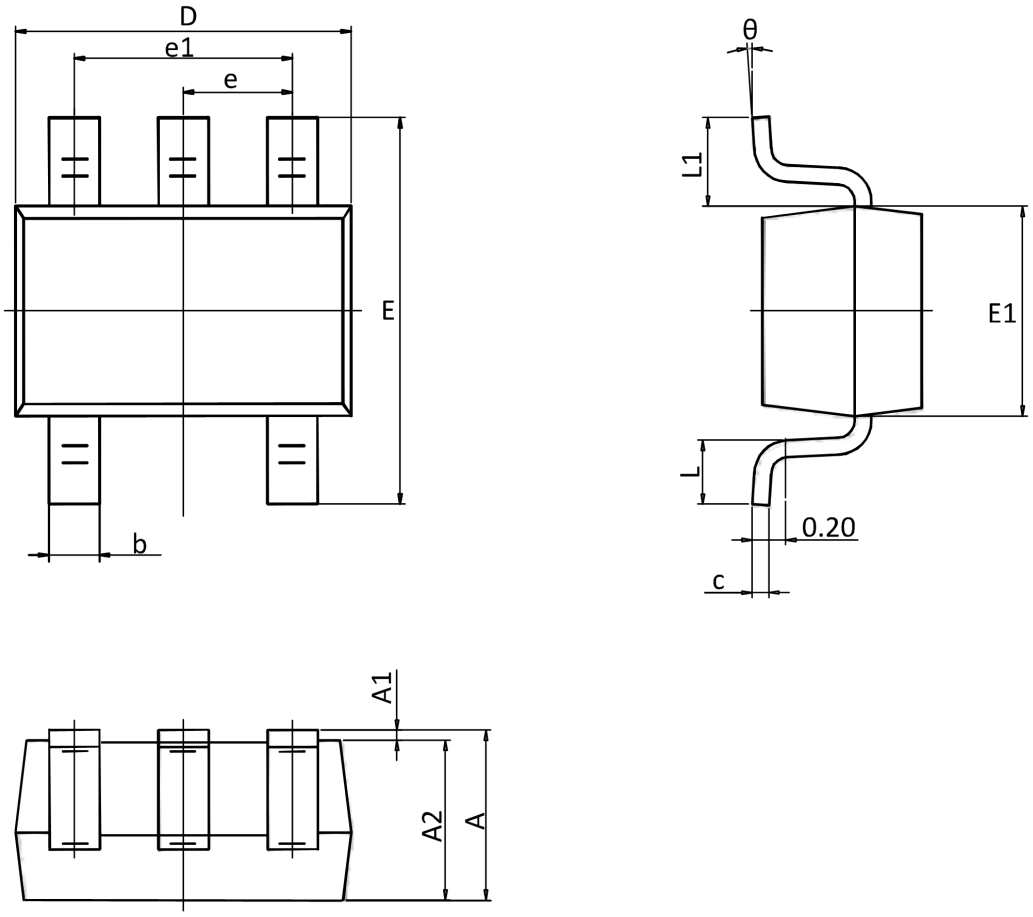
11. Package Outline

SOT23-5L



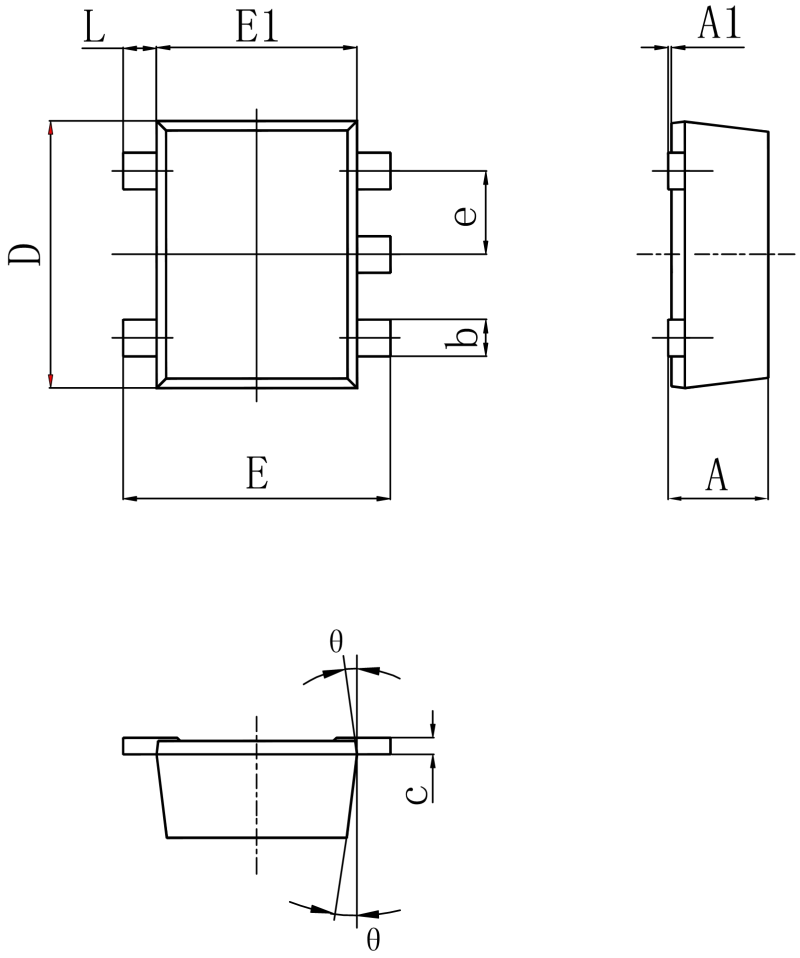
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

SOT353



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 REF.		0.021 REF.	
θ	0°	8°	0°	8°

SOT553



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
e	0.450	0.550	0.018	0.022
c	0.090	0.160	0.004	0.006
D	1.500	1.700	0.059	0.067
b	0.170	0.270	0.007	0.011
E1	1.100	1.300	0.043	0.051
E	1.500	1.700	0.059	0.067
L	0.100	0.300	0.004	0.012
θ	7 °REF.		7 °REF.	

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G08 Rev. 1.0	Mar 08, 2024	Product datasheet		