74HC574; 74HCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Draft datasheet, Rev. 1.0 Aug 08, 2024

1.General Description

The 74HC574 and 74HCT574 are 8-bit D-type transparent latches with 3-state outputs. The device features a clock (CP) and output enable ($\overline{OE}$) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2.Features and Benefits

- Wide operating voltage 2.7 V to 6.0 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 250 mA
- Input levels:
  - For 74HC574: CMOS level
  - For 74HCT574: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.7 V to 6.0 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3500 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74HC574D	SOP-20L	plastic small outline package; 20 leads; body width 7.5 mm	2000
74HCT574D			
74HC574PW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	2000
74HCT574PW			

4.Function Diagram

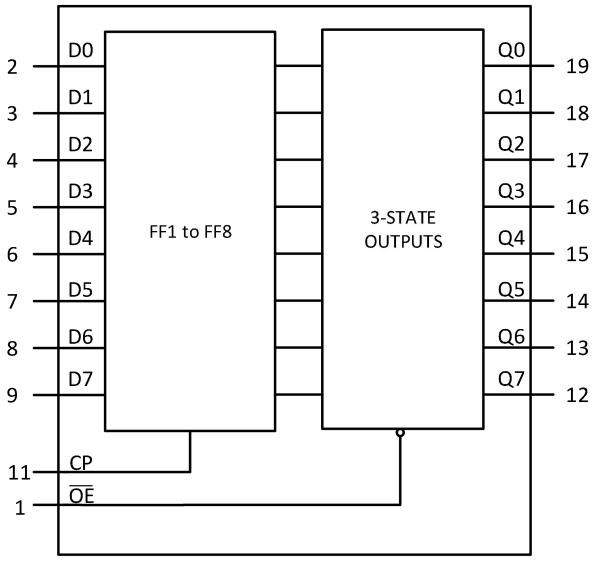


Fig. 1. Functional diagram

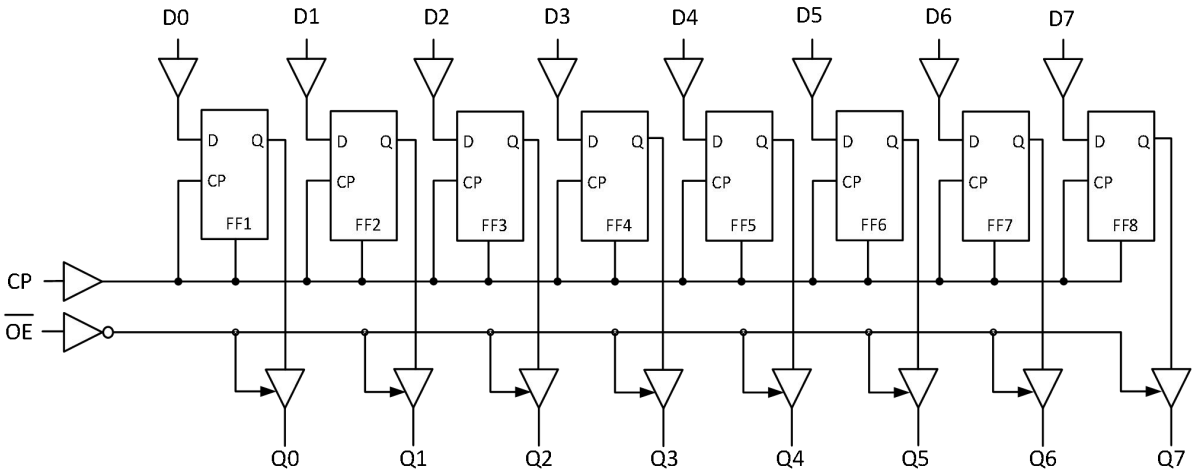


Fig. 2. Logic diagram

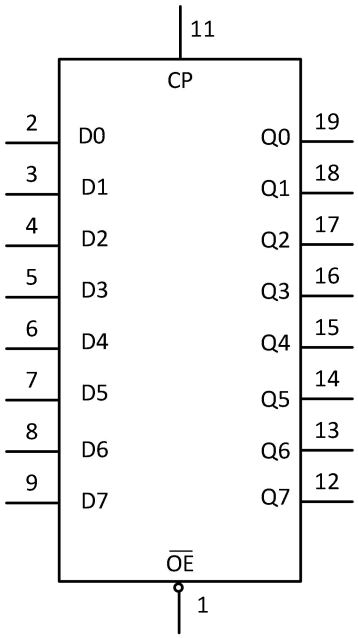


Fig. 3. Logic symbol

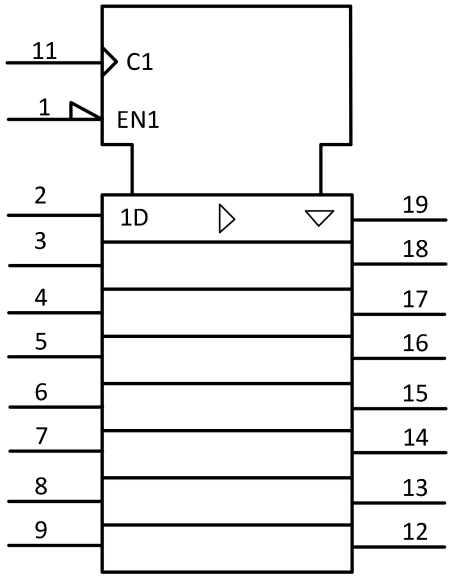


Fig. 4. IEC logic symbol

5.Pinning Information

5.1. Pinning

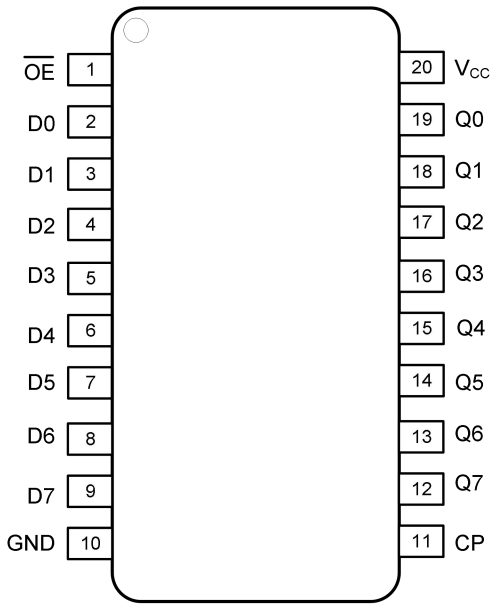


Fig. 5. Top view pin configuration SOP-20L and TSSOP-20L

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	3-state output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19,18,17,16,15,14,13,12	3-state flip-flop outputs
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data inputs
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
V_{CC}	20	supply voltage

6.Functional Description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating modes	Input			Internal flip-flop	Outputs
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable output	H	↑	l	L	Z
	H	↑	h	H	Z

7.Absolute Maximum Ratings

Stresses exceeding the absolut`e maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	output current	$-0.5V < V_O < V_{CC} + 0.5$ V		±35	mA
I_{CC}	supply current			70	mA
I_{GND}	ground current		-70		mA
P_{tot}	total power dissipation	Tamb = -40 °C to + 125 °C		500	mW
T_{stg}	storage temperature		-65	+150	°C

8.Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. MDD does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. Recommended Operating Conditions

Symbol	Parameter	Conditions	74HC574			74HCT574			Unit
			Min	Min	Typ	Min	Min	Typ	
V_{CC}	supply voltage		2.7	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0		V_{CC}	0		V_{CC}	V
V_O	output voltage		0		V_{CC}	0		V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
△t/△V	input transition rise and fall rate	V_{CC} = 2.0 V			625				ns/V
		V_{CC} = 4.5 V		1.67	139		1.67	139	ns/V
		V_{CC} = 6.0 V			83				ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC574								
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V	2.0			2.0		V
		V_{CC} = 4.5 V	3.15			3.15		V
		V_{CC} = 6.0 V	4.2			4.2		V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V			0.6		0.6	V
		V_{CC} = 4.5 V			1.35		1.35	V
		V_{CC} = 6.0 V			1.8		1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20µA; V_{CC} = 3.0 V	2.9			2.9		V
		I_O = -20µA; V_{CC} = 4.5 V	4.4			4.4		V
		I_O = -20µA; V_{CC} = 6.0 V	5.9			5.9		V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.84			3.7		V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.34			5.2		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20µA; V_{CC} = 3.0 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 4.5 V			0.1		0.1	V
		I_O = 20µA; V_{CC} = 6.0 V			0.1		0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V			0.33		0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 6.0 V			±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 6.0V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0A ; V_{CC} = 6.0 V			20		40	µA
C_I	input capacitance			6.5				pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT574								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0			2.0		V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8		0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = -20µA	4.4			4.4		V
		I_O = -6.0 mA	3.84			3.7		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		I_O = 20µA			0.1		0.1	V
		I_O = 6.0 mA			0.33		0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V			±1		±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} ; V_{CC} = 5.5 V ; V_O = V_{CC} or GND			±5		±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V			20		40	µA
ΔI_{CC}	additional supply current	per pin ; V_I = V_{CC} – 2.1 V ; I_O = 0 A ; other inputs at V_{CC} or GND ; V_{CC} = 4.5 V to 5.5 V			450		490	µA
C_I	input capacitance			6.5				pF

[1]All typical values are measured at T_{amb} = 25°C.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

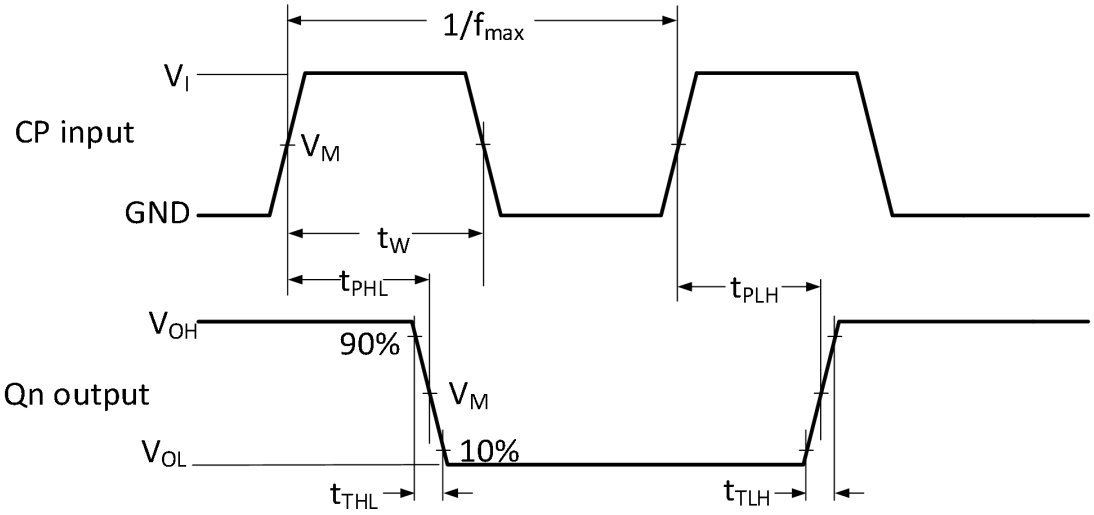
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC574								
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [2]						
		V_{CC} = 3.0 V			30		35	ns
		V_{CC} = 4.5 V			20		25	ns
		V_{CC} = 6.0 V			15		18	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 8 [3]						
		V_{CC} = 3.0 V			22		25	ns
		V_{CC} = 4.5 V			14		17	ns
		V_{CC} = 6.0 V			13		16	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 8 [4]						
		V_{CC} = 3.0 V			22		25	ns
		V_{CC} = 4.5 V			15		18	ns
		V_{CC} = 6.0 V			13		15	ns
t_t	transition time	Qn; see Fig. 6						
		V_{CC} = 3.0 V			8		10	ns
		V_{CC} = 4.5 V			7		9	ns
		V_{CC} = 6.0 V			7		9	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7						
		V_{CC} = 3.0 V	25			30		ns
		V_{CC} = 4.5 V	20			24		ns
		V_{CC} = 6.0 V	17			20		ns
t_{SU}	set up time	Dn to CP; see Fig.7						
		V_{CC} = 3.0 V	16			20		ns
		V_{CC} = 4.5 V	15			18		ns
		V_{CC} = 6.0 V	13			15		ns
t_h	hold time	Dn to CP; see Fig.7						
		V_{CC} = 3.0 V	5			5		ns
		V_{CC} = 4.5 V	5			5		ns
		V_{CC} = 6.0 V	5			5		ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max			
f_{max}	maximum frequency	CP; see Fig. 6						
		V_{CC} = 3.0 V	20			16		MHz
		V_{CC} = 4.5 V	24			20		MHz
		V_{CC} = 6.0 V	28			24		MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}; [6]		30				pF
74HCT574								
t_{pd}	propagation delay	CP to Qn; see Fig. 6 [2]						
		V_{CC} = 4.5 V			25		30	ns
t_t	transition time	Qn; see Fig. 6 [5]						
		V_{CC} = 4.5 V			7		9	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Fig. 8 [3]						
		V_{CC} = 4.5 V			20		25	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Fig. 8 [4]						
		V_{CC} = 4.5 V			20		25	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7						
		V_{CC} = 4.5 V	20			24		ns
t_{SU}	set up time	Dn to CP; see Fig.7						
		V_{CC} = 4.5 V	15			18		ns
t_h	hold time	Dn to CP; see Fig.7						
		V_{CC} = 4.5 V	5			5		ns
f_{max}	maximum frequency	CP; see Fig.6						
		V_{CC} = 4.5 V	24			20		ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} – 1.5 V ; [6]		30				pF

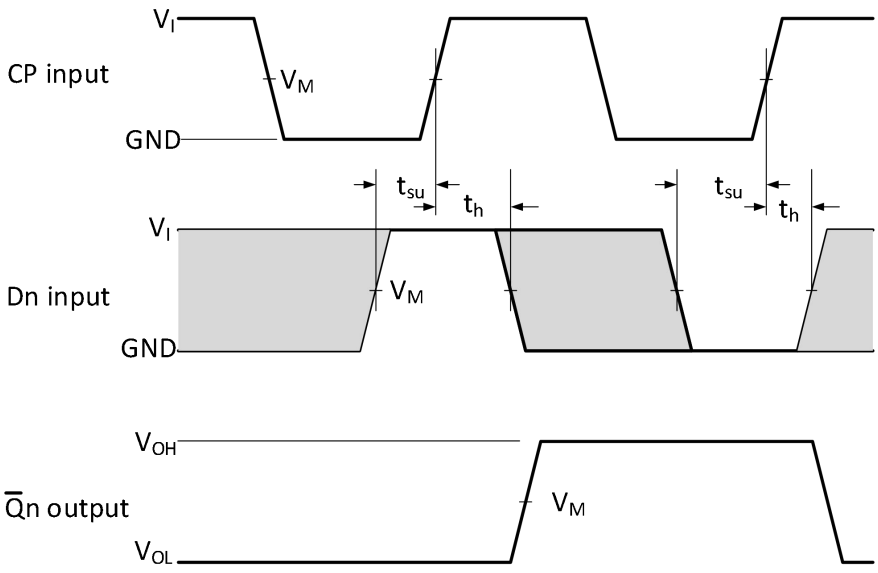
[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] t_t is the same as t_{THL} and t_{TLH}.
[6] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



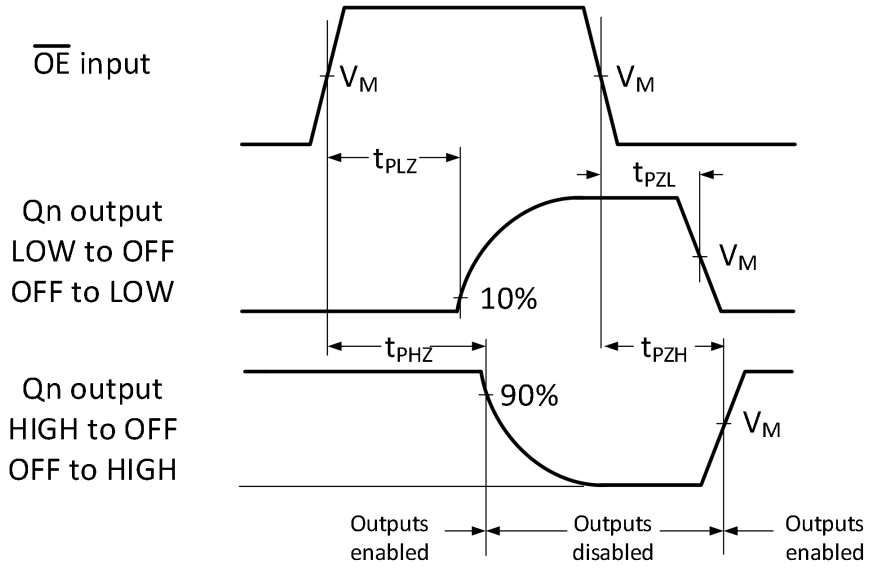
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

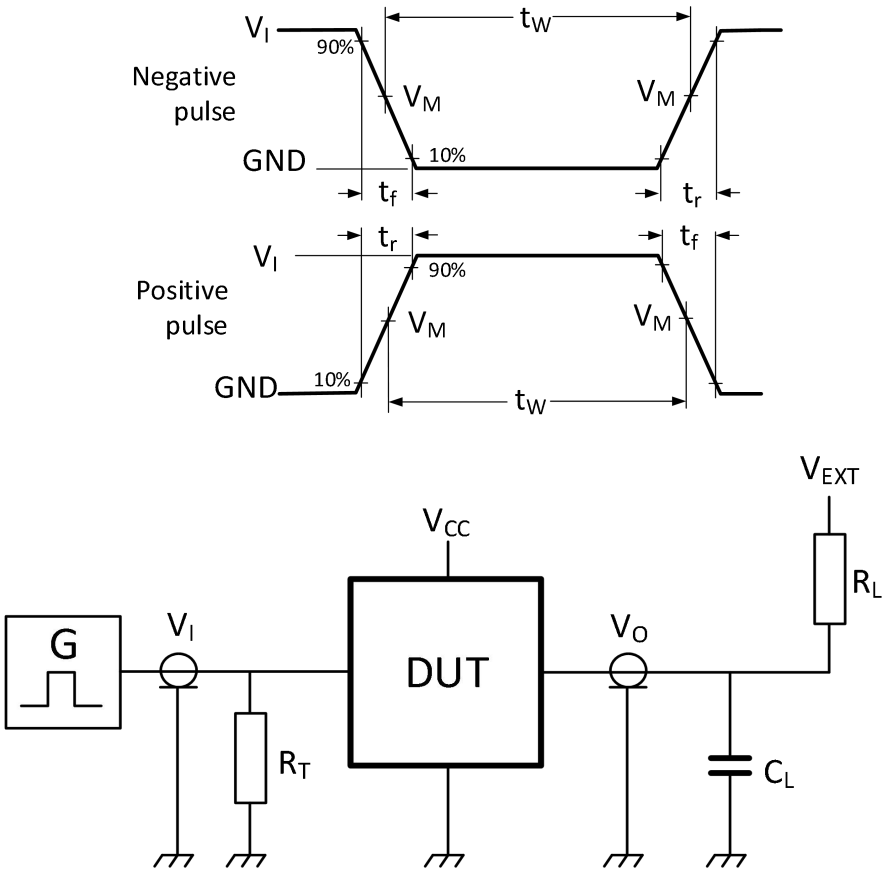


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC574	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT574	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

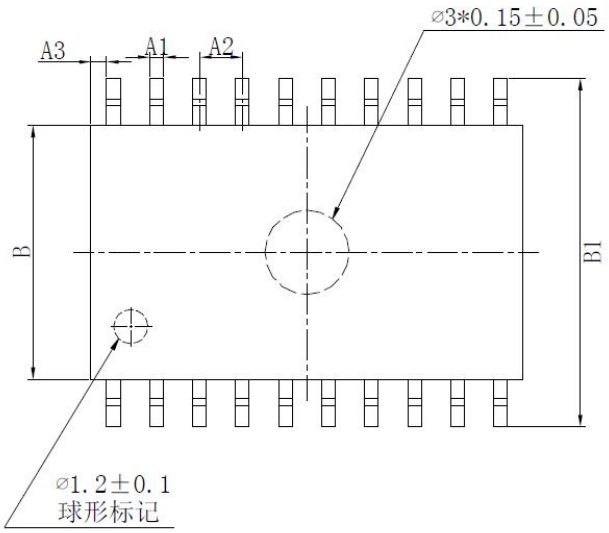
Fig. 9. Test circuit for measuring switching times

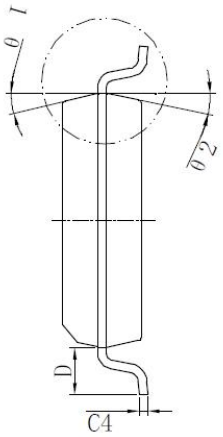
Table 9. Test data

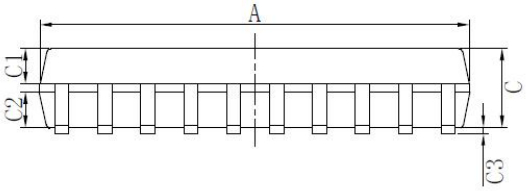
Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}
74HC574	V_{CC}	2.5 ns	50 pF	500Ω	V_{CC}	Open	GND
74HCT574	3 V	2.5 ns	50 pF	500Ω	V_{CC}	Open	GND

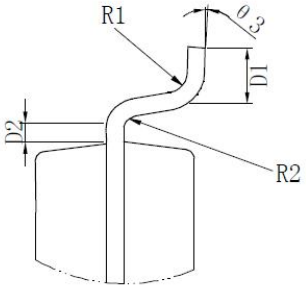
11. Package Outline

SOP-20L



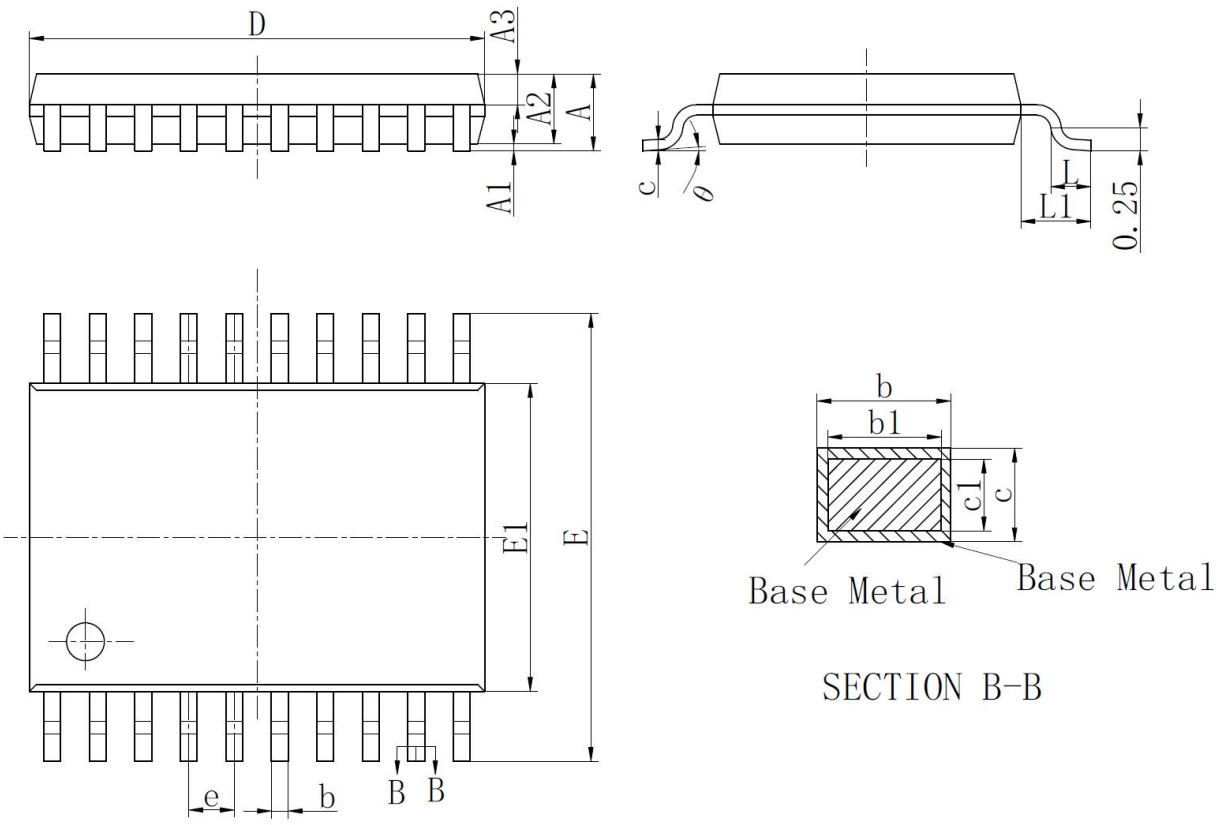






Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	12.600	12.900	C4	0.246	0.262
A1	0.381	0.431	D	1.353	1.453
A2	1.240	1.300	D1	0.764	0.964
A3	0.450	0.460	D2	0.18TYP	
B	7.400	7.600	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.150	2.300	θ1	12° TYP	
C1	0.938	1.038	θ2	12° TYP	
C2	0.938	1.2038	θ3	0° ~ 8°	
C3	0.145	0.205			

TSSOP-20L



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	-	1.20	E	6.20	6.60
A1	0.05	0.15	e	0.65BSC	
A2	0.80	1.05	L	0.45	0.75
A3	0.39	0.49	L1	1.00REF	
b	0.20	0.28	θ	0°	8°
b1	0.19	0.25			
c	0.13	0.17			
c1	0.12	0.14			
D	6.40	6.60			
E1	4.30	4.50			

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74HC_HCT574 Rev. 1.0	Apr 24, 2025	Draft datasheet		