



Product Specification

CSD17581Q5A

N-Channel Enhancement Mode MOSFET

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Descriptions

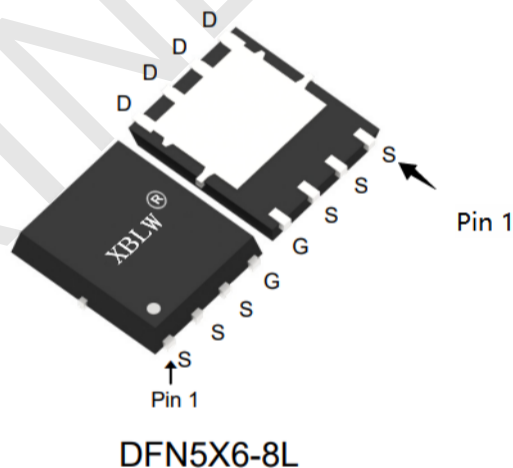
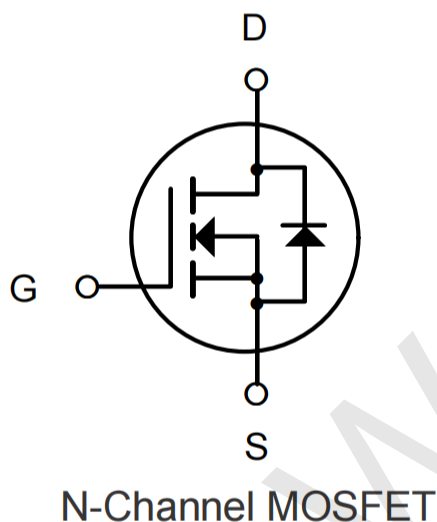
The CSD17581Q5A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

Features

- $V_{DS} = 30V, I_D = 90A$
- $R_{DS(ON)} < 2.4m\Omega$ $V_{GS} = 10V$

Applications

- Battery protection
- Load switch
- Uninterruptible power supply



Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
CSD17581Q5A	DFN5X6-8L	CSD17581	Tape	5000Pcs/Reel

Absolute Maximum Ratings ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 10V ¹	90	A
$I_D@T_c=100^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 10V ¹	65	A
I_{DM}	Pulsed Drain Current ²	160	A
EAS	Single Pulse Avalanche Energy ³	180	mJ
I_{AS}	Avalanche Current	60	A
$P_D@T_c=25^{\circ}\text{C}$	Total Power Dissipation ⁴	187	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.1	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C , I _D =1mA	---	0.014	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =30A	---	2	2.4	mΩ
		V _{GS} =4.5V , I _D =15A	---	2.5	3.2	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V , V _{GS} =0V , T _J =25°C	---	---	1	uA
		V _{DS} =24V , V _{GS} =0V , T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ±20V , V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V , I _D =30A	---	50	---	S
R _g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz	---	1.7	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} = 15V , V _{GS} = 10V , I _D = 15A	---	56.9	---	nC
Q _{gs}	Gate-Source Charge		---	13.8	---	
Q _{gd}	Gate-Drain Charge		---	23.5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} = 15V , V _{GS} =10V , R _G =3.3Ω, I _D =1A	---	20.1	---	ns
T _r	Rise Time		---	6.3	---	
T _{d(off)}	Turn-Off Delay Time		---	124.6	---	
T _f	Fall Time		---	15.8	---	
C _{iss}	Input Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz	---	4345	---	pF
C _{oss}	Output Capacitance		---	340	---	
C _{rss}	Reverse Transfer Capacitance		---	225	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V , Force Current	---	---	90	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =1A , T _J =25°C	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
- 3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=60A.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 85A.

Typical Characteristics

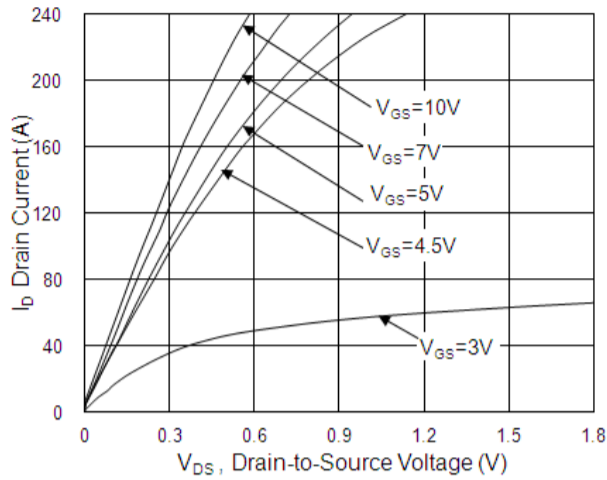


Fig 1. Typical Output Characteristics

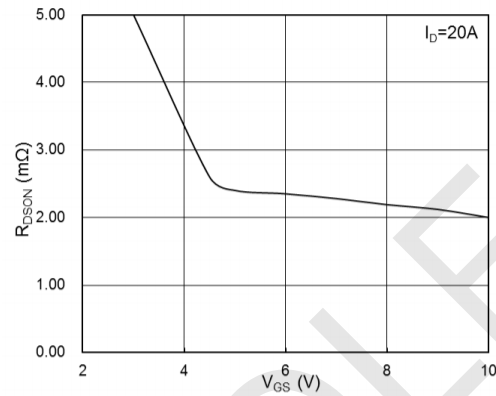


Fig 2. On-Resistance v.s Gate-Source

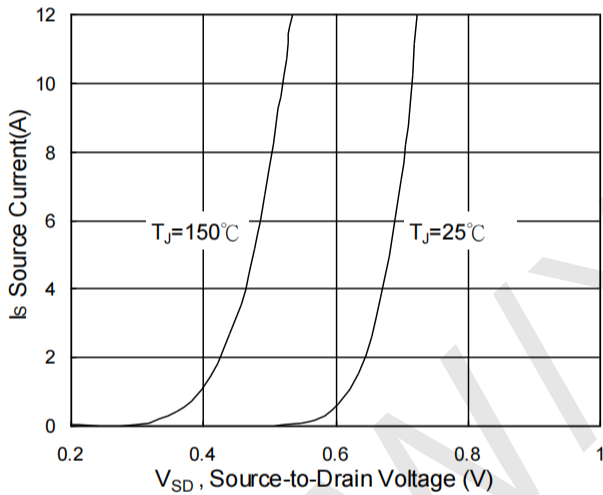


Fig 3. Forward Characteristics of Reverse

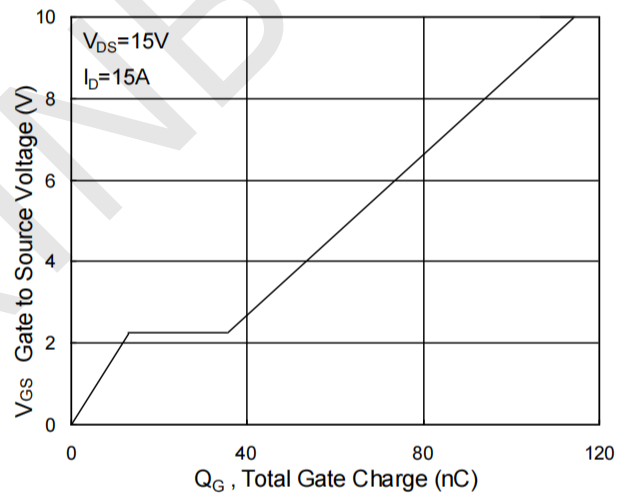


Fig 4. Gate-Charge Characteristics

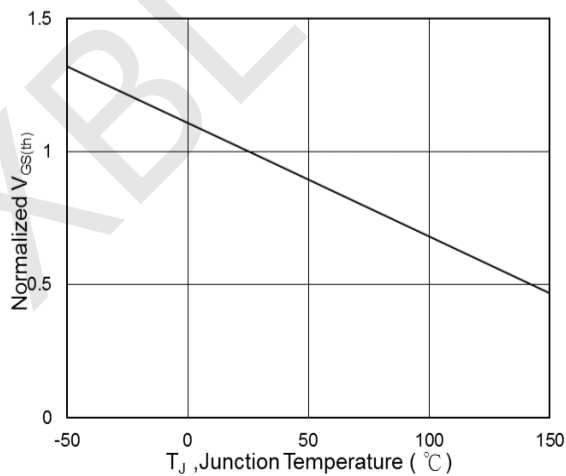


Fig 5. Normalized $V_{GS(th)}$ vs. T_J

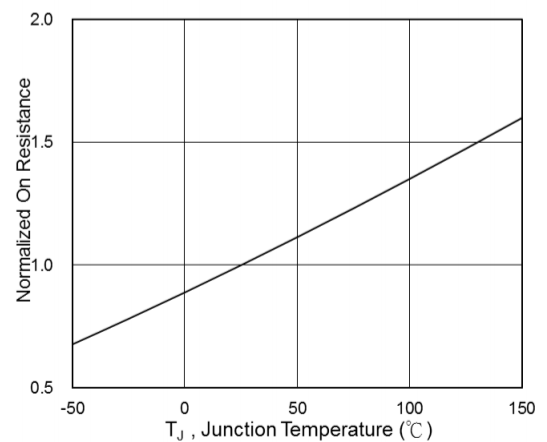


Fig 6. Normalized $R_{DS(on)}$ Vs. T_J

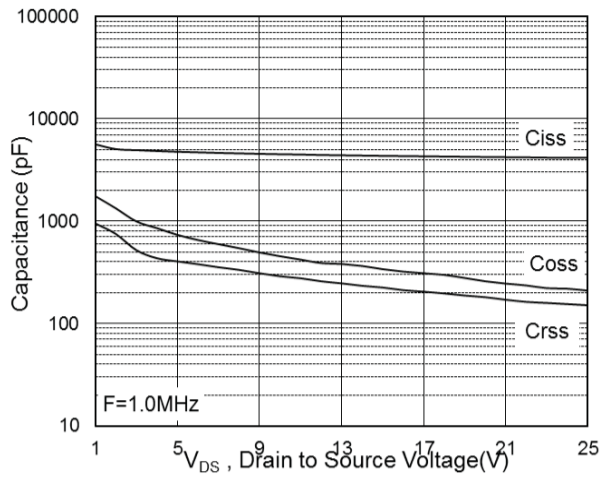


Fig 7. Capacitance

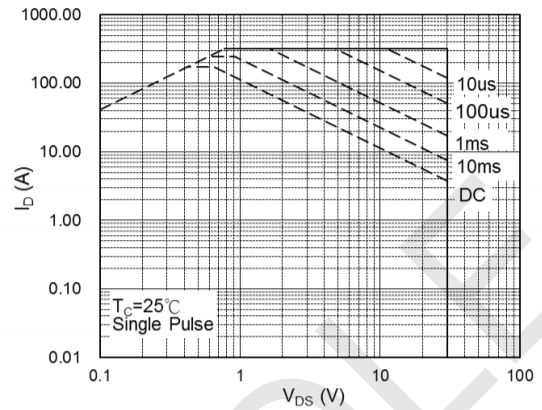


Fig 8. Safe Operating Area

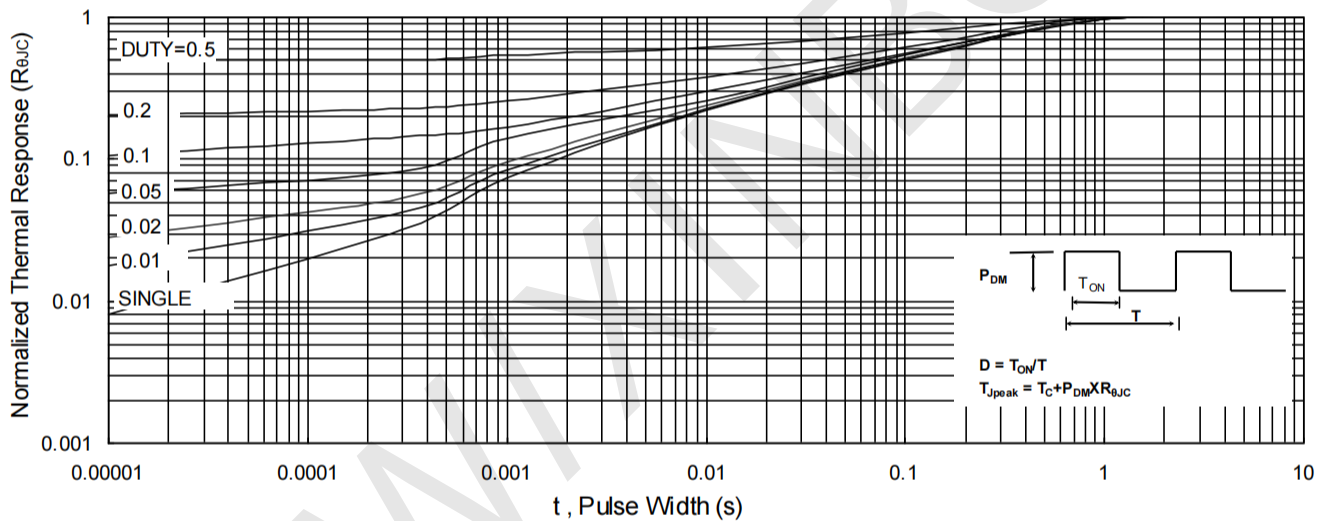


Fig 9. Normalized Maximum Transient Thermal Impedance

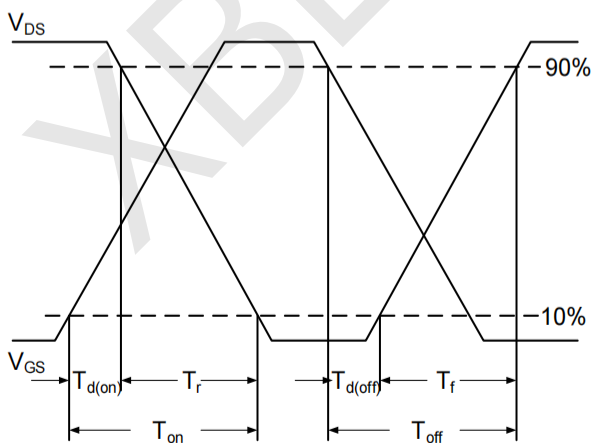


Fig 10. Switching Time Waveform

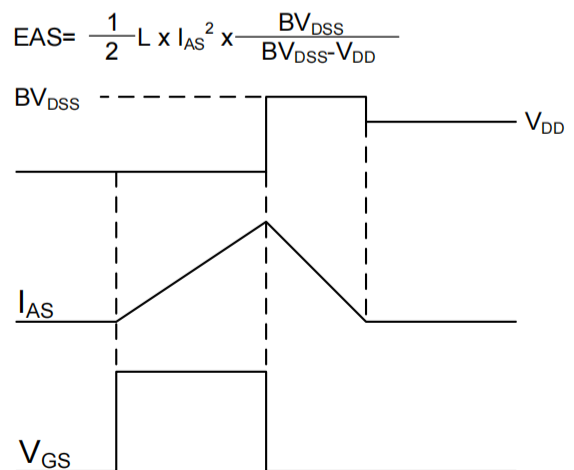
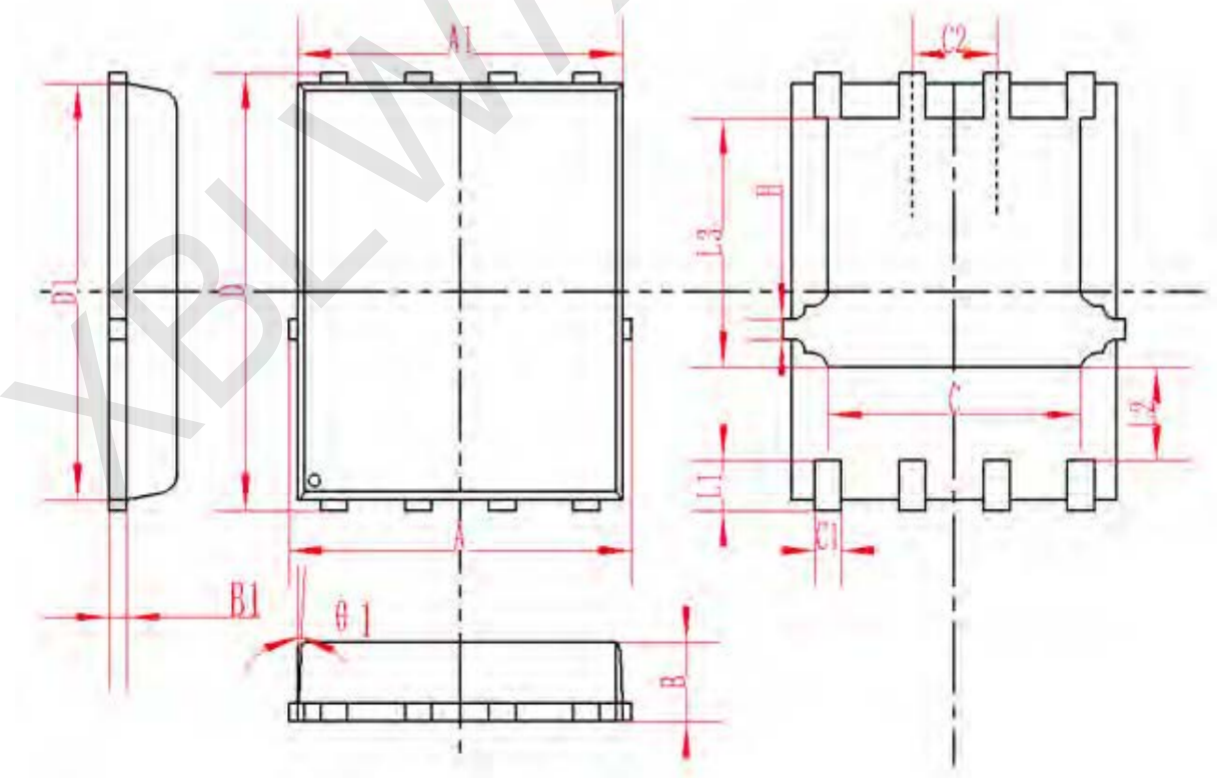


Fig 11. Unclamped Inductive Switching Waveform

Package Information

DFN5X6-8L

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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