1. DESCRIPTION

The XLA3072 3.3V, ±15kV ESD-protected, RS-485/RS-422 transceivers feature one driver and one receiver. These devices include fail-safe circuitry, guaranteeing a logic-high receiver output when receiver inputs are open or shorted. The receiver outputs a logic-high if all transmitters on a terminated bus are disabled (high impedance). The devices include a hot-swap capability to eliminate false transitions on the bus during power-up or hot insertion.

The XLA3072 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing errorfree data transmission up to 250kbps. The XLA3072 are intended for half-duplex communications

The XLA3072 transceivers draw 800µA of supply current when unloaded, or when fully loaded with the drivers disabled. All devices have a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus.

2. FEATURES

- Protection for Robust Performance
  - -±15kV Human Body Model ESD on I/O Pins
  - -True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility
  - -Enhanced Slew-Rate-Limiting Facilitates ErrorFree Data Transmission
  - -Hot-Swap Input Structure on DE and RE
- Flexible Feature Set for Ease of Design
  - -Allows up to 256 Transceivers on the Bus
  - -10µA Shutdown Current Mode for Power Savings

3. APPLICATIONS

- Lighting Systems
- Industrial Control
- Telecom
- Security Systems
- Instrumentation

4. ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND)

Supply Voltage (VCC).....+6V

Control Input Voltage (RE, DE, SLR,

H/F, TXP, RXP).....-0.3V to +6V

Driver Input Voltage (DI).....-0.3V to +6V

Driver Output Voltage (Z, Y, A, B) .....-8V to +13V

Receiver Input Voltage (A, B).....-8V to +13V

Receiver Input Voltage

Receiver Output Voltage (RO) ..... -0.3V to (VCC + 0.3V)

Driver Output Current.....±250mA

Continuous Power Dissipation (TA = +70°C)

8-Pin SO (derate 5.88mW/°C above +70°C).....471mW

Operating Temperature Ranges :

XLA3072..... -40°C to +85°C

Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

5. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output	V_{OD}	R_L = 100Ω (RS422), Figure 1		2		V_{CC}	V
		R_L = 54Ω (RS485), Figure 1		1.5		V_{CC}	
		No load				V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1 (Note 2)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1			V_{CC}/2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 2)				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$, TXP, RXP, H/$\overline{F}$		2			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$, TXP, RXP, H/$\overline{F}$				0.8	V
Input Hysteresis	V_{HYS}	DE, DI, $\overline{RE}$, TXP, RXP, H/$\overline{F}$			100		mV
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±1	µA
Input Impedance First Transition		DE		1		10	kΩ
Input Current	I_{IN2}	TXP, RXP, H/$\overline{F}$ internal pulldown		10		40	µA
SRL Input High Voltage				V_{CC}-0.4			V
SRL Input Middle Voltage				V_{CC} x 0.4		V_{CC} x 0.6	V
SRL Input Low Voltage						0.4	V
SRL Input Current		SRL = V_{CC}				75	µA
		SRL = GND		-75			
Output Leakage (Y and Z) Full Duplex	I_O	DE = GND, V_{CC} = GND or 3.6V	V_{IN} = +12V			125	µA
			V_{IN} = -7V	-100			

DC ELECTRICAL CHARACTERISTICS(continued)

(V_{CC} = 3.3V ±10%, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Short-Circuit Output Current	I_{OSD}	0 ≤ V_{OUT} ≤ 12V (Note 3)		40		250	mA
		-7V ≤ V_{OUT}≤ V_{CC} (Note 3)		-250		-40	
Driver Short-Circuit Foldback Output Current	I_{OSDF}	(V_{CC} - 1V) ≤ V_{OUT} ≤ 12V (Note 3)		20			mA
		-7V ≤ V_{OUT} ≤ 1V (Note 3)				-20	
Thermal-Shutdown Threshold	T_{TS}				175		°C
Thermal-Shutdown Hysteresis	T_{TSH}				15		°C
Input Current (A and B)	$I_{A, B}$	DE = GND, V_{CC} = GND or 3.6V	V_{IN} = +12V			125	µA
			V_{IN} = -7V	-100			
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_A+ V_B = 0V			15		mV
RO Output High Voltage	V_{OH}	I_O = -1mA		V_{CC}-0.6			V
RO Output Low Voltage	V_{OL}	I_O = 1mA				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0 ≤ V_O≤ V_{CC}				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO}≤ V_{CC}				±80	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, $\overline{RE}$ = 0, DE = V_{CC}			0.8	1.5	mA
		No load, $\overline{RE}$ = V_{CC}, DE = V_{CC}			0.8	1.5	
		No load, $\overline{RE}$ = 0, DE = 0			0.8	1.5	
Supply Current in Shutdown Mode	I_{SHDN}	$\overline{RE}$ = V_{CC}, DE = GND			0.05	10	µA
ESD PROTECTION							
ESD Protection for Y, Z, A, and B		Human Body Model			±15		kV

Note 1: All currents into the device are positive. All currents out of the device are negative. All voltages are referred to device ground, unless otherwise noted.

Note 2: ΔVOD and ΔVOC are the changes in VOD and VOC, respectively, when the DI input changes state.

Note 3: The short-circuit output current applies to peak current just prior to foldback current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

6. SWITCHING CHARACTERISTICS

6.1. Driver Switching Characteristics

XLA3072 with SRL = UNCONNECTED (250kbps)

(V_{CC} = 3.3V ±10%, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{DPLH}	C_L= 50pF, R_L= 54Ω, Figures 2 and 3	250		1500	ns
	t_{DPHL}		250		1500	ns
Driver Differential Output Rise or Fall Time	t_{DR} , t_{DF}	C_L= 50pF, R_L= 54Ω, Figures 2 and 3	350		1600	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	C_L= 50pF, R_L= 54Ω, Figures 2 and 3			200	ns
Maximum Data Rate			250			kbps
Driver Enable to Output High	t_{DZH}	Figure 4			2500	ns
Driver Enable to Output Low	t_{DZL}	Figure 5			2500	ns
Driver Disable Time from Low	t_{DLZ}	Figure 5			100	ns
Driver Disable Time from High	t_{DHZ}	Figure 4			100	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figure 4			5500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figure 5			5500	ns
Time to Shutdown	t_{SHDN}		50	200	600	ns

6.2. Receiver Switching Characteristics

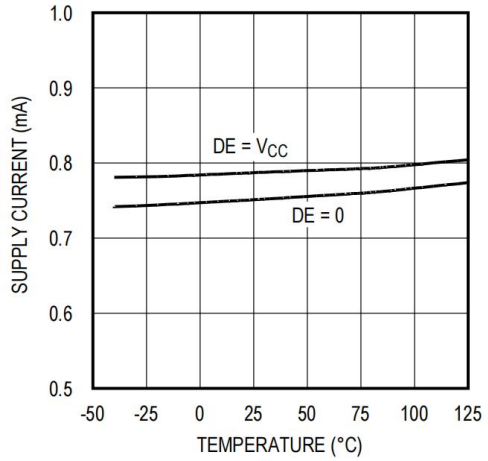
XLA3072 with SRL = UNCONNECTED (250kbps)

(V_{CC} = 3.3V ±10%, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.)

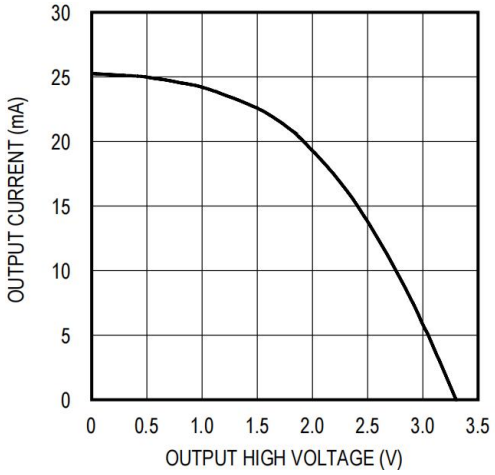
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Propagation Delay	t_{RPLH}	C_L = 15pF, Figures 6 and 7			200	ns
	t_{RPHL}				200	ns
Receiver Output Skew $\lvert t_{RPLH} - t_{RPHL} \rvert$	t_{RSKEW}	C_L = 15pF, Figures 6 and 7			30	ns
Maximum Data Rate			250			kbps
Receiver Enable to Output Low	t_{RZL}	Figure 8			50	ns
Receiver Enable to Output High	t_{RZH}	Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figure 8			4000	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figure 8			4000	ns
Time to Shutdown	t_{SHDN}		50	200	600	ns

7. TYPICAL OPERATING CHARACTERISTICS

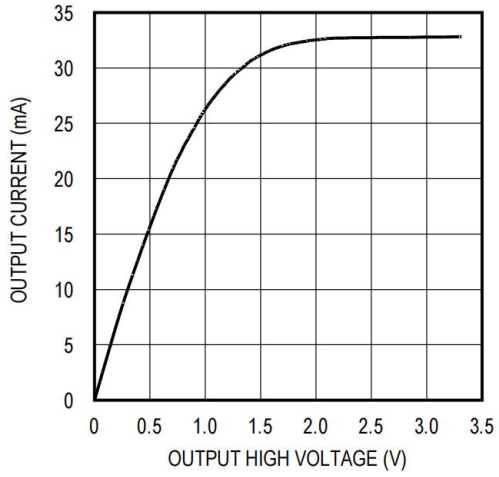
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



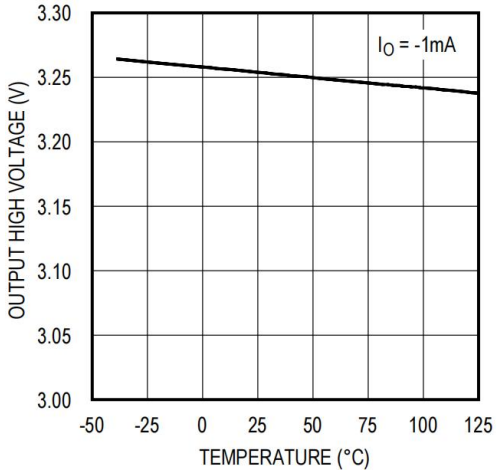
SUPPLY CURRENT vs. TEMPERATURE



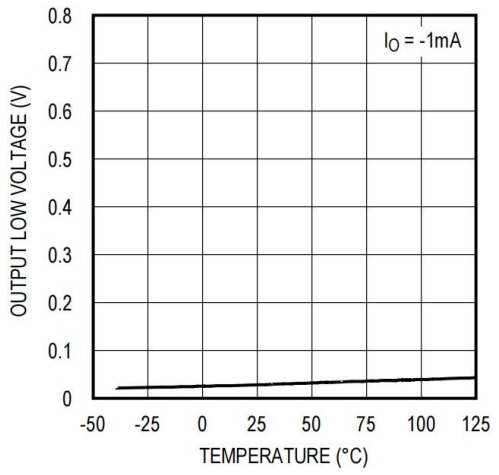
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



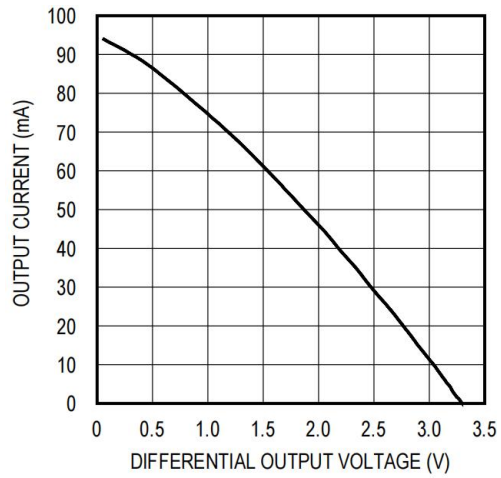
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE

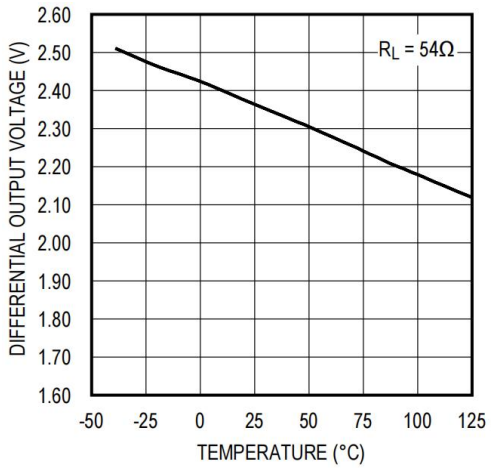


RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE

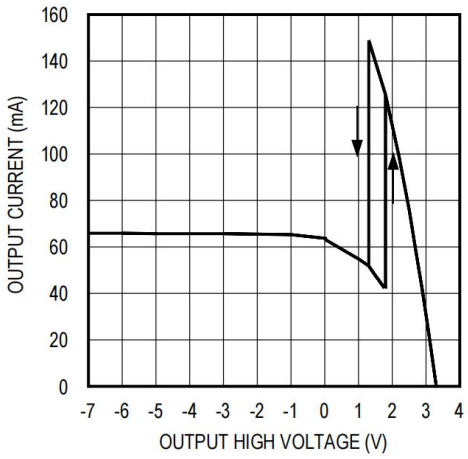


DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE

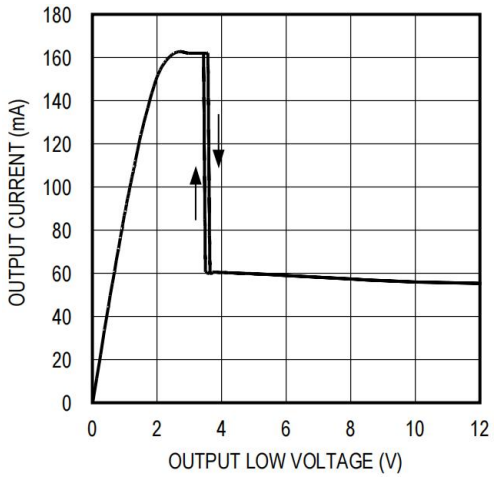
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



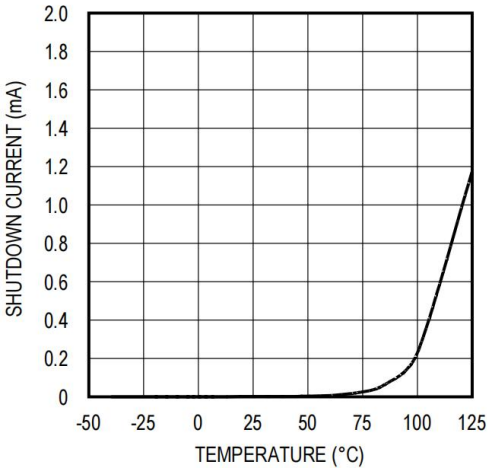
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



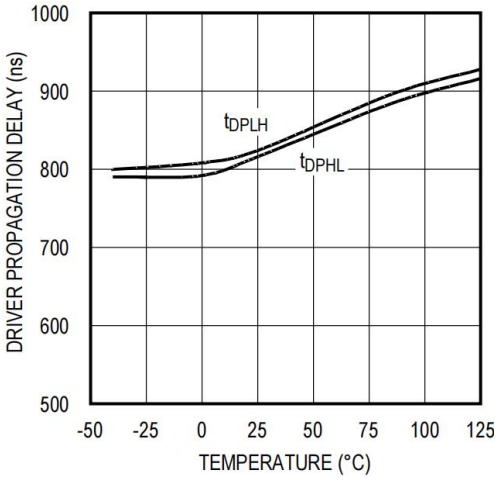
OUTPUT CURRENT vs. TRANSMITTER OUTPUT HIGH VOLTAGE



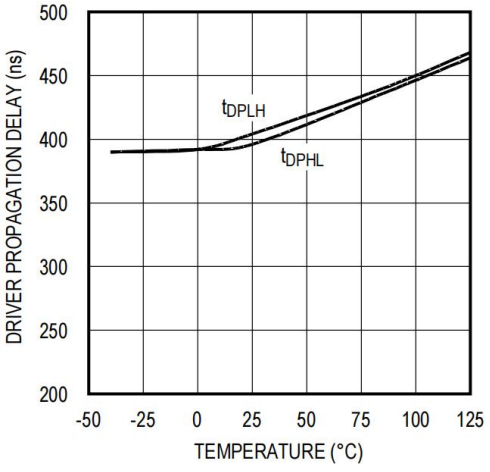
OUTPUT CURRENT vs. TRANSMITTER OUTPUT LOW VOLTAGE



SHUTDOWN CURRENT vs. TEMPERATURE

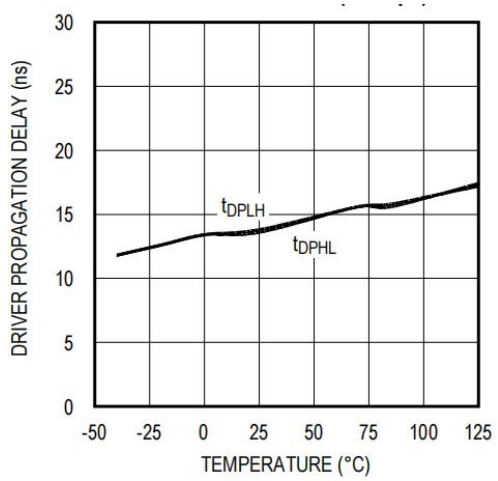


DRIVER PROPAGATION DELAY vs. TEMPERATURE (250kbps)

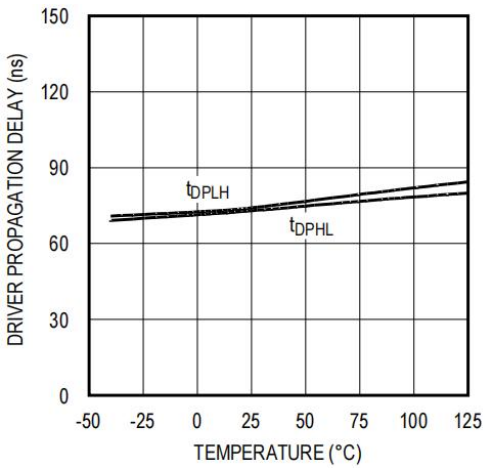


DRIVER PROPAGATION DELAY vs. TEMPERATURE (500kbps)

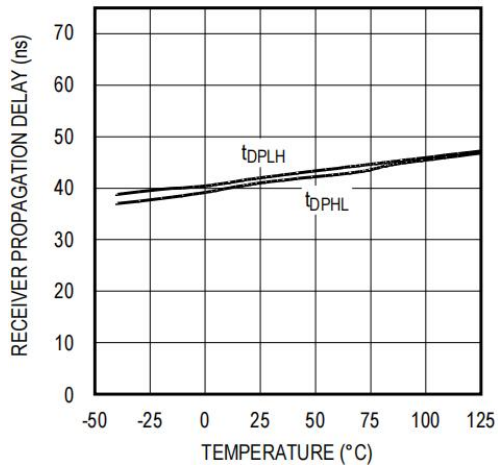
(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)



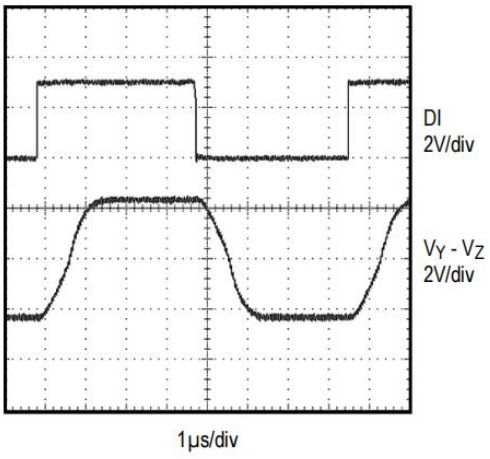
DRIVER PROPAGATION DELAY vs. TEMPERATURE (16Mbps)



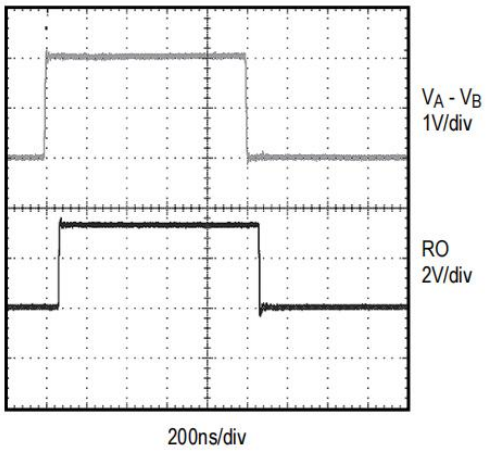
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (250kbps AND 500kbps)



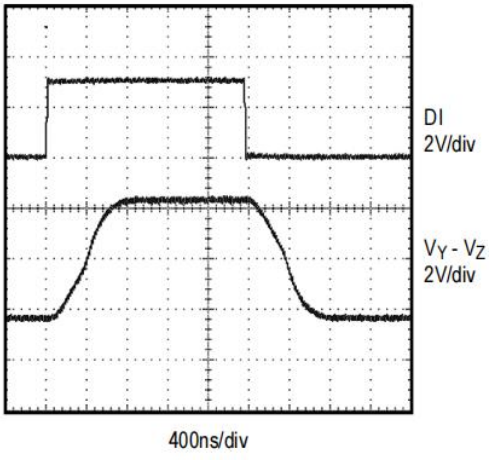
RECEIVER PROPAGATION DELAY vs. TEMPERATURE (16Mbps)



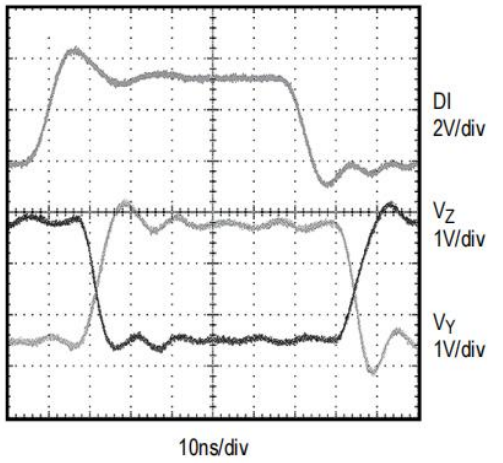
DRIVER PROPAGATION DELAY (250kbps)



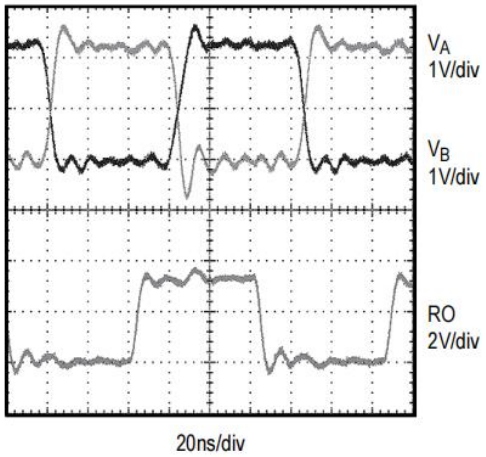
RECEIVER PROPAGATION DELAY (250kbps AND 500kbps)



DRIVER PROPAGATION DELAY (500kbps)



DRIVER PROPAGATION DELAY (16Mbps)



RECEIVER PROPAGATION DELAY (16Mbps)

8. TEST CIRCUITS AND WAVEFORMS

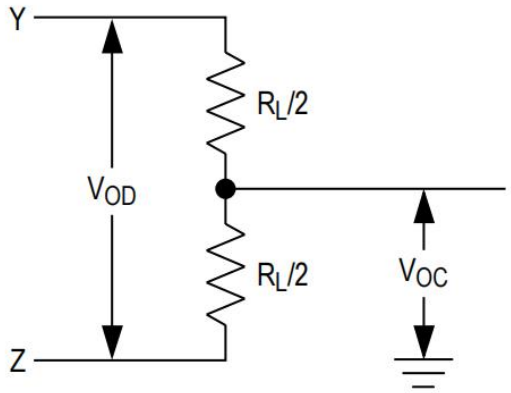


Figure 1. Driver DC Test Load

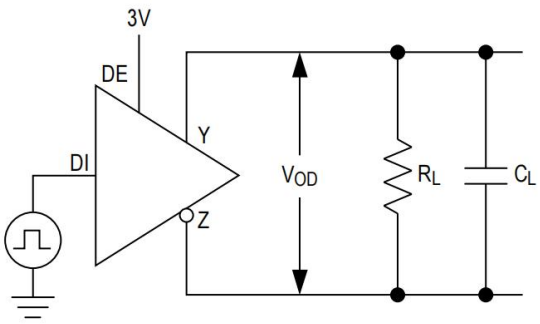


Figure 2. Driver Timing Test Circuit

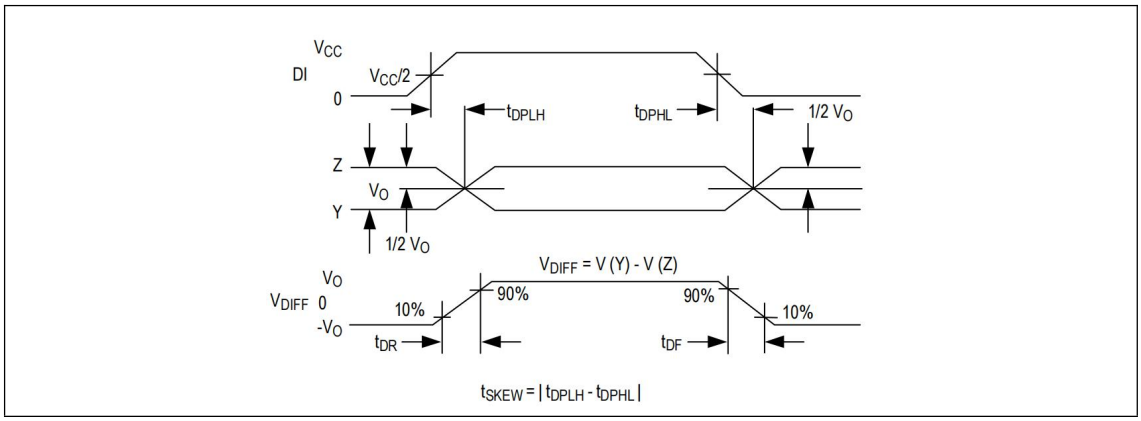


Figure 3. Driver Propagation Delays

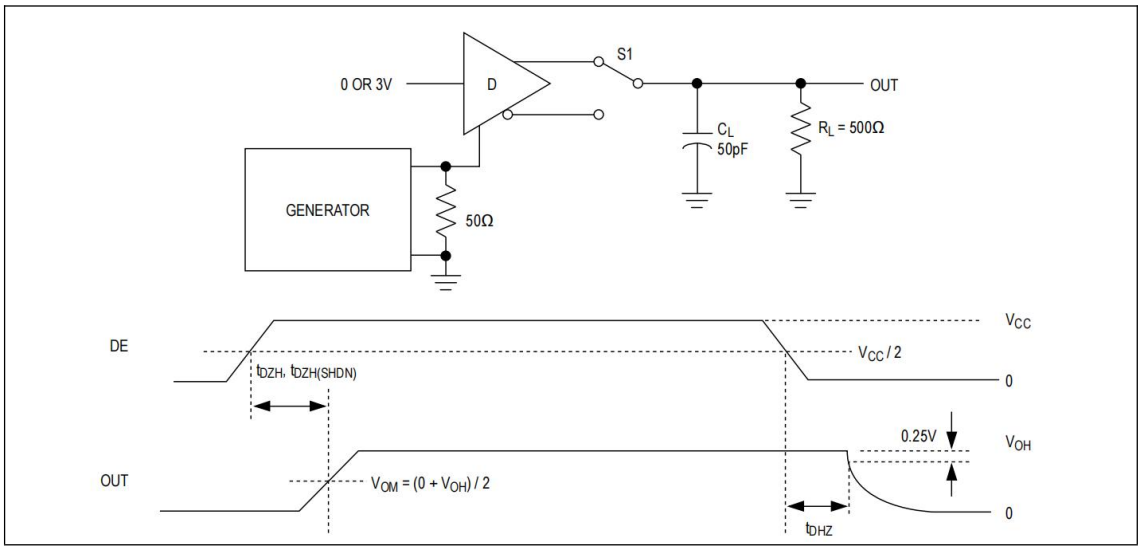


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

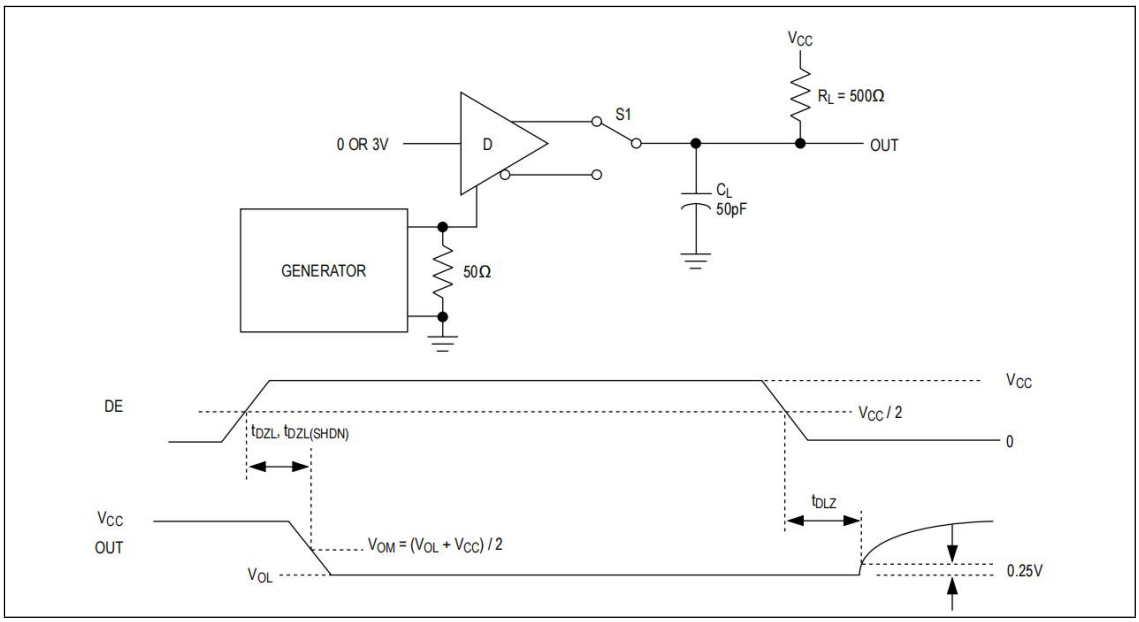


Figure 5. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

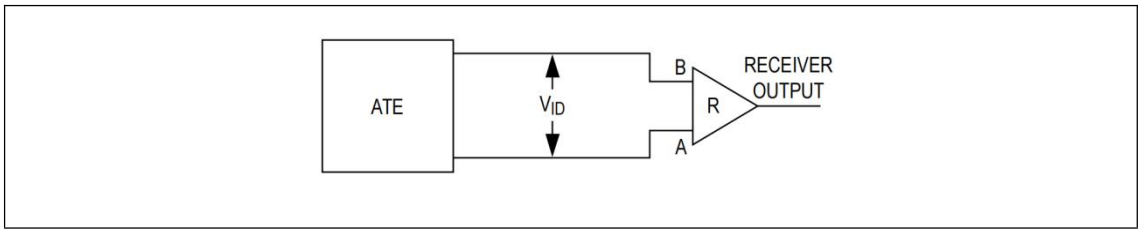


Figure 6. Receiver Propagation Delay Test Circuit

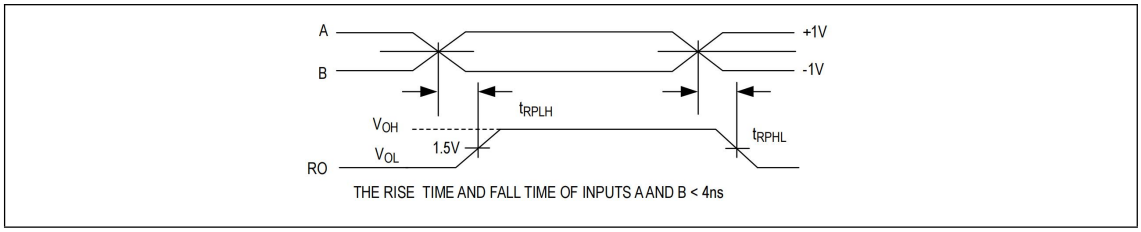


Figure 7. Receiver Propagation Delays

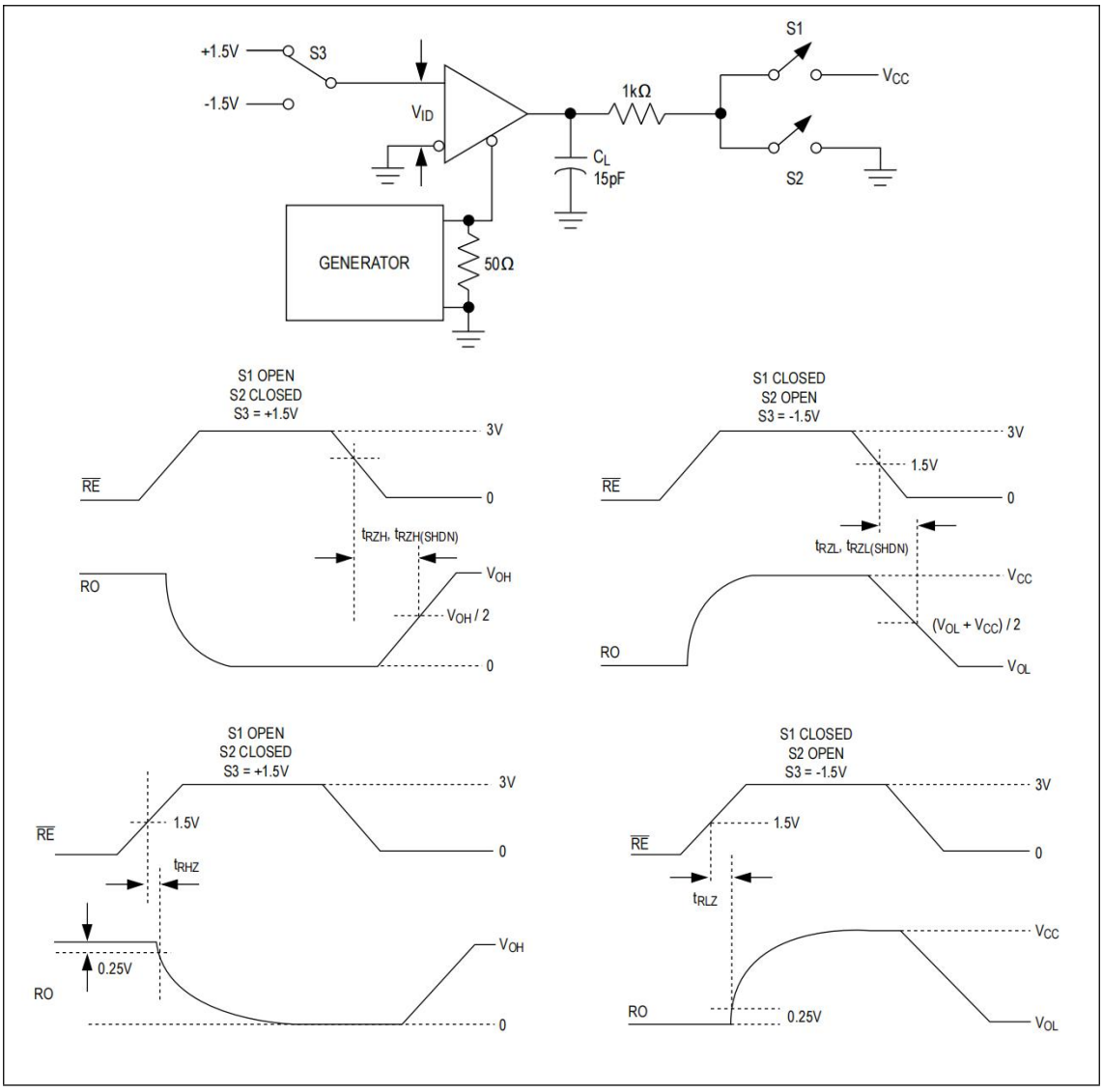


Figure 8. Receiver Enable and Disable Times

9. PIN DESCRIPTION

PIN HALF DUPLEX DEVICES	NAME	FUNCTION
1	RO	Receiver Output. When $\overline{RE}$ is low and if (A - B) ≥ -50mV, RO is high; if (A - B) ≤ -200mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input (see the Hot-Swap Capability section for details).
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the HotSwap Capability section for details).
4	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
5	GND	Ground
7	B	Inverting Receiver Input and Inverting Driver Output
6	A	Noninverting Receiver Input and Noninverting Driver Output
8	V_{CC}	Positive Supply V_{CC} = 3.3V ±10%. Bypass V_{CC} to GND with a 0.1µF capacitor.

10. FUNCTION TABLES

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B/Z	A/Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-z	High-z
1	0	X	Shutdown	

11. DETAILED DESCRIPTION

The XLA3072 high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The devices also feature a hot-swap capability allowing line insertion without erroneous data transfer (see the HotSwap Capability section). The XLA3072 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps.

The XLA3072 are half-duplex transceivers.

All devices operate from a single 3.3V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

11.1. Receiver Input Filtering

The receivers of the XLA3072 when operating in 250kbps mode, incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 25% due to this filtering.

11.2. Fail-Safe

The XLA3072 guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If A - B is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the XLA3072, this results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

11.3. Hot-Swap Inputs

When circuit boards are inserted into a hot, or powered, backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of these devices to a defined logic level. Leakage currents up to ±10µA from the highimpedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hotswap tolerable input.

11.4. Hot-Swap Input Circuitry

The enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal 10µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 500µA current sink, and M1, a 100µA current sink, pull DE to GND through a 5kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$ there is a complementary circuit employing two PMOS devices pulling $\overline{RE}$ to V_{CC}.

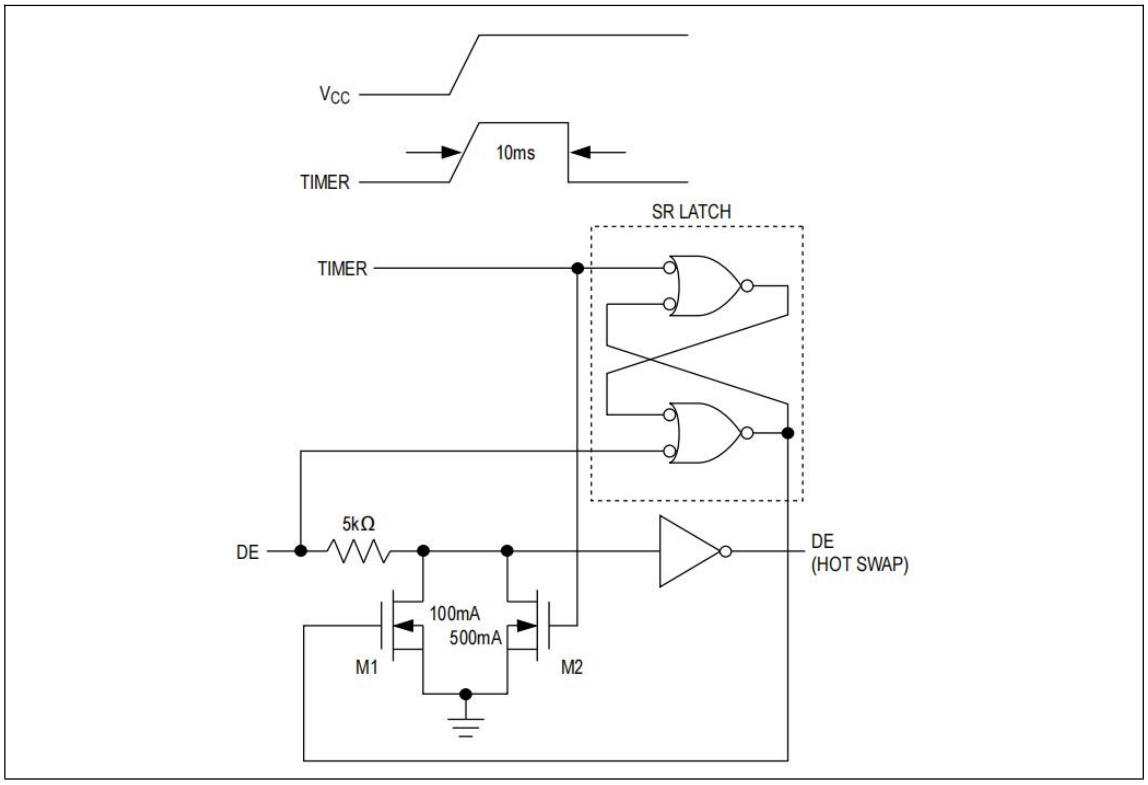


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

11.5. ±15kV ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the XLA3070 family of devices have extra protection against static electricity. Maxim's engineers have developed state-ofthe-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the devices keep working without latchup or damage. ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the devices are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±6kV using the Contact Discharge method specified in IEC 1000-4-2

11.6. ESD Test Conditions

ESD performance depends on a variety of conditions.

11.7. Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

11.8. IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The XLA3072of devices helps you design equipment to meet IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2, because series resistance isower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 1000-4-2 model, and Figure 10d shows the current waveform for IEC 1000-4-2 ESD Contact Discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

12. Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. Of course, all pins require this protection, not just RS-485 inputs and outputs.

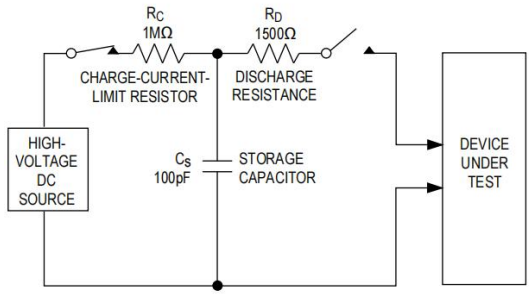


Figure 10a. Human Body ESD Test Model

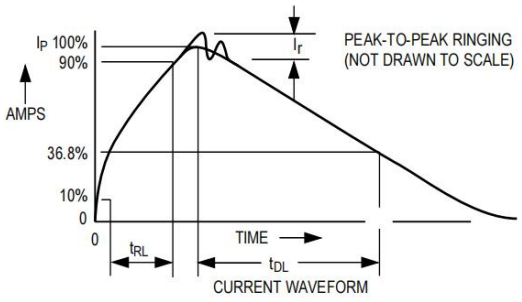


Figure 10b. Human Body Current Waveform

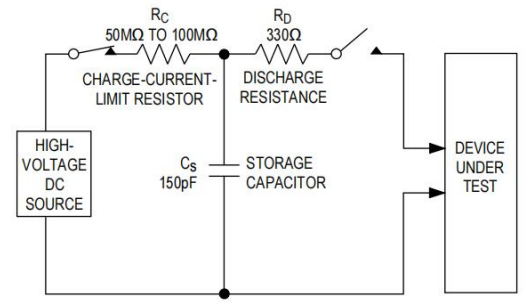


Figure 10c. IEC 1000-4-2 ESD Test Model

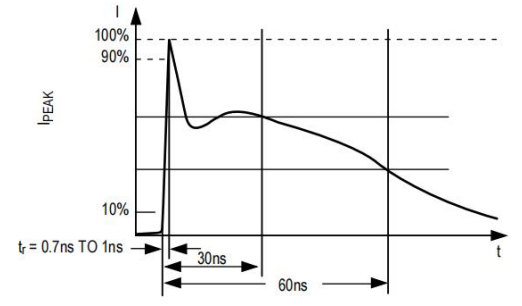


Figure 10d. IEC 1000-4-2 ESD Generator Current Waveform

13. APPLICATIONS INFORMATION

13.1. 256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (1-unit load), and the standard driver can drive up to 32-unit loads. The XLA3072of transceivers has a 1/8-unit load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices as well as other RS-485 transceivers with a total of 32-unit loads or fewer can be connected to the line.

13.2. Reduced EMI and Reflections

The XLA3072 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing errorfree data transmission up to 250kbps.

13.3. Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both RE high and DE low. In shutdown, the devices typically draw only 50nA of supply current.

RE and DE can be driven simultaneously; the parts are guaranteed not to enter shutdown if RE is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

Enable times t_{ZH} and t_{ZL} (see the SwitchingCharacteristics section) assume the part was not in a low-power shutdown state. Enable times $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ assume the parts were shut down. It takes drivers and receivers longer to become enabled from low-power shutdown mode ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

13.4. Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the Typical Operating Characteristics). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

13.5. Typical Applications

The XLA3072 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 11 show typical network application circuits.

To minimize reflections, terminate the line at both ends in its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate limited XLA3072 the two modes of the are more tolerant of imperfect termination.

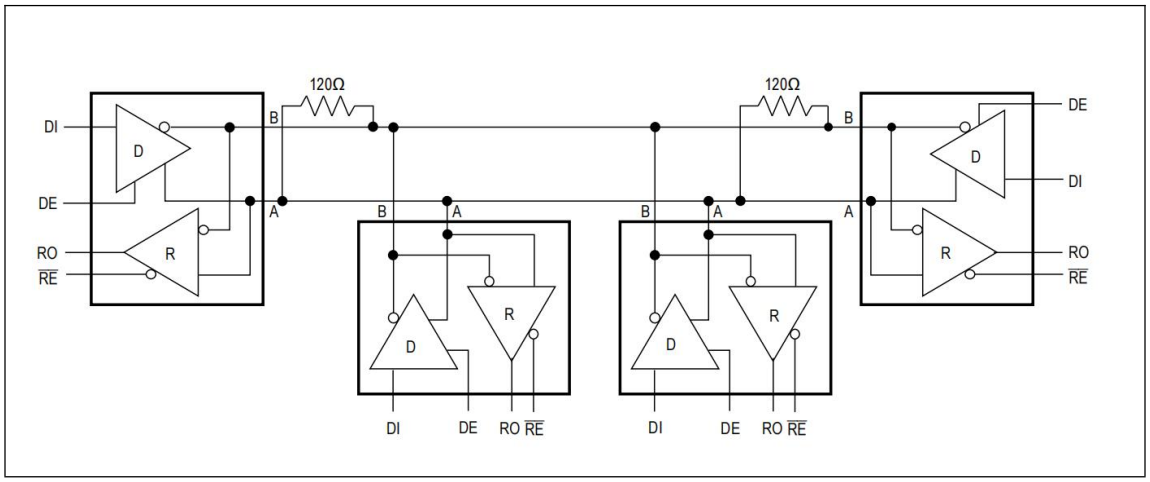
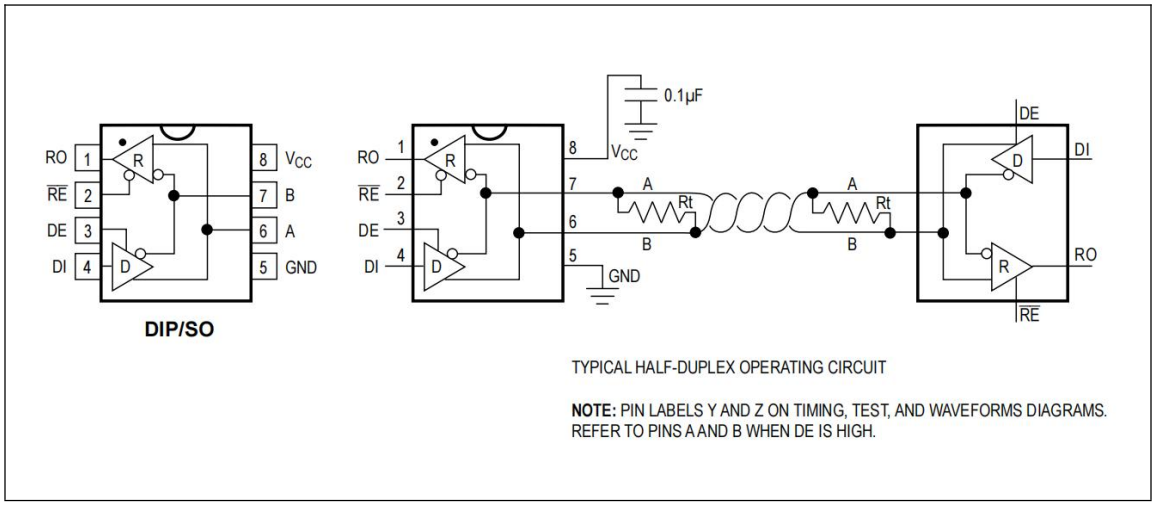


Figure 11. Typical Half-Duplex RS-485 Network

14. Pin Configurations and Typical Operating Circuits



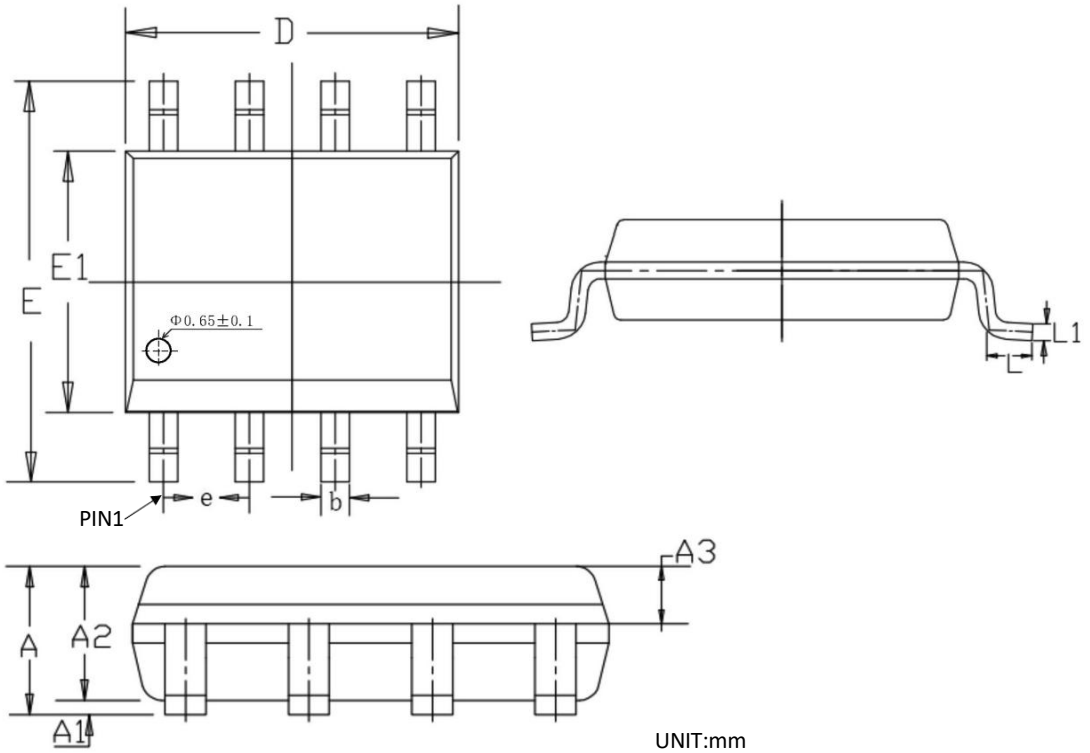
15. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLA3072EESA	XLA3072	SOP-8	4.90*3.90	-40 to +85	MSL3	T&R	2500

16. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—