

Sensitive Gate Silicon Controlled Rectifiers

Features

- ◆ Repetitive Peak Off-State Voltage : 600V
- ◆ R.M.S On-State Current ($I_{T(RMS)} = 0.8\text{ A}$)
- ◆ Low On-State Voltage (1.2V(Typ.)@ I_{TM})
- ◆ Available with tape & reel

General Description

Sensitive triggering SCR is suitable for the application where gate current limited such as small motor control, gate driver for large SCR, sensing and detecting circuits.

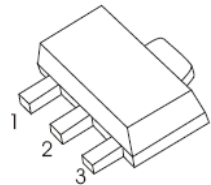
MARKING: T169

SOT-89-3L

1.KATHODE

2.ANODE

3.GATE



Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Condition	Ratings	Units
V_{DRM}	Repetitive Peak Off-State Voltage		600	V
$I_{T(AV)}$	Average On-State Current	Half Sine Wave : $T_C = 112^\circ\text{C}$	0.5	A
$I_{T(RMS)}$	R.M.S On-State Current	All Conduction Angle	0.8	A
I_{TSM}	Surge On-State Current	1/2 Cycle, 60Hz, Sine Wave Non-Repetitive	10	A
I^2t	I^2t for Fusing	$t = 8.3\text{ms}$	0.415	A^2s
P_{GM}	Forward Peak Gate Power Dissipation		2	W
$P_{G(AV)}$	Forward Average Gate Power Dissipation		0.1	W
I_{FGM}	Forward Peak Gate Current		1	A
V_{RGM}	Reverse Peak Gate Voltage		5.0	V
T_J	Operating Junction Temperature		- 40 ~ 125	$^\circ\text{C}$
T_{STG}	Storage Temperature		- 40 ~ 150	$^\circ\text{C}$

Electrical Characteristics ($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Symbol	Items	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
I_{DRM}	Repetitive Peak Off-State Current	$V_{\text{AK}} = V_{\text{DRM}}$ or V_{RRM} ; $R_{\text{GK}} = 1000\ \Omega$ $T_C = 25\text{ }^{\circ}\text{C}$ $T_C = 125\text{ }^{\circ}\text{C}$	— —	— —	10 200	μA
V_{TM}	Peak On-State Voltage (1)	($I_{\text{TM}} = 1\text{ A}$, Peak)	—	1.2	1.7	V
I_{GT}	Gate Trigger Current (2)	$V_{\text{AK}} = 6\text{ V}$, $R_L = 100\ \Omega$ $T_C = 25\text{ }^{\circ}\text{C}$ $T_C = -40\text{ }^{\circ}\text{C}$	— —	— —	200 500	μA
V_{GT}	Gate Trigger Voltage (2)	$V_D = 7\text{ V}$, $R_L = 100\ \Omega$ $T_C = 25\text{ }^{\circ}\text{C}$ $T_C = -40\text{ }^{\circ}\text{C}$	— —	— —	0.8 1.2	V
V_{GD}	Non-Trigger Gate Voltage (1)	$V_{\text{AK}} = 12\text{ V}$, $R_L = 100\ \Omega$ $T_C = 125\text{ }^{\circ}\text{C}$	0.2	—	—	V
dv/dt	Critical Rate of Rise Off-State Voltage	$V_D = \text{Rated } V_{\text{DRM}}$, Exponential waveform, $R_{\text{GK}} = 1000\ \Omega$ $T_J = 125\text{ }^{\circ}\text{C}$	500	800	—	$\text{V}/\mu\text{s}$
di/dt	Critical Rate of Rise On-State Current	$I_{\text{PK}} = 20\text{ A}$; $P_W = 10\mu\text{s}$; $di_G/dt = 1\text{ A}/\mu\text{s}$ $I_{\text{gt}} = 20\text{ mA}$	—	—	50	$\text{A}/\mu\text{s}$
I_{H}	Holding Current	$V_{\text{AK}} = 12\text{ V}$, Gate Open Initiating Current = 20mA $T_C = 25\text{ }^{\circ}\text{C}$ $T_C = -40\text{ }^{\circ}\text{C}$	— —	2 —	5.0 10	mA
$R_{\text{th(j-c)}}$	Thermal Impedance	Junction to case	—	—	15	$^{\circ}\text{C}/\text{W}$
$R_{\text{th(j-a)}}$	Thermal Impedance	Junction to Ambient	—	—	125	$^{\circ}\text{C}/\text{W}$

※ Notes :

1. Pulse Width $\leq 1.0\text{ ms}$, Duty cycle $\leq 1\%$
2. Does not include R_{GK} in measurement.

Typical Characteristics

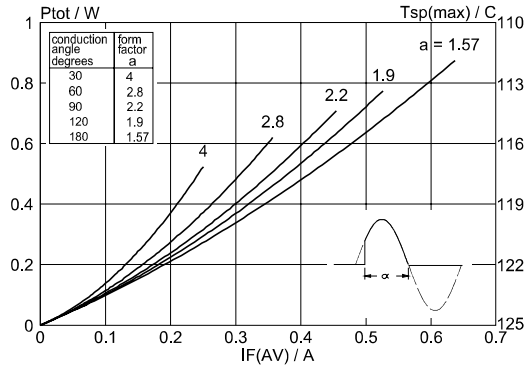


Fig.1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)}/I_{T(AV)}$.

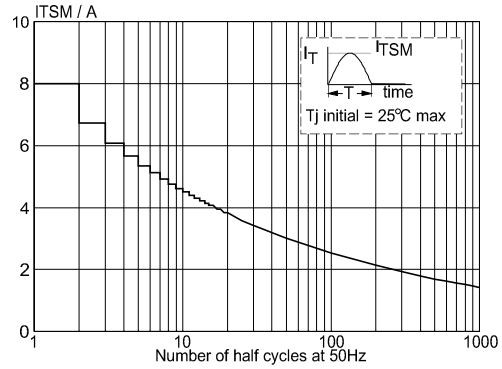


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50 \text{ Hz}$.

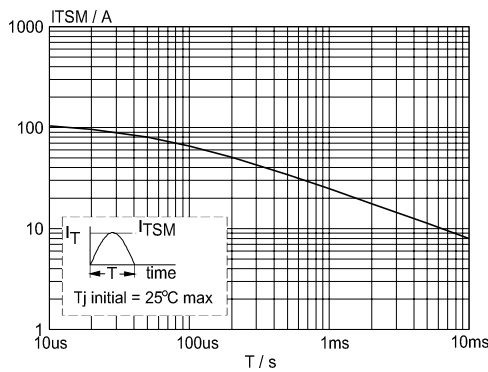


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10 \text{ ms}$.

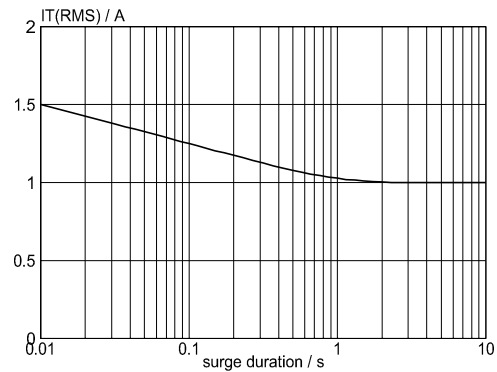


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50 \text{ Hz}$; $T_{sp} \leq 112^\circ \text{C}$.

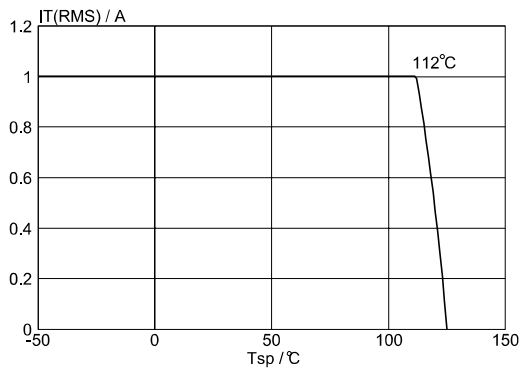


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp} .

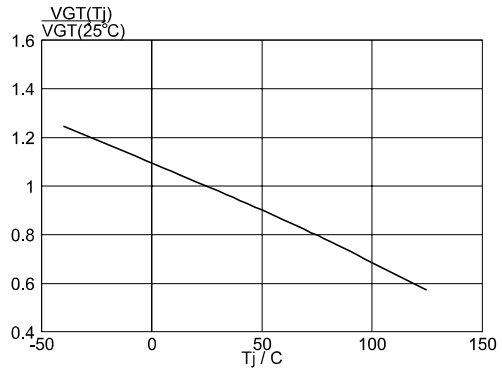


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ \text{C})$, versus junction temperature T_j .

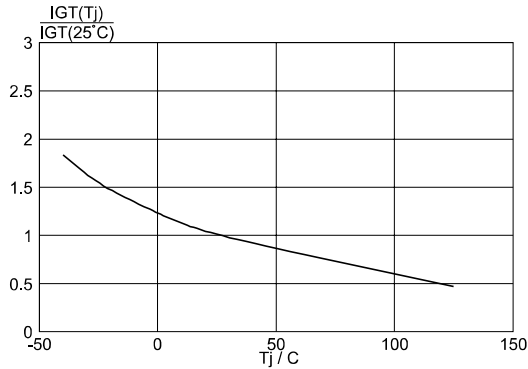


Fig. 7. Normalised gate trigger current $I_{GT}(T_J) / I_{GT}(25^\circ\text{C})$, versus junction temperature T_J .

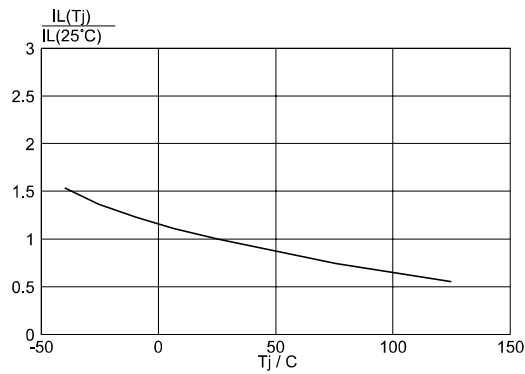


Fig. 8. Normalised latching current $I_L(T_J) / I_L(25^\circ\text{C})$, versus junction temperature T_J , $R_{GK} = 1\text{ k}\Omega$.

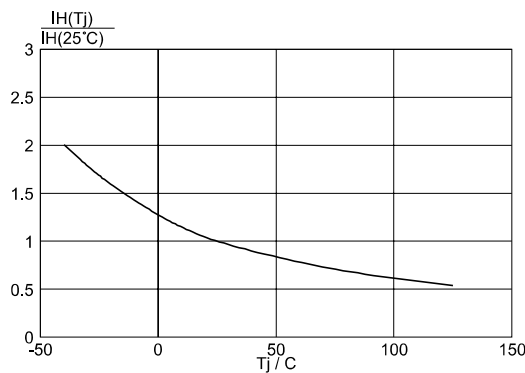


Fig. 9. Normalised holding current $I_H(T_J) / I_H(25^\circ\text{C})$, versus junction temperature T_J , $R_{GK} = 1\text{ k}\Omega$.

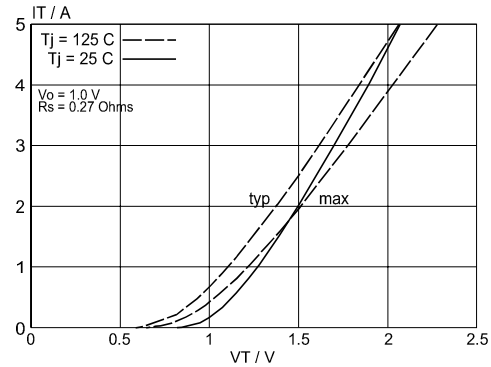


Fig. 10. Typical and maximum on-state characteristic.

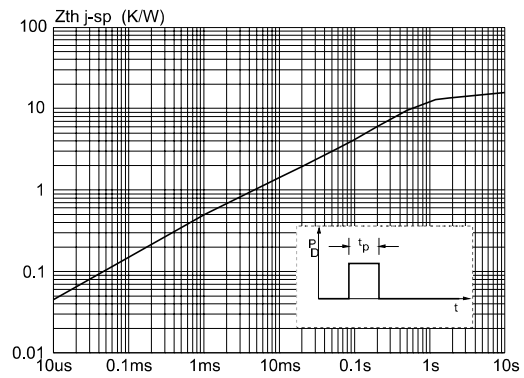


Fig. 11. Transient thermal impedance $Z_{th\ j-sp}$ versus pulse width t_p .

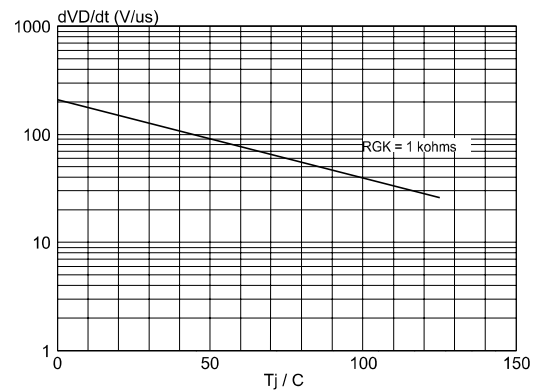


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_J .