

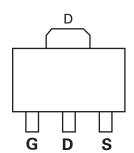
# BSS87,115-VB Datasheet N-Channel 200 V (D-S) MOSFET

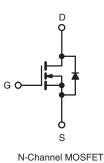
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	200					
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.8				
Q <sub>g</sub> (Max.) (nC)	8.2					
Q <sub>gs</sub> (nC)	1.8					
Q <sub>gd</sub> (nC)	4.5					
Configuration	Single					

#### **FEATURES**

- · Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Fast switching
- Ease of paralleling
- Simple drive requirements







ABSOLUTE MAXIMUM RATINGS (To	c = 25 °C, unl	ess otherwis	se noted)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		$V_{DS}$	200	.,	
Gate-Source Voltage	$V_{GS}$	± 20	V		
Continuous Drain Current	\/ at 10 \/	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C		2.0	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	1.2	Α
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	7.7		
Linear Derating Factor		0.025	W/°C		
Linear Derating Factor (PCB Mount) e		0.017	¬ w/ c		
Single Pulse Avalanche Energy b		E <sub>AS</sub>	50	mJ	
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub> 0.96		А		
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	0.31	mJ		
Maximum Power Dissipation $T_C = 25  ^{\circ}C$			P <sub>D</sub>	3.1	w
Maximum Power Dissipation (PCB Mount) e	T <sub>A</sub> =	T <sub>A</sub> = 25 °C		2.0	VV
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	5.0	V/ns		
Operating Junction and Storage Temperature Ran	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	- °C		
Soldering Recommendations (Peak Temperature)		300	7		

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 81 mH,  $R_G$  = 25  $\Omega$ ,  $I_{AS}$  = 0.96 A (see fig. 12). c.  $I_{SD} \le 3.3$  A,  $dI/dt \le 70$  A/µs,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT			
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	40	°C/W			
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1	60				

#### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS			TYP.	MAX.	UNIT
Static				L	L		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> :	200	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I <sub>D</sub> = 1 mA	-	0.30	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			25	
zero date voltage Drain Current		V <sub>DS</sub> = 160 \	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			250	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	$I_D = 0.58 \text{ A}^{\text{ b}}$	-	0.8	-	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> =	= 50 V, I <sub>D</sub> = 0.58 A	0.51	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$		$V_{GS} = 0 V$	-	140	-	pF
Output Capacitance	$C_{oss}$		$V_{DS} = 25 \text{ V},$	-	53	-	
Reverse Transfer Capacitance	$C_{rss}$	f = 1	f = 1.0 MHz, see fig. 5		15	-	
Total Gate Charge	Qg			=.	-	8.2	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$I_D = 3.3 \text{ A}, V_{DS} = 160 \text{ V},$ see fig. 6 and 13 b	=	-	1.8	nC
Gate-Drain Charge	Q <sub>gd</sub>		See lig. 6 dild 16	-	-	4.5	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = 100 \text{ V}, I_{D} = 3.3 \text{ A},$ $R_{g} = 24 \Omega, R_{D} = 30 \Omega, \text{ see fig. } 10^{\text{ b}}$		=.	8.2	-	ns
Rise Time	t <sub>r</sub>			=	17	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	14	-	
Fall Time	t <sub>f</sub>		1			-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from		-	4.0	-	nH
Internal Source Inductance	L <sub>S</sub>	package and die contact	-	6.0	-	ווח	
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the		-	-	0.96	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	integral revers p - n junction	-	-	7.7		
Body Diode Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C},  I_S = 0.96  \text{A},  V_{GS} = 0  \text{V}^{ \text{b}}$		=	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	- T <sub>.I</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dl/dt = 100 A/µs b		-	150	310	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1J = 25 °C, I <sub>F</sub>	-	0.60	1.4	μC	
Forward Turn-On Time	t <sub>on</sub>	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	y L <sub>S</sub> and	L <sub>D</sub> )

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300~\mu s$ ; duty cycle  $\leq 2~\%$ .



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

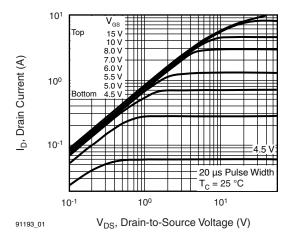


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

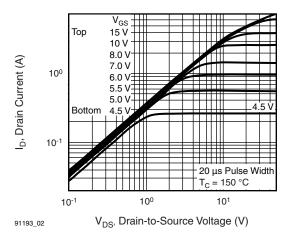


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

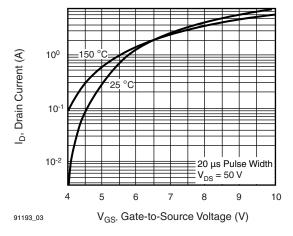


Fig. 3 - Typical Transfer Characteristics

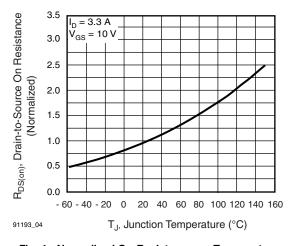


Fig. 4 - Normalized On-Resistance vs. Temperature

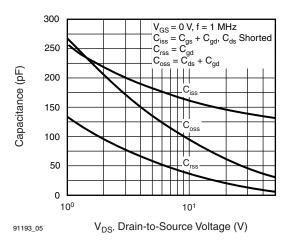


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

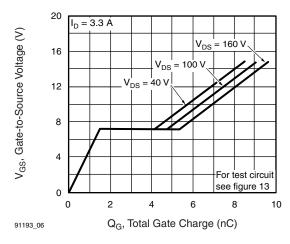


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



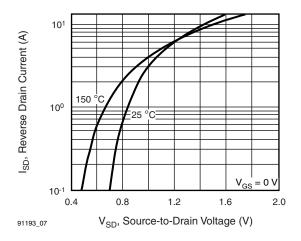


Fig. 7 - Typical Source-Drain Diode Forward Voltage

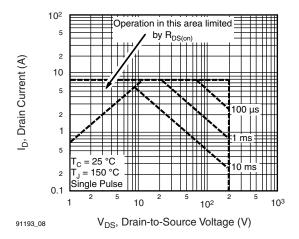


Fig. 8 - Maximum Safe Operating Area

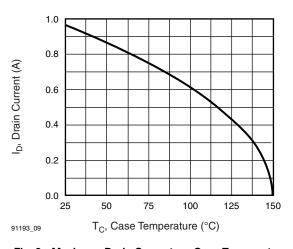


Fig. 9 - Maximum Drain Current vs. Case Temperature

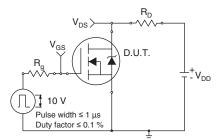


Fig. 10a - Switching Time Test Circuit

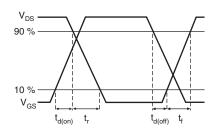


Fig. 10b - Switching Time Waveforms

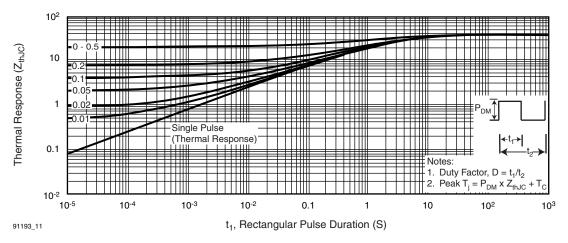


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



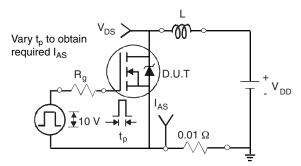


Fig. 12a - Unclamped Inductive Test Circuit

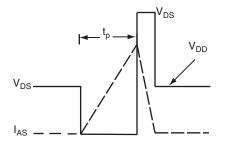


Fig. 12b - Unclamped Inductive Waveforms

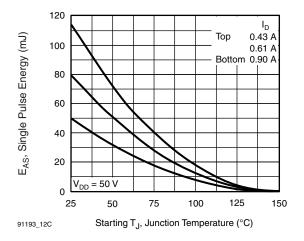


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

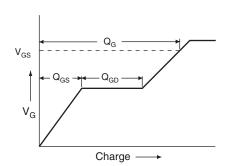


Fig. 13a - Basic Gate Charge Waveform

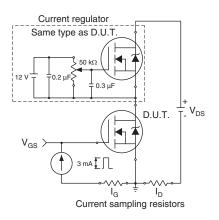
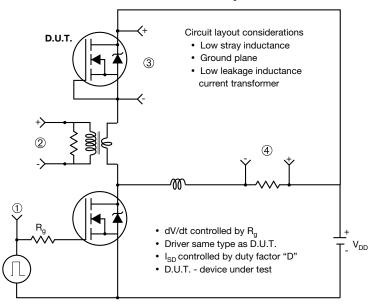


Fig. 13b - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



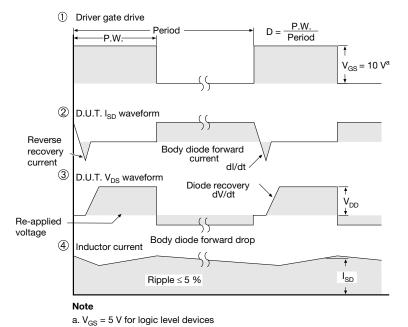
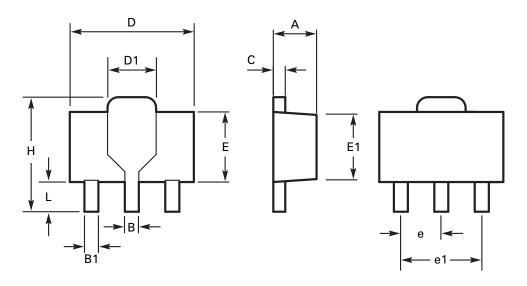


Fig. 14 - For N-Channel



### Package outline - SOT89



DIM	Millin	neters	Inc	hes	DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
Α	1.40	1.60	0.550	0.630	Е	2.29	2.60	0.090	0.102
В	0.44	0.56	0.017	0.022	E1	2.13	2.29	0.084	0.090
B1	0.36	0.48	0.014	0.019	е	1.50 BSC		0.059 BSC	
С	0.35	0.44	0.014	0.017	e1	3.00 BSC		0.118 BSC	
D	4.40	4.60	0.173	0.181	Н	3.94	4.25	0.155	0.167
D1	1.62	1.83	0.064	0.072	L	0.89	1.20	0.035	0.047

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches



# **Disclaimer**

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

Taiwan VBsemi Electronics Co., Ltd., branches, agents, employees, and all persons acting on its or their representatives (collectively, the "Taiwan VBsemi"), assumes no responsibility for any errors, inaccuracies or incomplete data contained in the table or any other any disclosure of any information related to the product.(www.VBsemi.com)

Taiwan VBsemi makes no guarantee, representation or warranty on the product for any particular purpose of any goods or continuous production. To the maximum extent permitted by applicable law on Taiwan VBsemi relinquished: (1) any application and all liability arising out of or use of any products; (2) any and all liability, including but not limited to special, consequential damages or incidental; (3) any and all implied warranties, including a particular purpose, non-infringement and merchantability guarantee.

Statement on certain types of applications are based on knowledge of the product is often used in a typical application of the general product VBsemi Taiwan demand that the Taiwan VBsemi of. Statement on whether the product is suitable for a particular application is non-binding. It is the customer's responsibility to verify specific product features in the products described in the specification is appropriate for use in a particular application. Parameter data sheets and technical specifications can be provided may vary depending on the application and performance over time. All operating parameters, including typical parameters must be made by customer's technical experts validated for each customer application. Product specifications do not expand or modify Taiwan VBsemi purchasing terms and conditions, including but not limited to warranty herein.

Unless expressly stated in writing, Taiwan VBsemi products are not intended for use in medical, life saving, or life sustaining applications or any other application. Wherein VBsemi product failure could lead to personal injury or death, use or sale of products used in Taiwan VBsemi such applications using client did not express their own risk. Contact your authorized Taiwan VBsemi people who are related to product design applications and other terms and conditions in writing.

The information provided in this document and the company's products without a license, express or implied, by estoppel or otherwise, to any intellectual property rights granted to the VBsemi act or document. Product names and trademarks referred to herein are trademarks of their respective representatives will be all.

## **Material Category Policy**

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be oHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.