MP9931

100V Input, Synchronous Step-Down Controller

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP9931 is a high-voltage, synchronous step-down switching regulator controller that can directly step-down voltages from up to 100V. It has capable of driving dual N-channel MOSFET switches.

The MP9931 Adaptive Constant-On-Time (COT) control architecture provides fast transient response and eases loop stabilization. The DC auto tune loop provides good load and line regulation.

PSM Mode and USM Mode enables non-synchronous operation to optimize light load efficiency.

The operating frequency of MP9931 can be programmed by an external resistor or synchronized to an external clock for noise-sensitive applications.

Fault protections are available including a precision input over voltage protection (OVP), output over current protection (OCP), and thermal shutdown.

The MP9931 is available in a QFN-23(4.0mmx4.0mm) package.

FEATURES

Basic Function

- Lossless $R_{DS\ (on)}$ or shunt current sense
- COT Control offers Fast Load Transient Response
- 7V-to-100V Input Voltage Range
- Output adjusts from 0.8V to 80V
- 450μA Quiescent Current
- 4μA EN Shutdown Current
- 60ns Min-on-time
- Low Dropout Operation: max duty up to 99%
- USM/PSM/FCCM Selectable by Mode Pin
- Selectable Frequency by FREQ Resistor: 100kHz -1000kHz
- Power Good Indicator
- Ramp selectable by RAMP pin
- Selectable current limit by ILIM Resistor
- V_{DRV} Power from V_{OUT} when V_{OUT}>8.4V
- External V_{DRV}: bias V_{DRV} with external voltage source which is higher than internal V_{DRV}

Drive Ability

- 10V N-Channel MOS Gate Driver with 4.2A Source and 5.2A Sink Capability

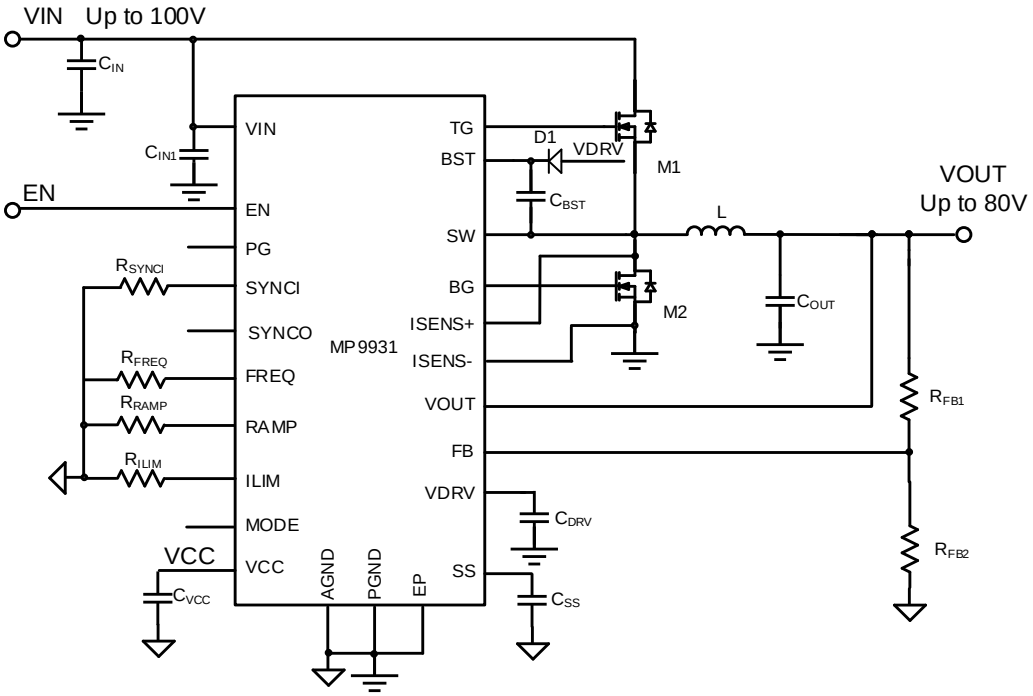
SYNCI/SYNCO

- SYNCI with external clock
- 180º Out-of-Phase SYNCO

APPLICATIONS

- Energy Storage System
- USB PD Charger
- POE System Power Supply
- Industrial Power Supplies
- E-bike Auxiliary Power Supplies
- General-Purpose Power Supplies

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP9931GR	QFN-23 (4mmx4mm)	*See Below*	*1*

* For Tape & Reel, add suffix -Z (e.g. MP9931GR-Z)

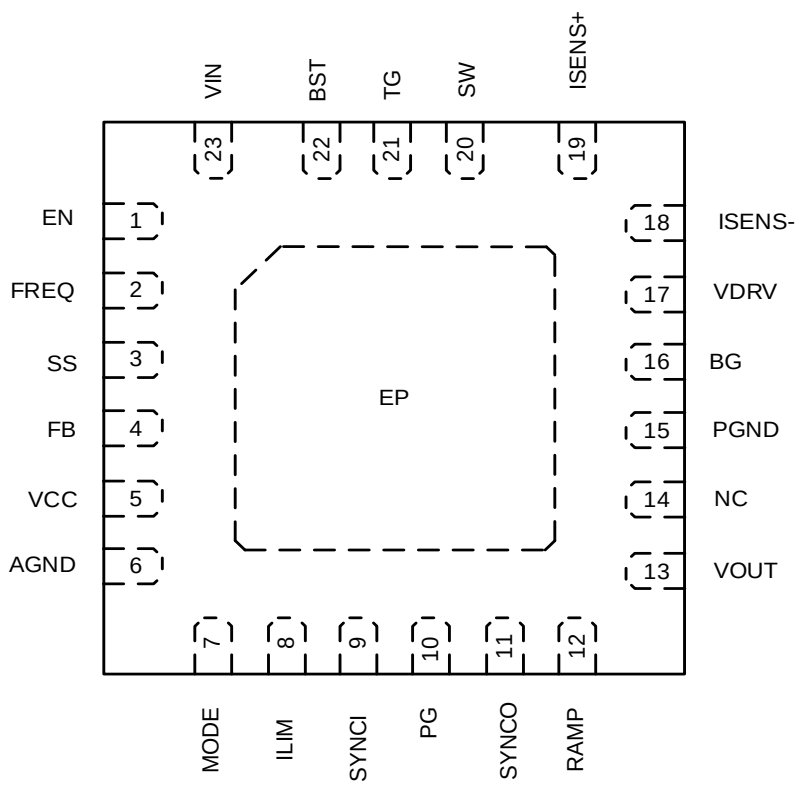
TOP MARKING

MPSYWW
MP9931
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP9931: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-23 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable control pin.** When EN is pull low, the controller is in the shutdown mode with all functions disabled. When EN voltage is pull high to above 1.2 V, the SS voltage can ramp up and pulse-width modulated gate-drive signals are delivered to the TG and BG pins.
2	FREQ	**Switching frequency select.** Connect a resistor between FREQ and AGND to set the switching frequency. It cannot be adjusted on-line, suggest Vin/EN off then on again after FREQ pin setup is changed. 1% tolerance resistor is recommended for it's good accuracy. **FREQ pin** / **Switch Frequency** GND / 100kHz 20kΩ to GND / 150kHz 45.3kΩ to GND / 200kHz 80.6kΩ to GND / 250kHz 124kΩ to GND / 300kHz 180kΩ to GND / 400kHz 243kΩ to GND / 600kHz VCC / 1MHz
3	SS	**Soft-start control input.** This pin is used to program the soft-start period with an external capacitor between SS to AGND.
4	FB	**Output feedback.** An external resistor divider from the output to AGND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
5	VCC	**Internal 5V LDO output.** The most control circuits are powered from the VCC voltage. Decouple VCC with a ceramic capacitor at least 1μF placed as close to it as possible. 2.2uF X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	AGND	**Analog ground.** Select AGND as the control circuit reference point.
7	MODE	**Operation mode selection**. Pull MODE to VCC to operate in forced CCM mode. Float MODE to operate in PSM mode with ultrasonic mode (USM) at light load. Connect MODE to ground to operate in PSM mode without USM. Mode can be adjusted on-line.
8	ILIM	**Current limit adjust.** Connect a resistor between ILIM and GND to set the valley current limit. Current limit can be adjusted on-line. **ILIM pin** / **Valley Current Limit** / **Negative Current limit** GND / 25mV / 25mV 51kΩ to GND / 50mV / 25mV 120kΩ to GND / 75mV / 50mV VCC / 100mV / 50mV
9	SYNCI	**Sync signal input.** If an external sync clock is applied to this pin, internal clock will follow the sync frequency.
10	PG	**Power good output.** The output of this pin is open drain.

PIN FUNCTIONS *(continued)*

<table>
<tr><th>Pin #</th><th>Name</th><th>Description</th></tr>
<tr><td>11</td><td>SYNCO</td><td>Sync signal output. Outputs a clock which are 180° out-of-phase with internal Oscillator Clock or external Synchronize Clock when part works in CCM mode, DCM or USM. SYNCO outputs 0V in other cases (Sleep mode, Fault protections, etc.).</td></tr>
<tr><td>12</td><td>RAMP</td><td>Internal ramp selection. Connect a resistor between RAMP and AGND to set the internal ramp. A large ramp will make the chip work more stable, while a small ramp will bring better load transient response performance. RAMP cannot be adjusted on-line.
<table>
<tr><th>RAMP pin</th><th>RAMP SET</th></tr>
<tr><td>GND</td><td>X</td></tr>
<tr><td>51kΩ to GND</td><td>0.5X</td></tr>
<tr><td>120KΩ to GND</td><td>0.33X</td></tr>
<tr><td>180KΩ to GND</td><td>2X</td></tr>
<tr><td>VCC</td><td>4X</td></tr>
</table></td></tr>
<tr><td>13</td><td>VOUT</td><td>VOUT sense and bias supply. VOUT will supply VDRV and internal VCC regulator via this pin. It will disable the power from VIN as long as VOUT is higher than 8.4V. VOUT pin must be connected to output for internal ton calculation.</td></tr>
<tr><td>14</td><td>NC</td><td>Not connected. NC pin need to be floating.</td></tr>
<tr><td>15</td><td>PGND</td><td>System ground. Power ground reference for the internal low side switch driver and the VDRV regulator circuit. Connect this pin directly to the negative terminal of the VDRV decoupling capacitor.</td></tr>
<tr><td>16</td><td>BG</td><td>Bottom gate driver. Connect this pin to the gate of the synchronous N-channel MOSFET.</td></tr>
<tr><td>17</td><td>VDRV</td><td>Decoupling Input Pin for Driver Power supply. Decouple with a minimum 4.7µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended.</td></tr>
<tr><td>18</td><td>ISENS-</td><td>Negative input for the current sense. ISENS+ and ISENS- should be layout with differential pair lines.</td></tr>
<tr><td>19</td><td>ISENS+</td><td>Positive input for the current sense. ISENS+ can be connected to either the drain of the low-side MOSFET for lossless R_{DS}(on) sensing or a current sense resistor connected to the source of the low-side MOSFET for accurate current limit and ZCD(zero current detection). ISENS+ and ISENS- should be layout with differential pair lines.</td></tr>
<tr><td>20</td><td>SW</td><td>Switch node. Reference for the V_{BST} supply and high current returns for bootstrapped switch.</td></tr>
<tr><td>21</td><td>TG</td><td>Top gate drive. The TG pin drives the gate of the top N-channel MOSFET. The TG driver draws power from the BST capacitor and returns to SW pin, providing a true floating drive to the top N-channel MOSFET.</td></tr>
<tr><td>22</td><td>BST</td><td>Bootstrap. This pin is the positive power supply for the internal floating high side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.</td></tr>
<tr><td>23</td><td>VIN</td><td>Input voltage. Operates from a 7V to 100V input. Ceramic capacitor is needed to prevent large voltage spikes from appearing at the input.</td></tr>
<tr><td>EP</td><td>-</td><td>Exposed Pad. Connect it to ground.</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) ..... -0.3V to 110V
SW .....-0.3V (-5V for <20ns) to 110V
ISENS+.....-0.3V (-5V for <20ns) to 110V
BST - SW..... -0.3V to 14V
V_{DRV} ..... -0.3V to 14V
V_{OUT} .....-0.3V (-5V for <10µs) to 85V
TG - SW.....0.3V to V_{BST} + 0.3V
BG ..... -0.3V to V_{DRV} + 0.3V
EN .....-0.3V to + 6.5V(<100µA when >6V)
All other pins..... -0.3V to +6.5V
Continuous power dissipation (TA = +25°C) **(2)**
QFN-23 (4.0mmx4.0mm) ..... TBDW
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... –65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM)..... ±750V

Recommended Operating Conditions (3)

Input voltage VIN ..... 7V to 100V
Output voltage VOUT..... 0.8V to 80V
External bias V_{DRV}..... 10.5V to 12V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-23(4.0mmx4.0mm)

JESD51-7 (4) ..... TBD ... TBD °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

VIN= 48V, EN = 2V, T_J = -40°C to 125°C (5), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDRV Regulator						
VDRV UVLO rising threshold	$V_{DRV\_UV\_R}$			6.5		V
VDRV UVLO hysteresis	$V_{DRV\_UV\_HYS}$			600		mV
VDRV Voltage	V_{DRV}	I_{DRV} = 0mA		10		V
VDRV Regulation		I_{DRV} = 20mA		2		%
VOUT rising threshold, override V_{IN} supply VDRV	$Vo\_V_{DRV\_R}$			8.4		V
VOUT falling threshold, V_{IN} supply VDRV	$Vo\_V_{DRV\_F}$			7.4		V
VCC Regulator						
VCC Voltage	VCC	I_{CC}=0mA		5		V
VCC Regulation		I_{CC}=20mA		2		%
Supply Current						
VIN quiescent current	I_Q	V_{FB}=0.88V, V_{OUT}=0V, PSM		450		µA
		V_{FB}=0.88V,V_{OUT}=12V, PSM		50		µA
VIN shutdown current	I_{SHDN}	V_{EN} = 0V		4		µA
VIN OVP						
VIN over voltage rising threshold	$V_{IN\_OV\_R}$			105		V
VIN over voltage hysteresis	$V_{IN\_OV\_HYS}$			2		V
Enable Control						
EN UVLO rising threshold	$V_{EN\_UVLO\_R}$			1.2		V
EN UVLO hysteresis	$V_{EN\_UVLO\_HYS}$			200		mV
EN input current	I_{EN}	V_{EN}=2V		0	1	µA
Feedback (FB)						
FB Reference Voltage	V_{REF}	T_J=25°C	0.792	0.800	0.808	V
		T_J=-40°C to 125°C	0.788	0.800	0.812	V
Feedback current	I_{FB}	V_{FB} = 1.05V		-50		nA
FB under voltage threshold	V_{FB_UV}			30%		V_{REF}
FB under voltage hysteresis	$V_{FB\_UV\_HYS}$			20%		V_{REF}
FB over voltage threshold	V_{FB_OV}			108%		V_{REF}
FB over voltage recover hysteresis	$V_{FB\_OV\_HYS}$			3%		V_{REF}
Soft start						
SS capacitor charging current	I_{SS}	Vss=0V		4		µA

ELECTRICAL CHARACTERISTICS *(continued)*

VIN= 48V, EN = 2V, T_J = -40°C to 125°C (5), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Switching Frequency						
Switching Frequency	f_{SW}	Connect FREQ to GND		100		kHz
		R_{FREQ}=20kΩ		150		kHz
		R_{FREQ}=45.3kΩ		200		kHz
		R_{FREQ}=80.6kΩ		250		kHz
		R_{FREQ}=124kΩ		300		kHz
		R_{FREQ}=180kΩ		400		kHz
		R_{FREQ}=243kΩ		600		kHz
		Connect FREQ to VCC		1000		kHz
Min TG on time	$t_{TG\_MIN\_ON}$			60		ns
Min BG on time	$t_{BG\_MIN\_ON}$			200		ns
Max TG on time	$t_{TG\_MAX\_ON}$	V_{IN}-V_{OUT}<3V		20		µs
		3V<V_{IN}-V_{OUT}<6V		10		µs
Max Duty Cycle	D_{MAX}			99.0		%
Minimum switching frequency in USM	f_{SW_USM}	USM	20			kHz
Dead Time						
Dead time from TG falling to BG rising	$t_{DT\_BG\_R}$	trigger point 5V to 5V		35		ns
Dead time from BG falling to TG rising	$t_{DT\ BG\_F}$	trigger point 5V to 5V		35		ns
SYNCHRONICATION INPUT AND OUTPUT						
SYNCI external clock frequency range	f_{SYNCI}		80%		120%	Fsw
SYNCI voltage rising threshold	V_{SYNC_R}		2			V
SYNCI voltage falling threshold	V_{SYNC_F}				0.8	V
Minimum SYNCI pulse-width (6)	t_{SYNC_MIN}		50			ns
SYNCO output HIGH logic	V_{SYNCO_H}	ISYNCO = -1mA source	4.7			V
SYNCO output LOW logic	V_{SYNCO_L}	ISYNCO = 1mA sink			0.3	V
SYNCO pulse duty cycle	D_{SYNCO}			50%		
Phase from PLL clock rising to SYNCO rising (6)	P_{DLY}	50% to 50%		180°		
BST Power						
BST Forward Voltage	V_{DROP_BST}	VDRV to BST, BST pin sourcing 20mA		0	1	V
BST to SW quiescent current, not switching	I_{BST_LKG}	No switching, Vsw=48V, Vbst=58V		27		µA
Mode Selection						
PSM mode with USM	V_{USM}				0.4	V
PSM mode without USM	V_{PSM}		1		1.6	V
FCCM mode	V_{FCCM}		2.5			V
Power Good (PG)						
Power Good rising threshold	PG_{TH_R}	FB rising		95%		V_{REF}
		FB falling		105%		V_{REF}
Power Good falling threshold	PG_{TH_F}	FB falling		90%		V_{REF}
		FB rising		108%		V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

VIN= 48V, EN = 2V, T_J = -40°C to 125°C(5), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good delay	t_{PG_DLY}	Low to high		300		µs
		High to low		150		µs
Power Good sink current capability	V_{PG}	IC enabled, Sink 4mA			0.4	V
Power Good leakage current	I_{PG_LKG}	PG High state, VPG=5V		1.5		µA
Gate Drivers						
TG pull-up resistor (7)	R_{TG_UP}	V_{BST}-V_{SW}=10V, TG high state, I_{TG}=-100mA		1.2		Ω
TG pull-down resistor (7)	R_{TG_DN}	V_{BST}-V_{SW}=10V, TG low state, I_{TG}=100mA		0.7		Ω
BG pull-up resistor (7)	R_{BG_UP}	V_{DRV}=10V, BG high state, I_{BG}=-100mA		1.2		Ω
BG pull-down resistor (7)	R_{BG_DN}	V_{DRV}=10V, BG low state, I_{BG}=100mA		0.7		Ω
TG, BG source current (7)	I_{OH}	V_{BST}-V_{SW}=10V, V_{DRV}=10V, TG=SW, BG=PGND Not test in ATE		4.2		A
TG, BG sink current (7)	I_{OL}	V_{BST}-V_{SW}=10V, V_{DRV}=10V, TG=BST, BG=VDRV		5.2		A
Over Current Protection						
Valley current limit voltage	V_{VAL_LIMIT}	ILIM connect to GND		25		mV
		R_{ILIM} = 51kΩ		50		mV
		R_{ILIM} = 120kΩ		75		mV
		ILIM connect to VCC		100		mV
Negative Current Limit						
Negative current limit voltage	V_{NCL_LIMIT}	ILIM connect to GND		25		mV
		R_{ILIM} = 51kΩ		25		mV
		R_{ILIM} = 120kΩ		50		mV
		ILIM connect to VCC		50		mV
ZCD						
ZCD detect voltage	V_{ZCD}			1		mV
Current temperature coefficient						
Current temperature coefficient (7)	TC	R_{DS_ON} mode		4500		ppm/℃
		R_{SENSE} mode		0		ppm/℃
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		℃
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		℃

Note:

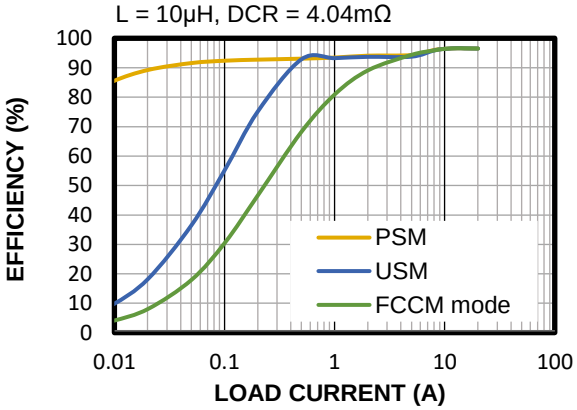
5) Not tested in production. Guaranteed by over-temperature correlation.
6) Not tested in production. Derived by design.
7) Not tested in production. Derived by sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, Freq = 100kHz, L=10μH, EN=2V, PSM, T_A = +25°C, unless otherwise noted.

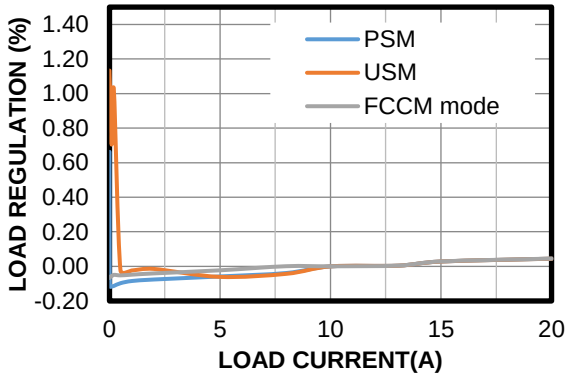
Efficiency vs. Load Current

L = 10μH, DCR = 4.04mΩ



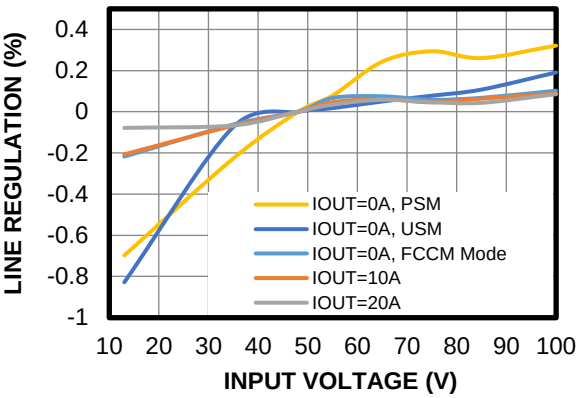
Load Regulation - BUCK

L = 10μH

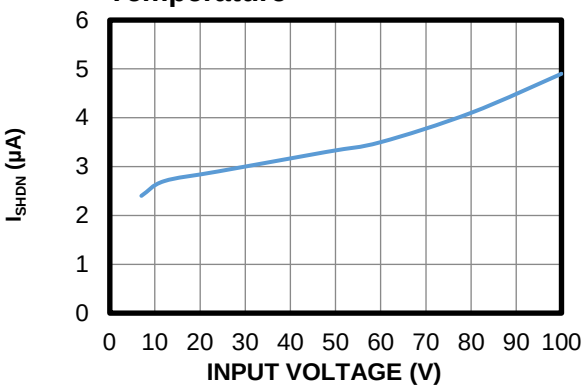


Line Regulation

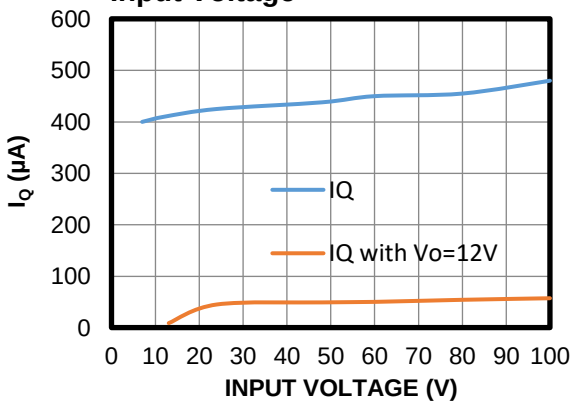
L = 10μH



ShutdownCurrentvs. Temperature



Quiescent Supply Current vs. Input Voltage

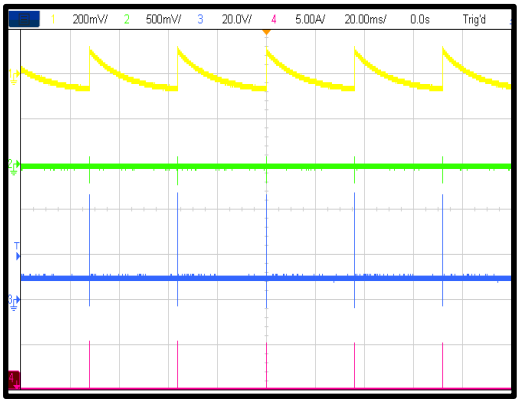


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

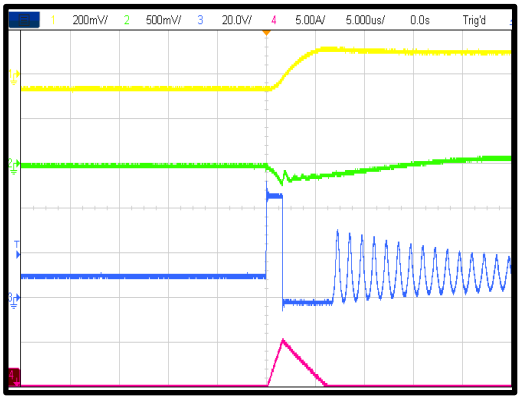
Steady State

I_{OUT} = 0A, PSM



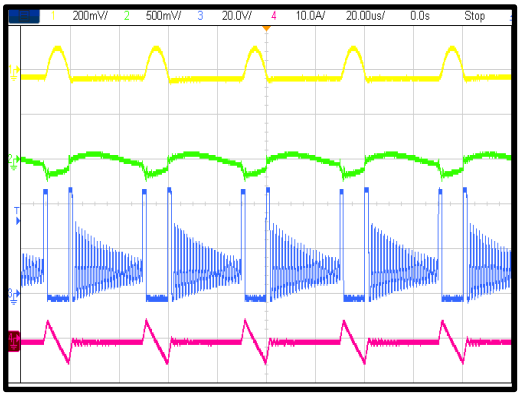
Steady State

I_{OUT} = 0A, PSM



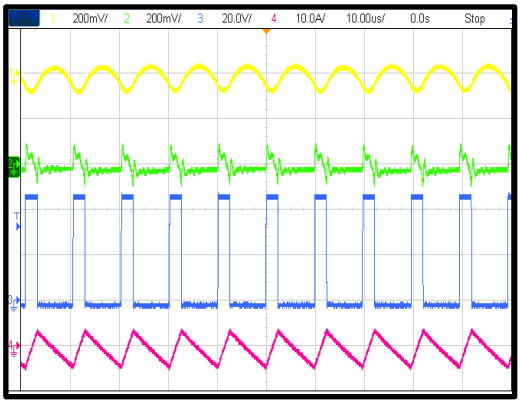
Steady State

I_{OUT} = 0A, USM



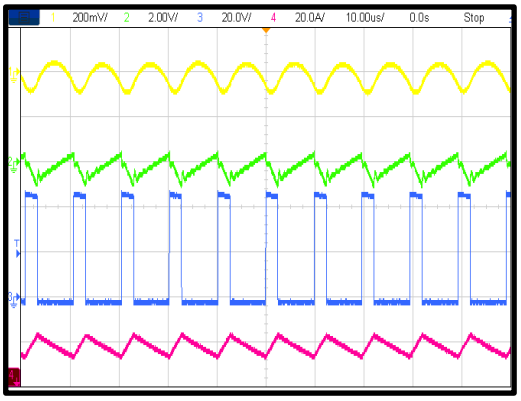
Steady State

I_{OUT} = 0A, FCCM Mode



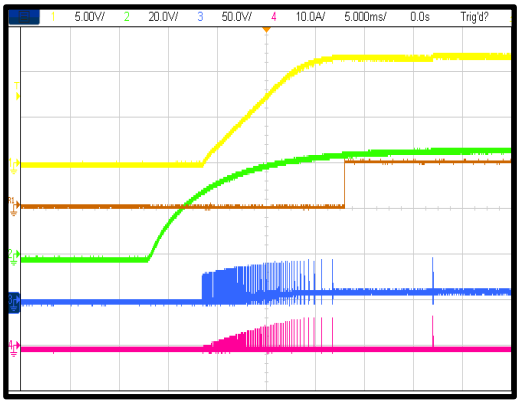
Steady State

I_{OUT} = 20A



Start-Up through VIN

I_{OUT} = 0A, PSM

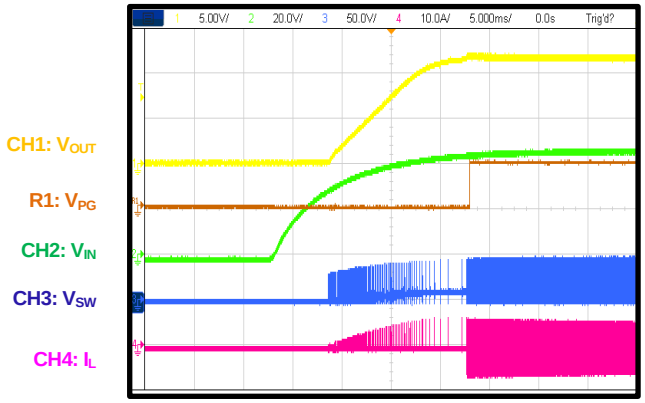


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

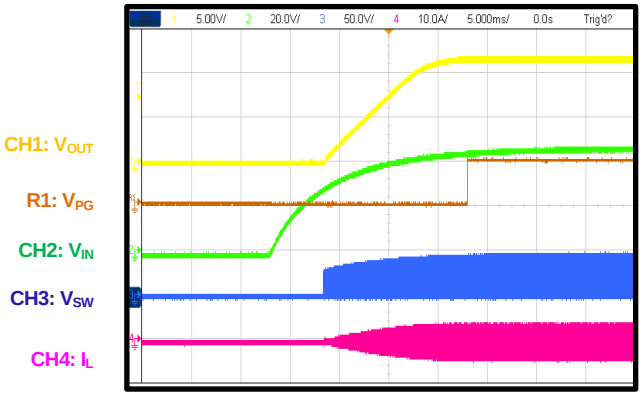
Start-Up through VIN

I_{OUT} = 0A, USM



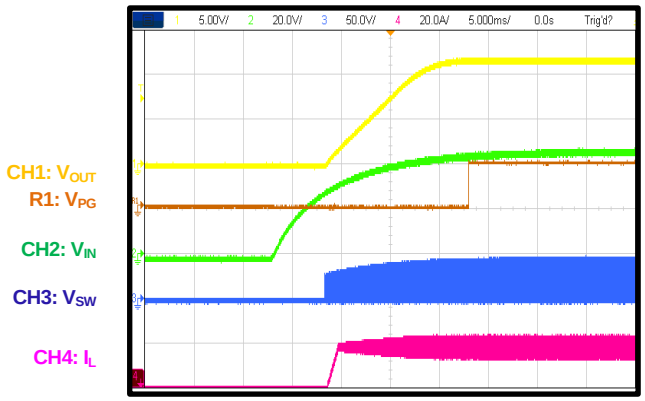
Start-Up through VIN

I_{OUT} = 0A, FCCM Mode



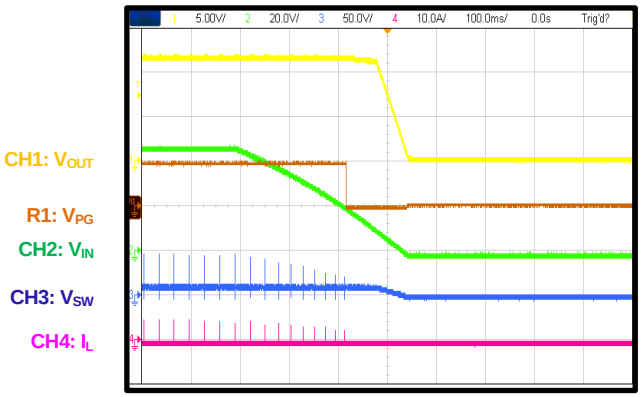
Start-Up through VIN

I_{OUT} = 20A



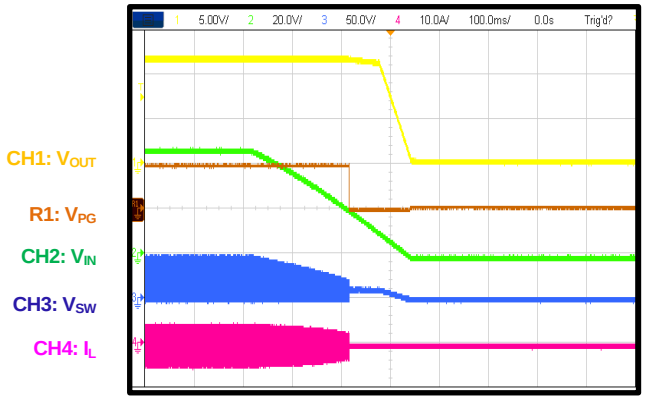
Shutdown through VIN

I_{OUT} = 0A, PSM



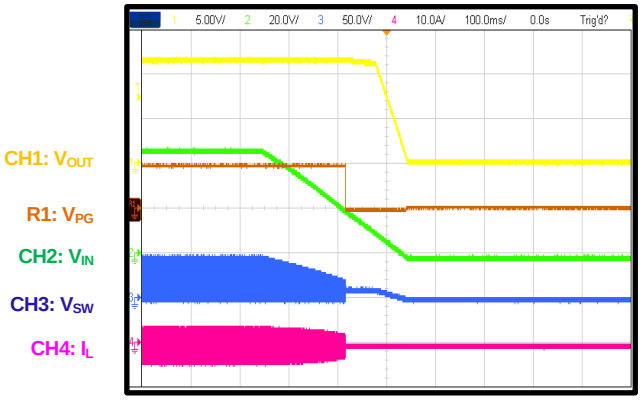
Shutdown through VIN

I_{OUT} = 0A, USM



Shutdown through VIN

I_{OUT} = 0A, FCCM Mode

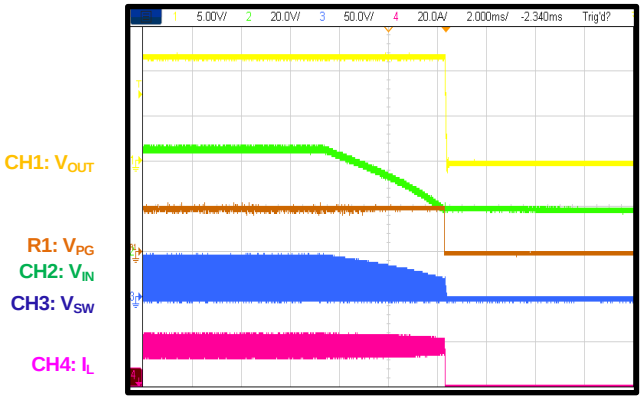


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

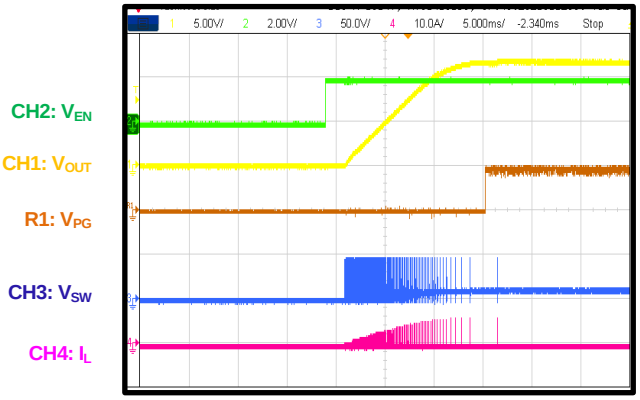
Shutdown through VIN

I_{OUT} = 20A



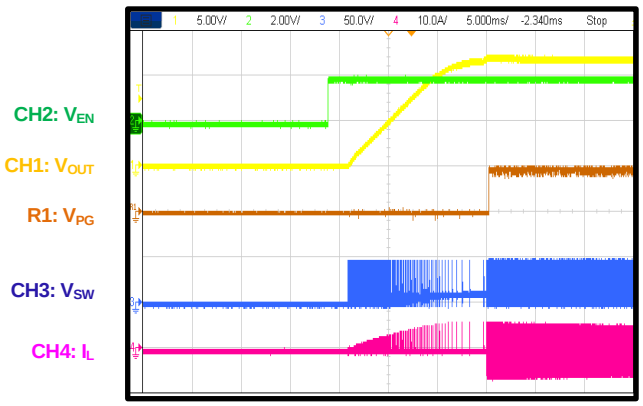
Start-Up through EN

I_{OUT} = 0A, PSM



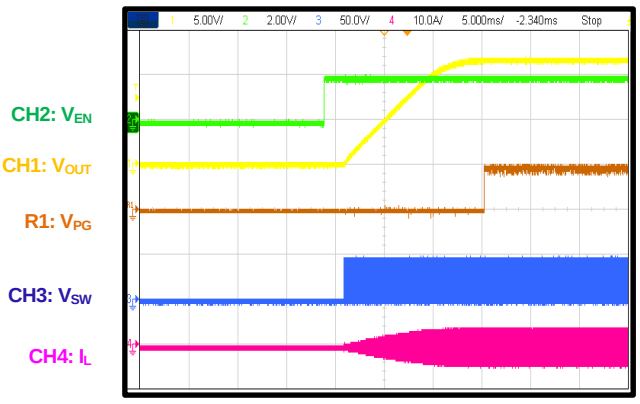
Start-Up through EN

I_{OUT} = 0A, USM



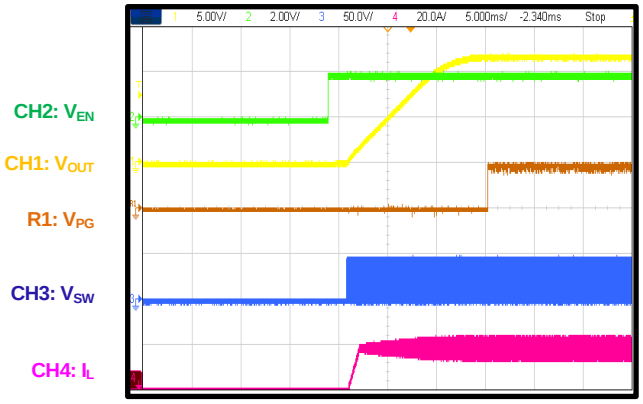
Start-Up through EN

I_{OUT} = 0A, FCCM Mode



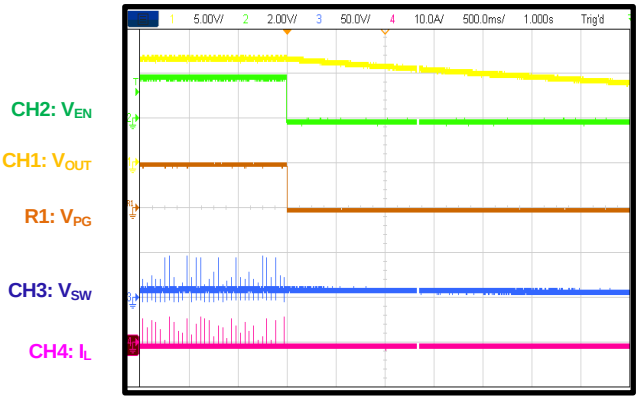
Start-Up through EN

I_{OUT} = 20A



Shutdown through EN

I_{OUT} = 0A, PSM

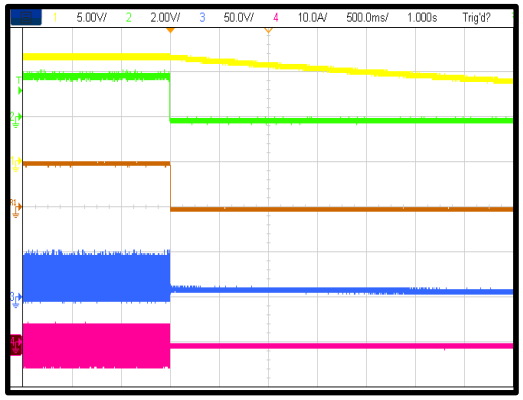


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

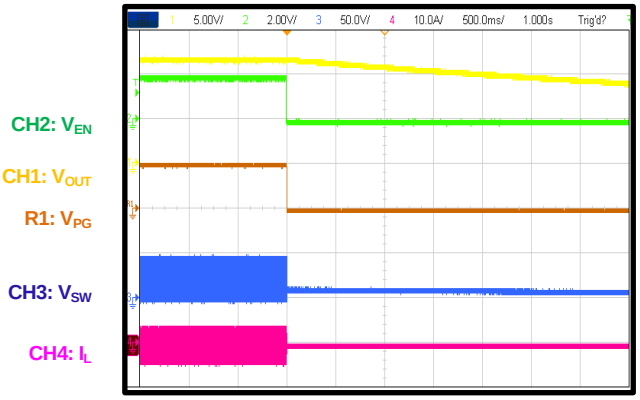
Shutdown through EN

I_{OUT} = 0A, USM



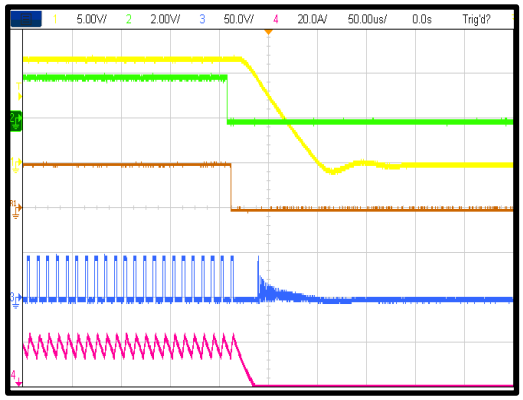
Shutdown through EN

I_{OUT} = 0A, FCCM Mode



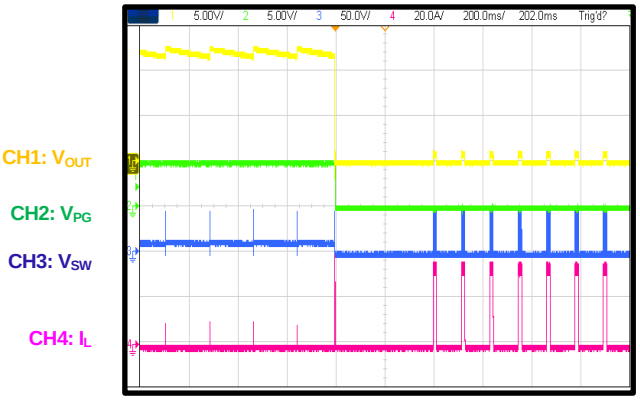
Shutdown through EN

I_{OUT} = 20A



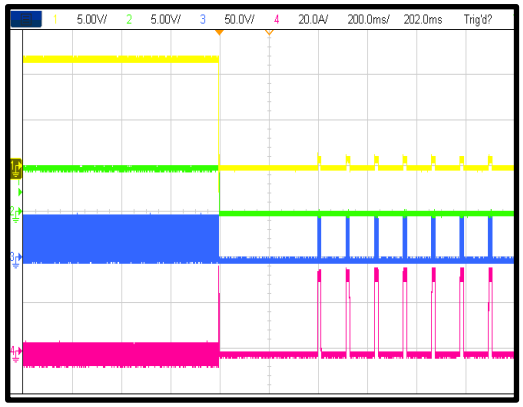
SCP Entry

I_{OUT} = 0A, PSM



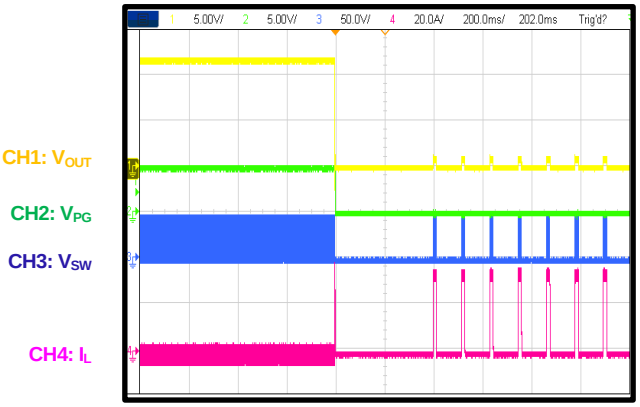
SCP Entry

I_{OUT} = 0A, USM



SCP Entry

I_{OUT} = 0A, FCCM Mode

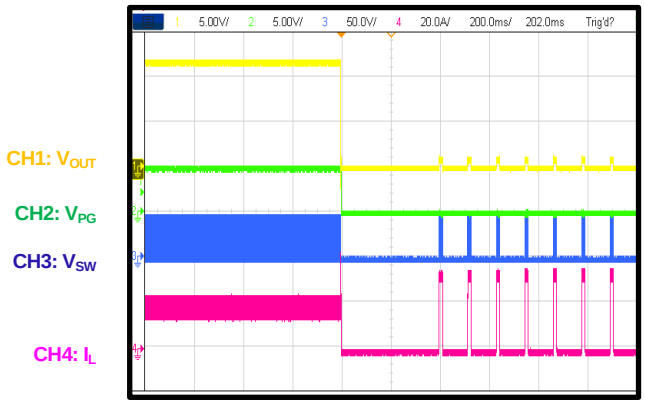


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

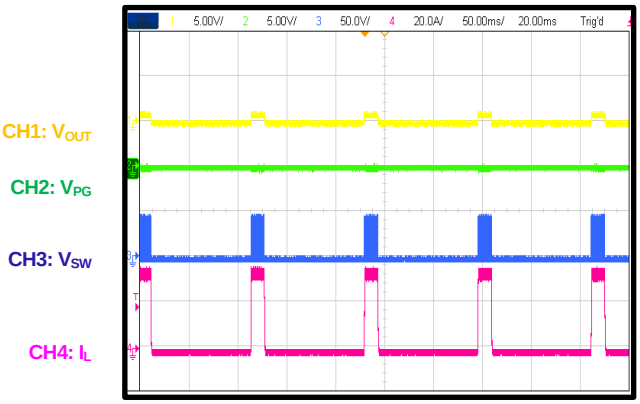
SCP Entry

I_{OUT} = 20A



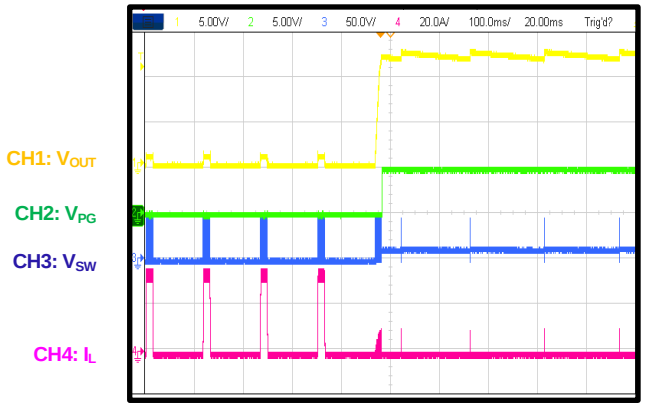
SCP Steady State

V_{OUT} short to GND



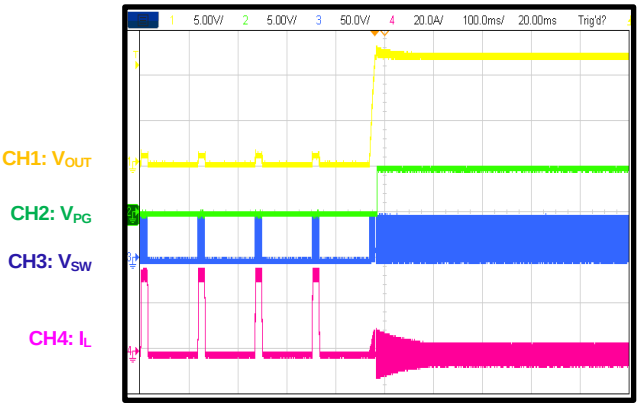
SCP Recovery

I_{OUT} = 0A, PSM



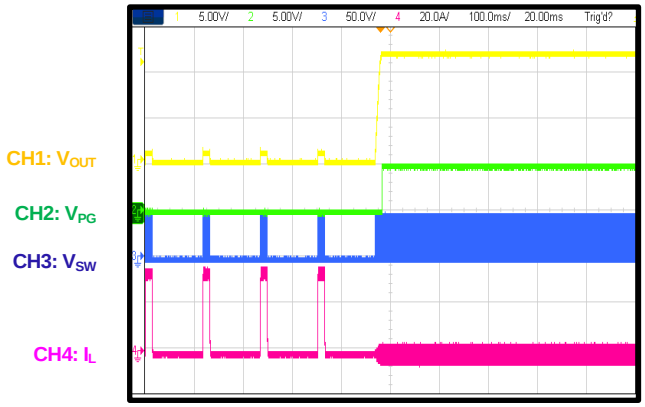
SCP Recovery

I_{OUT} = 0A, USM



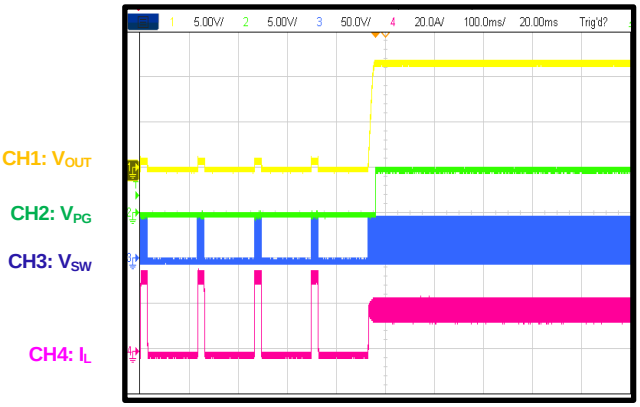
SCP Recovery

I_{OUT} = 0A, FCCM Mode



SCP Recovery

I_{OUT} = 20A

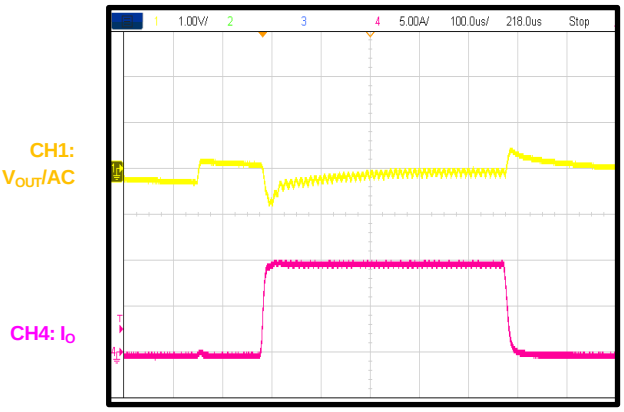


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 27. V_{IN} = 48V, V_{OUT} = 12V, freq=100kHz, L=10uH, PSM, T_A = 25°C, unless otherwise noted.

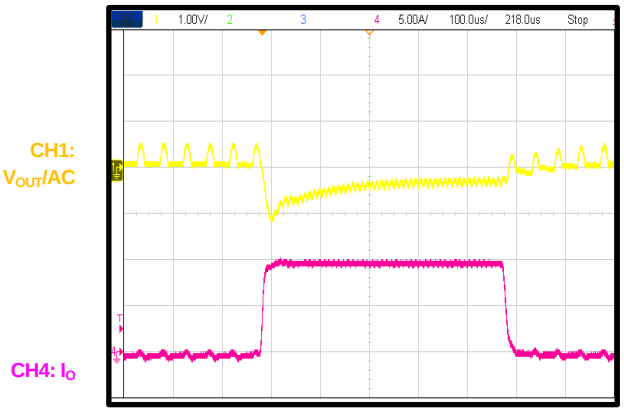
Load Transient

I_{OUT} = 0A to 10A, PSM, slew rate 1A/µs



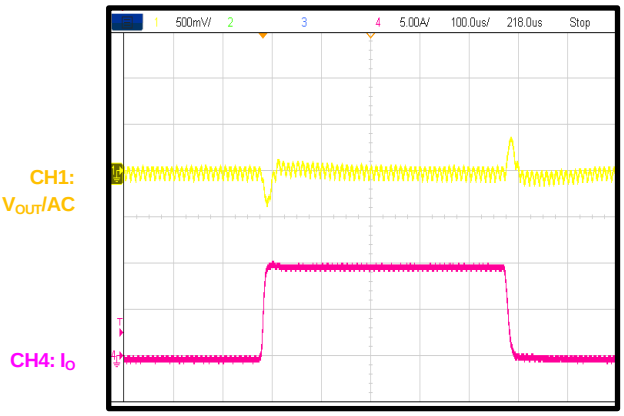
Load Transient

I_{OUT} = 0A to 10A, USM, slew rate 1A/µs



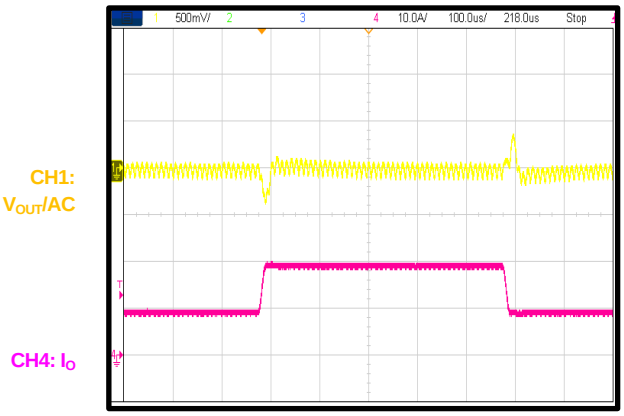
Load Transient

I_{OUT} = 0A to 10A, FCCM Mode, slew rate 1A/µs



Load Transient

I_{OUT} = 10A to 20A, slew rate 1A/µs



FUNCTIONAL BLOCK DIAGRAM

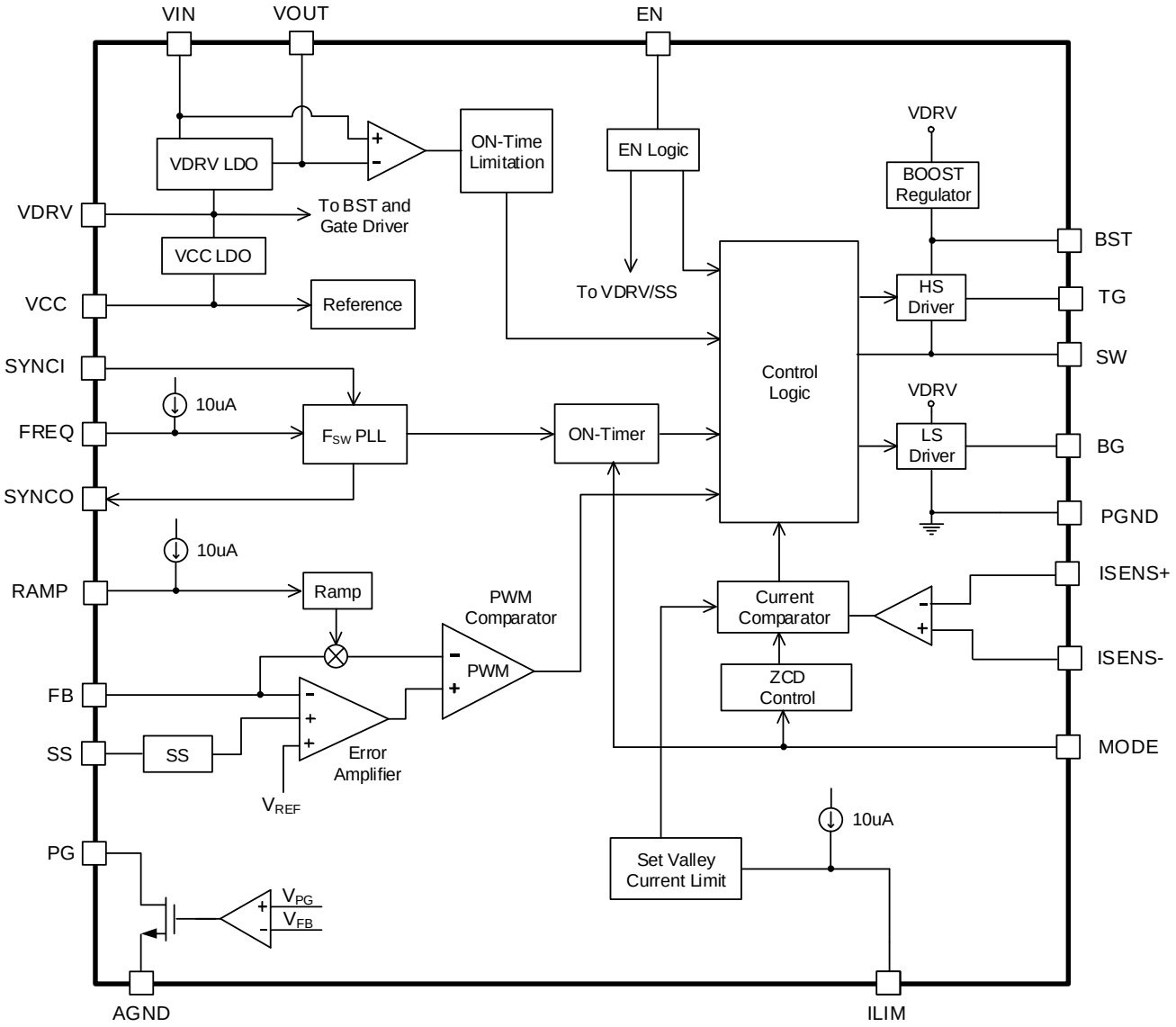


Figure 1: Block Diagram

OPERATION

Overview

The MP9931 is a high-performance, step down, synchronous converter controller IC with a wide input range. It implements COT control mode, switching frequency programmable control architecture to regulate the output voltage with external N-channel MOSFET switches.

Adaptive Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto tune loop provides good load and line regulation.

Under normal load condition, the controller operates in full PWM mode. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by the output voltage and input voltage to make the switching frequency fairly constant over input voltage range.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

Heavy-Load Operation

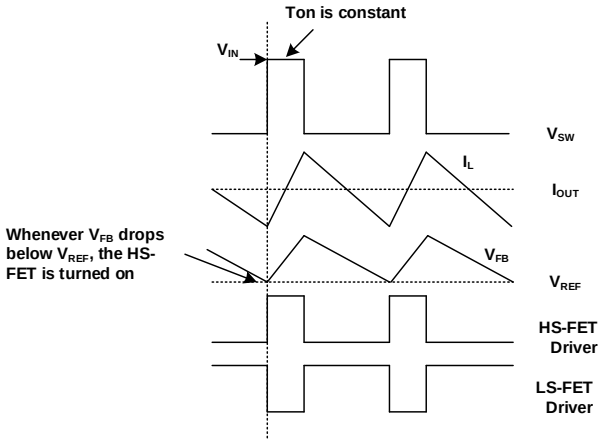


Figure 2: Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 2. When V_{FB} is below V_{REF}, HS-MOSFET is turned on for a fixed interval. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until next period.

There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To prevent shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

In CCM mode operation, the switching frequency is fairly constant and it is also called PWM mode.

In light load condition, MP9931 can be set in different MODE, refer to next section for detail.

Operation Mode

MP9931 works with fix frequency in heavy load condition. When load current decreases, MP9931 can work in forced continuous conduction mode (FCCM), pulse skip mode (PSM), or Ultrasonic Mode (USM) based on MODE pin setting. Refer to Table 1 for MODE pin setting. The operation mode can be change on-line.

Table 1: MODE Setting

MODE pin	Light Load Mode
GND	PSM without USM
FLOAT	PSM with USM
VCC	FCCM mode

Pulse-Skip Mode (PSM)

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

The light load operation is shown in Figure 3. When V_{FB} is below V_{REF}, HS-MOSFET is turned on for a fixed interval. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. Both the BG and TG will be pull LOW whenever the inductor current reaches zero. At light load or no load condition, the output drops very slowly and the MP9931 reduces the switching frequency naturally. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-MOSFET is not turned ON as frequently as at heavy load condition. This is also called Pulse-

Skip Mode (PSM).

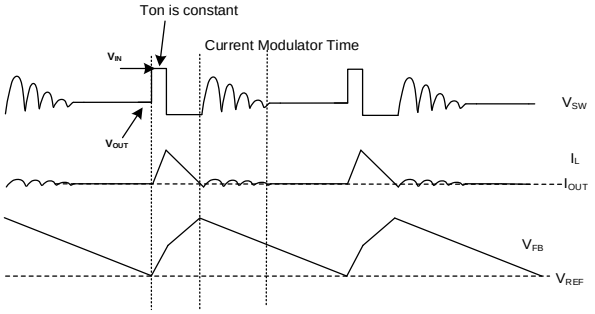


Figure 3: Light Load Operation

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-MOSFET is turned ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as equation 1:

$$I_{OUT\_Critical}=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L\times F_{SW}\times V_{IN}} \quad (1)$$

It turns into CCM mode once the output current exceeds the critical level. After that, the switching frequency fairly constant over the output current range.

Forced Continuous Conduction Mode (FCCM)

When the MP9931 sets in FCCM mode, if load is light, low-side FET doesn't turn off when inductor current touch ZCD. The inductor current goes negatively flowing from Vout to GND when LS-FET is on. This forces the inductor current to work in continuous conduction mode (CCM) with a fixed frequency, producing a lower V_{OUT} ripple than in PSM mode.

The FCCM mode operation is shown in Figure 4. HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until next period.

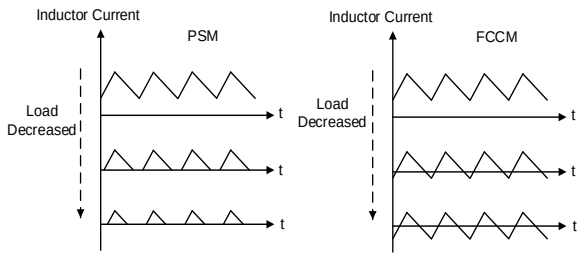


Figure 4: PSM Mode and Forced CCM Mode

Ultrasonic Mode (USM)

Ultrasonic mode (USM) is used to keep the switching frequency above audible frequency areas during light-load conditions. Once part goes into light load, Ton shrinks and ZCD drops to avoid IC switching frequency go below 20kHz.

Low Dropout Operation

Low dropout mode is designed to improve dropout when VIN is close to VOUT by further increase HS-FET on time after min-off-time is reached. At low dropout mode, the MP9931 is designed to operate at Ton extended mode as long as the voltage across BST - SW is greater than BST under-voltage lockout (UVLO). When the voltage from BST to SW drops below BST UVLO, the BST UVLO circuit turns off the high-side MOSFET (HS-FET), After the BST capacitor voltage is re-charged above BST UVLO, the HS-FET turns on again to regulate the output. Since the BST regulation voltage is far greater than BST UVLO, the HS-FET can remain on for a long time without requirement to refresh the BST capacitor, thus increasing the effective duty cycle of the switching regulator. The low dropout operation makes the MP9931 suitable for application where VIN is close with VOUT. The max extend on time is limited by VIN-VOUT, when 3V<VIN-VOUT<6V, it's 10μs, when VIN-VOUT <3V, it's 20μs.When ss is pulled up to vcc the low drop out mode is disabled.

Constant Current (CC) Mode

MP9931 provide a CC mode operation for battery charge. Pull up SS to VCC via 10kΩ to enable CC Mode. At this condition, output UV protection and low drop out mode is disabled. FB pull down to GND or divide from VCC to set FB to lower than 0.8V are both ok for this condition. Figure 5 shows SS and FB typical connection for CC mode application.

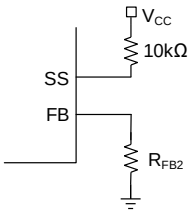


Figure 5: CC Mode

The CC average current is set by valley current limit and inductor current ripple, can be calculate by equation 2 as below.

$$I_{CC} = \frac{V_{ILIM}}{R_S} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Recommend use shunt resistor current sensing for CC mode to achieve better accuracy at full temperature range.

Synchronization

MP9931 frequency (internal oscillator set by FREQ pin) can be synchronized to an external clock with range ±20% of programmed switching frequency through SYNCI pin. When add one clock signal to SYNCI pin, the internal clock rising edge is synchronized to the external clock rising edge.

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap capacitor (C_{BST}), which is normally refreshed when the high-side MOSFET (HS-FET) turns off. This floating driver has its own UVLO protection.

VDRV Power Supply and VCC Regulator

Both high-side BST and low-side MOSFET drivers are powered from V_{DRV}, usually a 4.7μF ceramic capacitor is needed at V_{DRV} Pin to prevent large voltage spikes.

An internal low dropout linear regulator supplies VCC power from V_{DRV}, most of the internal circuit are powered from the VCC regulator, a 2.2μF ceramic capacitor is recommended from VCC to AGND. All VIN, V_{DRV} and VCC have their own UVLO circuit to protect the chip from operating at an insufficient supply voltage.

When VIN power is supplied and EN is high, MP9931 regulate V_{DRV} from VIN first. If V_{OUT} voltage >8.4V, MP9931 will slowly scale down the V_{DRV} and make it approximately equal to V_{OUT}, then, disable the VIN to V_{DRV} LDO1 and enable the V_{OUT} to V_{DRV} LDO2. When V_{OUT} drop below 7.4V, the source to V_{DRV} will be change back to VIN and V_{DRV} voltage will be scaled accordingly.

If 8.4V<V_{OUT}<10V, the V_{DRV} LDO2 is in low dropout mode and V_{DRV} is approximately equal to V_{OUT}. When VOUT is greater than 10V, VDRV is regulated to 10V, so that MP9931 can get higher efficiency for internal driver loss.

V_{DRV} can also be power from external voltage source.

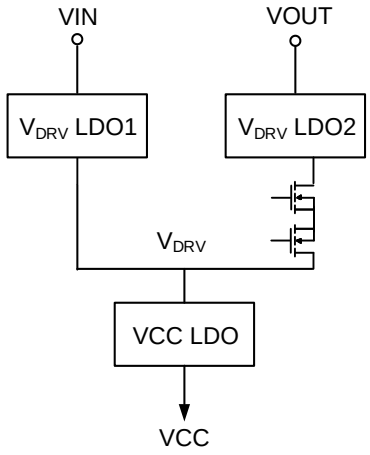


Figure 6: Internal LDO Structure

Enable (EN) and Programmable UVLO

EN pin enables and disables the MP9931. When applying a voltage lower than 0.4V, MP9931 is shutdown. After the voltage rise to the EN high threshold (1.2V typically), the MP9931 enables and starts switching operation. Switching operation is disabled when EN voltage falls below its falling threshold.

Tie EN to VIN through a resistor divider R_{EN_UP} and R_{EN_DOWN} to program the VIN start up threshold (see Figure 7).

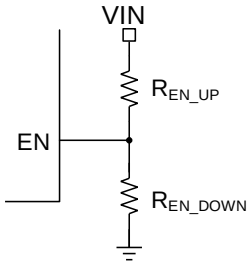


Figure 7: EN Divider Resistors

EN pin can be directly connect to VIN via a pull-up resistor limits the EN input current below 100μA, which prevents damage to the EN circuit internal.

For example, when connecting 100V to VIN, then the pull up resistor should be larger than 935kΩ.

R_{PULL_UP} ≥ (100V – 6.5V) / 100μA = 935kΩ.

Switching Frequency

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by

reducing MOSFET switching loss, but requires larger inductance and capacitance to maintain low output voltage ripple. The switching frequency of MP9931 can be set by the R_{FREQ} connected to FREQ and AGND pin as below table.

Table 2: Switching Frequency Selection

FREQ pin	Switching Frequency
0Ω	100kHz
20kΩ to GND	150kHz
45.3kΩ to GND	200kHz
80.6kΩ to GND	250kHz
124kΩ to GND	300kHz
180kΩ to GND	400kHz
243kΩ to GND	600kHz
VCC	1MHz

When EN is high and VCC rising above its UVLO, MP9931 starts work by source a current pulse to FREQ pin to detect FREQ setting. This detection set the switching frequency and latch the setting after MP9931 startup.

Current Sense

The MP9931 implements a lossless current sense scheme designed to limit the inductor current during an overload or short-circuit condition. Figure 8 portrays the current sense method using the on-state resistance of the low-side MOSFET. Meanwhile, Figure 9 shows an alternative implementation with current shunt resistor R_S. The MP9931 senses the inductor current during the PWM off-time.

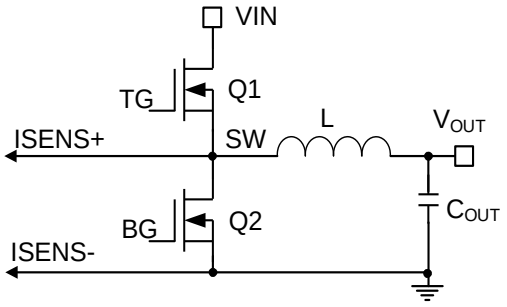


Figure 8: MOSFET $R_{DS\ (on)}$ Current Sensing

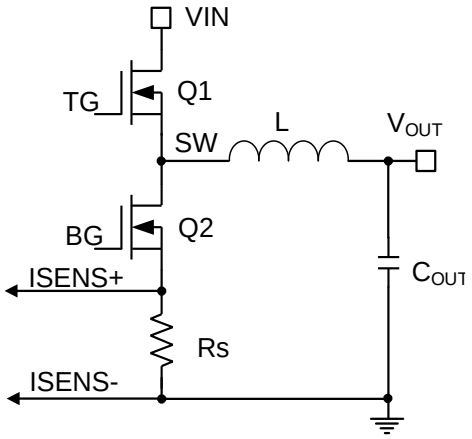


Figure 9: Shunt Resistor Current Sensing

The MP9931 has four fixed options for current limit setting as shown in table 3.

When use lossless current sense， MP9931 monitors the inductor current by on-state resistance of the low-side MOSFET. The current limit can be calculate by equation 3.

$$I_{ILIM} = \frac{V_{ILIM}}{R_{DS\_ON}} \quad (3)$$

When use shunt resistor current sensing， the current sense resistor R_S monitors the inductor current. Its value is chosen based on the current limit threshold. The relationship between the inductor valley current I_{ILIM} and R_S is:

$$I_{ILIM} = \frac{V_{ILIM}}{R_S} \quad (4)$$

The typical values for R_S are in the range of 2mΩ to 10mΩ.

Valley Current Limit set

The ILIM pin of the MP9931 sources a reference current that flows to external resistor R_{ILIM}, to program the current limit sense voltage. TG is not allowed to pull high when voltage of ISENS+ and ISENS- fall below the sense voltage limit set by ILIM pin.

Connect ILIM pin to AGND through resistor R_{ILIM} to program the current limit sense voltage between ISENS+ and ISENS- pin as below table.

Table 3: Valley Current Limit Threshold

ILIM pin	Valley Current Limit Threshold
GND	25mV
51kΩ to GND	50mV
120kΩ to GND	75mV
VCC	100mV

The MP9931 detects the appropriate mode at start-up and sets the temperature coefficient (TC) accordingly. MP9931 provide a TC of +4500 ppm/°C to generally track the R_{DS}(on) temperature variation of the low-side MOSFET. Conversely, MP9931 have no TC in R_{SENSE} mode. This controls the valley of inductor current during a steady state overload at the output.

Over-Current Protection (OCP)

The MP9931 has a hiccup, cycle-by-cycle, over-current limiting control. The MP9931 limited the voltage between ISENS+ and ISENS- pin for the valley current. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 30% of the V_{REF}). Once UV is triggered, the MP9931 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP9931 exits hiccup mode once the over-current condition is removed.

RAMP Set

The RAMP pin of the MP9931 can be used to select the internal ramp for stability. With different R_{RAMP} to GND, can set different ramp value. Below table 4 shows the relationship of ramp pin pull down resistor R_{RAMP} and internal R value for RAMP calculate.

Table 4: RAMP vs. Internal R

RAMP pin	RAMP	R (kΩ)
GND	1X	2077
51kΩ to GND	0.5X	4077
120kΩ to GND	0.33X	6077
180kΩ to GND	2X	1077
VCC	4X	577

RAMP can be calculate by equation 5 as below:

$$RAMP(mV) = K_{DIV} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \mathrm{R(k\Omega)}} \quad (5)$$

K_{DIV} is fixed to 0.44×10^4.

For example, select 1X ramp for 48V input, 12V output, RAMP is about 21mV.

Note: Larger RAMP set is better for stability, but transient performance will be worse at the same time.

Power Good Function

The MP9931 includes an open-drain power good output that indicates whether the regulator's output is within the range of its nominal value. When the output voltage is out of this range, the PG output is pulled to low. It should be pull up to a voltage source through a resistor (e.g., 100kΩ).

PG pin has self-driving capability, if MP9931 is off and PG pin is pulled up to another DC power source through a resistor, the PG pin can also be pulled low by self-driving circuit.
The relationship between the PG clamped voltage and the pull-up current is shown in Figure 10.

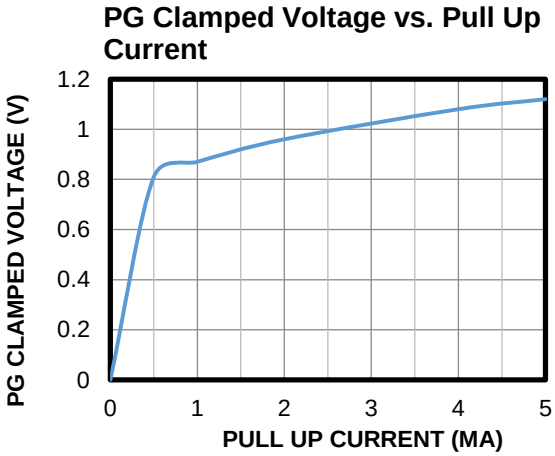


Figure 10: PG Clamped Voltage vs. Pull Up Current

Soft Start

The soft start (SS) is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage ramping up from 0V to VCC. When it is lower than the internal V_{REF}, SS

voltage overrides V_{REF}, so the error amplifier uses SS voltage as the reference. When SS voltage is higher than V_{REF}, V_{REF} regains control.

An external capacitor connected from SS to AGND is charged by an internal current source, producing a ramped voltage. The soft-start time (t_{SS}) is set by the external SS capacitor and can be calculated by equation 6 as below:

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times V_{REF}(V)}{I_{SS}(\mu\text{A})} \quad (6)$$

Where C_{SS} is the value of external SS capacitor, V_{REF} is the internal reference voltage, and I_{SS} is the SS charge current. Typical value of Iss is 4uA. SS will be reset when a protection happened except for output over voltage protection.

With Css=47nF, t_{SS} is about 9.4ms.

Pre-bias Startup

The MP9931 is designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, MP9931 won't switch until SS ramps up to the value reference to the V_{OUT} bias voltage. The BST voltage will be refreshed in this condition.

Output Over-Voltage Protection

MP9931 output voltage is monitored by FB voltage. If FB voltage is typically 108% of the reference, it'll trigger OVP. Once it triggers OVP, MP9931 will stop switching, MP9931 recover to normal loop control when V_{OUT} drops to 105% of regulation voltage.

Thermal Protection

The MP9931 has thermal protection by monitoring the IC temperature internally. This function prevents the chip from operating at exceedingly high temperature. If the junction temperature exceeds the OTP rising threshold, the whole chip shuts down. It is a non-latch protection and once the junction temperature drops below with the hysteresis threshold, the device resumes operation by initiating a soft-start.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage.

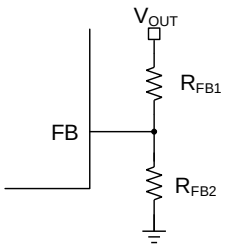


Figure 11: V_{OUT} Setting Resistor

If R_{FB1} is determined, then R_{FB2} can be calculated with below formula:

$$R_{FB2}=\frac{R_{FB1}}{\frac{V_{OUT}}{0.8V}-1} \quad (7)$$

Table 5: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
12	160 (1%)	11.5 (1%)
33	324(1%)	8.06(1%)

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. Use ceramic capacitors for the best performance. Place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R dielectrics are recommended due to their stable temperature characteristics and low ESR.

The input capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current (I_{CIN_MAX}). The input ripple current (I_{CIN}) can be estimated with Equation (8):

$$I_{CIN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (9):

$$I_{CIN}=\frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating that exceeds half the maximum load current (I_{LOAD_MAX}).

The input capacitance value determines converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, then select C_{IN} to meet the system's specification.

ΔV_{IN} can be estimated with Equation (10):

$$\Delta V_{IN}=\frac{I_{OUT}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (11):

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{f_{SW}\times C_{IN}} \quad (11)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (12):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}})\times(R_{ESR}+\frac{1}{8\times f_{SW}\times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}. The capacitance also dominates ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (13):

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_{SW}^{2}\times L\times C_{OUT}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (13)$$

When using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (14):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}})\times R_{ESR} \quad (14)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching V_{IN}. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}; however, a larger-value inductor has a larger physical size, a higher series resistance, and a lower saturation current. Recommend to choose an inductor so that the peak-to-peak inductor ripple current (ΔI_L) is between 20% and 50% of the maximum output

current (I_{OUT_MAX}). The peak inductor current (I_{L_PEAK}) should be below the saturation current. The inductance (L) can be calculated with Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Choose an inductor that will not saturate under the maximum I_{L_PEAK}. I_{L_PEAK} can be calculated with Equation (16):

$$L_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

PCB Layout Guidelines

For a controller, the layout is always an important step in design. A poor layout would result in reduced performance, EMI problems, resistive loss and even system instability. Following step would help to guarantee a good layout design:

1. Input power loop between input capacitor, high-side MOSFET and low-side MOSFET should be as small as possible, SW trace should be as short and wide as possible. At the same time, one small decoupling capacitor should be placed close to the IC's VDRV pin and PGND pin.
2. Feedback loop should be far away from noise source such as SW trace, the feedback divider resistor should be as close as possible to FB pin.
3. VCC capacitors should be placed as close as possible to VCC pin.
4. A short and wide type resistor is recommended for current sense when shunt resistor current sensing is used.
5. Layout the gate drive traces as directly as possible. Layout the forward and return traces close together, either running side by side or on top of each other on adjacent layers to minimize the inductance of the gate drive path.
6. Route the sensing traces (ISENS+, ISENS-) in paired way with smallest closed area. Avoid crossing noisy areas such as SW or high-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
7. VOUT for feedback sense and connection to VOUT pin should be layout separately to avoid the power supply for Vdrv interrupt the feedback.
8. The ground return of input/output capacitor should be tied close with large GND copper area.
9. For heavy load, suggest layout large copper, more layers and more vias for heat sink.

Figure 12 shows the recommended components place for MP9931. For the layout, the corresponding schematic can be found on Figure 13.

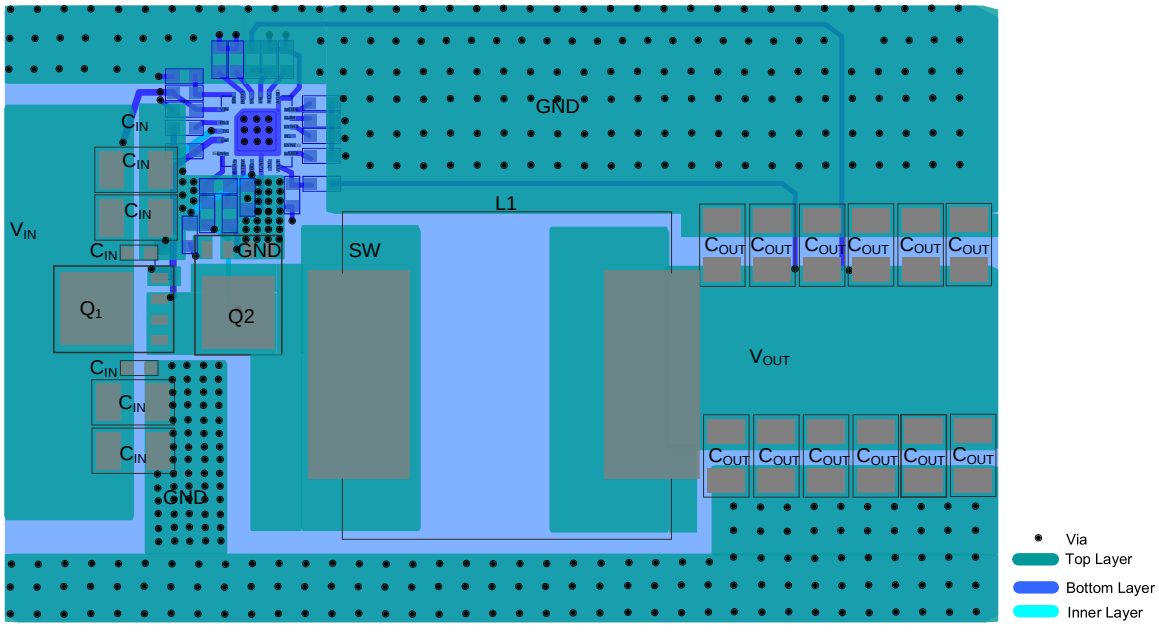


Figure 12: Layout Recommendation

Design Example

Below is a design example following the application guidelines for the following specifications:

Table 6: Design Example

V_{IN}	48V
V_{OUT}	12V
I_{OUT}	0A-20A

The typical application circuit for V_{OUT} = 12V in Figure 13 shows the detailed application schematic, and it is the basis for the typical performance waveforms. For more detailed device applications, please refer to the related Evaluation Board Datasheets

TYPICAL APPLICATION CIRCUITS

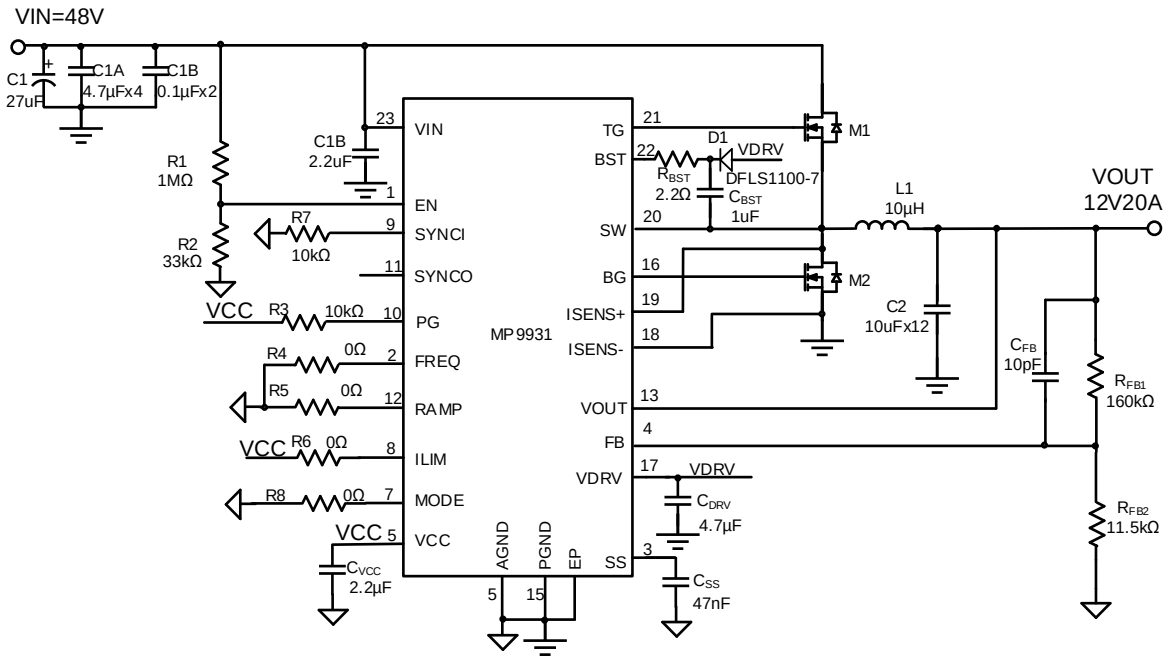


Figure 13: Application Circuit for 12V Output

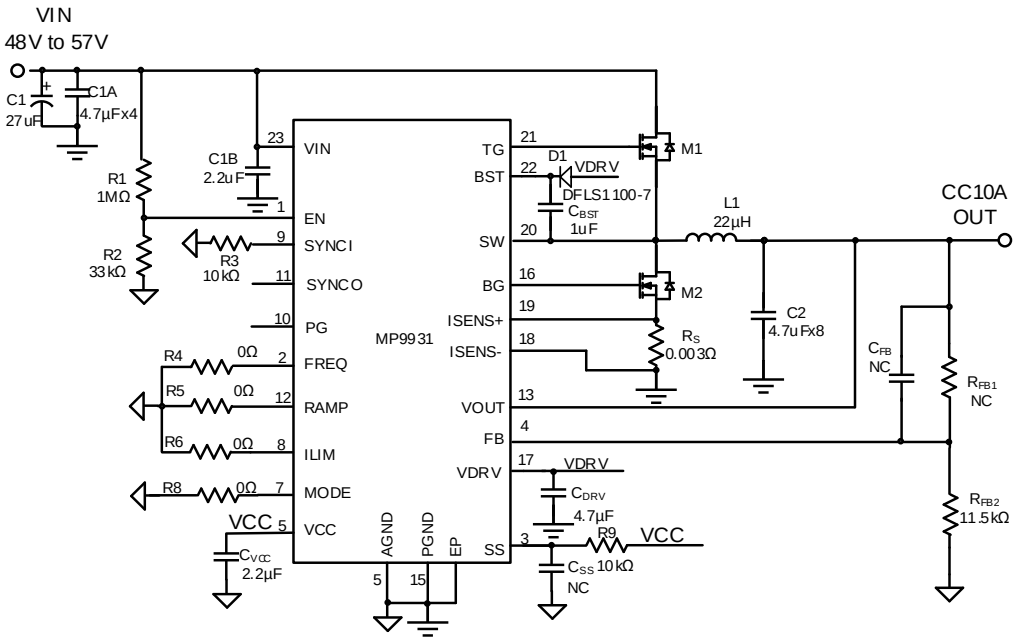
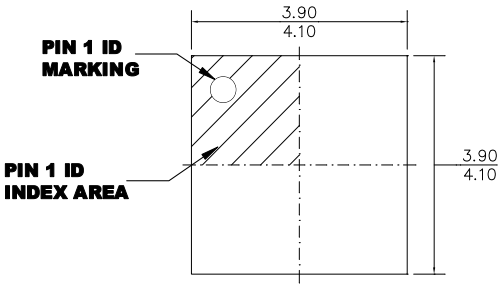


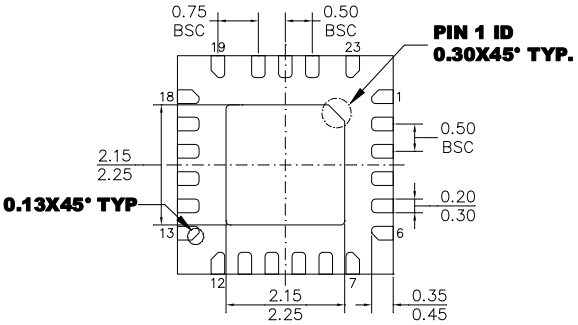
Figure 14: Application Circuit for CC10A Output

PACKAGE INFORMATION

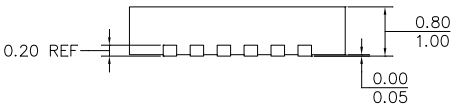
QFN-23 (4mmx4mm)



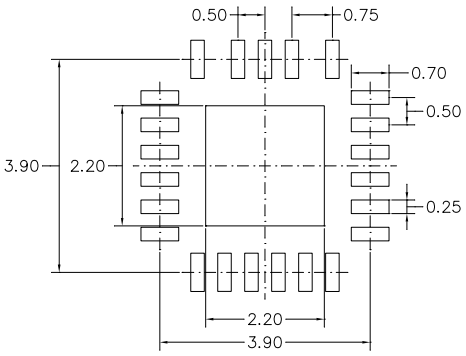
TOP VIEW



BOTTOM VIEW



SIDE VIEW

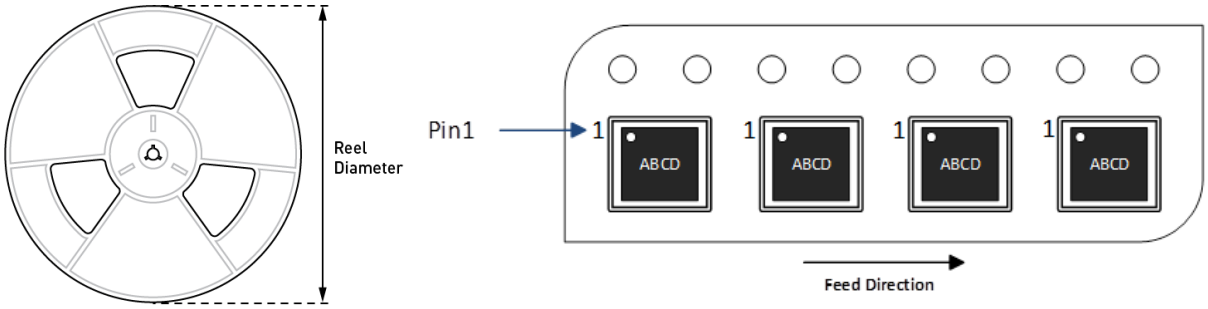


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9931GR-Z	QFN-23 (4mmx4mm)	5000	N/A	N/A	13 in.	12 mm	8 mm