TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX CAN transceiver with support for CAN FD and fail-safe functionality

1. DESCRIPTION

The TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX CAN transceiver series conforms to the ISO 11898-2 (2016) standard for the high-speed physical layer of Controller Area Networks (CAN). These transceivers are tailored for CAN FD networks, supporting data rates of up to 5 Mbps (Megabits per second). They incorporate an auxiliary power input for adjusting I/O levels, enabling customization of input pin thresholds and RXD output levels.

For enhanced energy efficiency, the series includes a standby mode. Additionally, all devices in this series provide a wide array of protection features, bolstering the durability of both the devices and the network. These protection features further contribute to the overall reliability and robustness of the CAN communication system.

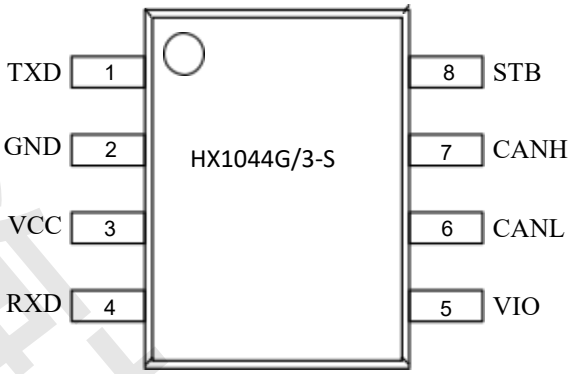
2. FEATURES

- Functions within a single supply voltage span of +1.4V to +5.5V
- ESD Protection Levels:
  - CDM (Charged Device Model) Classification: ±1500V
  - CANH/CANL HBM (Human Body Model) Rating: ±16kV
- Compliance with Physical Layer Standards:
  - ISO 11898-2:2016 and ISO 11898-5:2007
- EMC Performance:
  - Supports SAE J2962-2 and IEC 62228-3 (up to 500kbps) without the need for common-mode chokes
- I/O Voltage Range Compatibility:
  - Supports 3.3V and 5V MCUs
- Additional Features:
  - Standby Mode Support
  - VIO Compatibility
  - Ideal Passive Behavior when Unpowered: High-impedance state on bus and logic pins (no load), enabling seamless power-up/power-down operation on the bus and RXD output
- Protection Characteristics:
  - Bus Fault Protection: ±58V
  - IEC ESD Protection up to ±15kV
  - Undervoltage Protection on VCC and VIO power supplies
  - Transmitter Dominant Timeout (TXD DTO) for data rates as low as 10kbps
  - Thermal Shutdown Protection (TSD)
- Receiver Common-Mode Input Voltage Range: ±30V
- Standard Signal Delay: 110 nanoseconds
- Operating temperature range at the junction: from –55°C to 150°C.
- Offered in an SOP-8 packaging format.

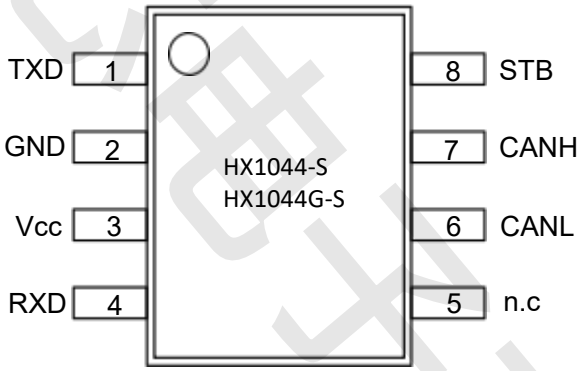
3. APPLICATIONS

- Telecommunication base station
- Two-wheeled vehicle
- Energy storage

4. PIN CONFIGURATIONS AND FUNCTIONS



(TOP VIEW)



Pin Functions			
NAME	**TYPE**	**DESCRIPTION**	
1	TXD	Digital Input	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Ground connection
3	VCC	Power	Transceiver 5V supply voltage
4	RXD	Digital Output	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Power	Support 2.7V to 5.5V VIO. Only for HX1044G/3-S VQ
5	n.c	Not connected	not connected; in HX1044-S/HX1044G-S version
6	CANL	Bus I/O	Low-level CAN bus input/output line
7	CANH	Bus I/O	High-level CAN bus input/output line
8	STB	Digital Input	Standby Mode control input (active high)
---	VIO	Power	Transceiver I/O level shifting supply voltage

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	5V bus supply voltage range, VCC	All devices	−0.3	6	V
	I/O level-shifting voltage range, VIO	Devices with the "V" suffix	−0.3	6	V
	CAN bus I/O voltage range (CANH, CANL), VBUS		−58	58	V
	Max differential voltage between CANH and CANL,V(Diff)		−58	58	V
	Logic input terminal voltage range (TXD, S),V(Logic_Input)	All devices	−0.3	6	V
	Logic output terminal voltage range (RXD),V(Logic_Output)		−0.3	+7 and VI ≤ VIO	V
Current	RXD (receiver) output, IO(RXD)		−8	8	mA
Temperature	Junction, TJ		−55	150	°C
	Storage, Tstg		−65	150	°C

5.2 ESD RATINGS

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge		Human-body model (HBM) CANH/CANL, per ANSI/ESDA/JEDEC JS-001(1)	±16000	V
		Human-body model (HBM) Other PINs, per ANSI/ESDA/JEDEC JS- 001(1)	±8000	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(1)	±1500	

NOTES

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
5V Bus Supply Voltage Range	VCC	4.5		5.5	V
I/O Level-Shifting Voltage Range	VIO	2.8		5.5	V
RXD Terminal HIGH Level Output Current	IOH(RXD)	−2			mA
RXD Terminal LOW Level Output Current	IOL(RXD)			2	mA

5.4 THERMAL INFORMATION

PARAMETER	SYMBOL	TBD	UNITS
Junction-to-Ambient Thermal Resistance	RθJA	TBD	°C/W
Junction-to-Board Thermal Resistance	RθJB	TBD	°C/W
Junction-to-Top Characterization Parameter	ψJT	TBD	°C/W
Junction-to-Board Characterization Parameter	ψJB	TBD	°C/W

Junction-to-Case (Top) Thermal Resistance	RθJC(top)	TBD	°C/W
Junction-to-Case (Bottom) Thermal Resistance	RθJC(bot)	---	°C/W

5.5 ELECTRICAL CHARACTERISTICS

TA = –40°C to 125°C, VCC = 4.5V to 5.5V, VIO = 2.8V to 5.5V, RL = 60Ω, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
5V Supply Current	ICC	Normal mode (dominant), TXD = 0V, RL = 60Ω , CL =open, RCM = open, S = 0V, typical bus load		37		mA
		Normal mode (dominant), TXD = 0V, RL = 50Ω , CL =open, RCM = open, S = 0V, high bus load		38		mA
		Normal mode (dominant – with bus fault), TXD = 0V, S = 0V, CANH = – 12V, RL =open, CL= open, RCM = open		43		mA
		Normal mode (recessive), TXD = VCC or VIO, RL = 50Ω , CL = open, RCM = open, S = 0V		1.3		mA
		STB mode, devices with the "V" suffix (I/O level-shifting), VCC not needed in Standby mode, TXD = VIO, RL = 50Ω , CL = open, RCM = open, S = VIO		0.5		mA
I/O Supply Current	IIO	Normal mode, recessive, RXD floating, TXD = STB = 0V		55		µA
		Normal mode, Dominant, RXD floating, TXD = STB = 0V		145		µA
		Standby mode: RXD floating, TXD = STB = VIO, VCC = 0 or 5.5V		10	13.5	µA
Rising Undervoltage Detection on VCC for Protected Mode	UVVCC	All devices		4.2	4.4	V
Falling Undervoltage Detection on VCC for Protected Mode			3.5	4.0	4.25	V
Hysteresis Voltage on UVVCC	VHYS(UVVCC)			200		mV
Undervoltage Detection on VIO for Protected Mode	UVVIO	Devices with the "V" suffix (I/O level-shifting); rising under voltage detection on VIO (devices with VIO)		2.1	2.2	V
		Devices with the "V" suffix (I/O level-shifting); falling under voltage detection on VIO (devices with VIO)	1.7	1.8	1.95	V
Hysteresis Voltage on UVVIO for Protected Mode	VHYS(UVVIO)	Devices with the "V" suffix (I/O level-shifting)		258		mV
STB TERMINAL (MODE SELECT INPUT)						
High-Level Input Voltage	VIH	Devices with the "V" suffix (I/O level-shifting)	0.7 × VIO			V
		Devices without the "V" suffix (5V only)	2			V
Low-Level Input Voltage	VIL	Devices with the "V" suffix (I/O level-shifting)			0.3 × VIO	V
		Devices without the "V" suffix (5V only)			0.8	V
High-Level Input Leakage Current	IIH	S = VCC = VIO = 5.5V	–2		2	µA
Low-Level Input Leakage Current	IIL	S = 0V, VCC = VIO = 5.5V	–15	0	–1	µA
Unpowered Leakage Current	Ilkg(OFF)	S = 5.5V, VCC = VIO = 0V	–1	0	1	µA
TXD TERMINAL (CAN TRANSMIT DATA INPUT)						
High-Level Input Voltage	VIH	Devices with the "V" suffix (I/O level-shifting)	0.7 × VIO			V

Low-Level Input Voltage	VIL	Devices with the "V" suffix (I/O level-shifting)			0.3 × VIO	V
High-Level Input Leakage Current	IIH	TXD = VCC = VIO = 5.5V	–2.5	0	1	µA
Low-Level Input Leakage Current	IIL	TXD = 0V, VCC = VIO = 5.5V	–200	–150	–60	µA
Unpowered Leakage Current	Ilkg(OFF)	TXD = 5.5V, VCC = VIO = 0V	–1	0	1	µA
Input Capacitance	CI	VIN =0.4 × sin(2 × π × 2 × 106 × t) + 2.5V		5		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)						
High-Level Output Current	IOH	VRXD = VIO - 0.4V	-8	-3	-1	mA
						mA
Low-Level Output Current	IOL	VRXD = 0.4V, bus dominant	1		12	mA
DRIVER ELECTRICAL CHARACTERISTICS						
Bus Output Voltage (Dominant), CANH	VO(DOM)	TXD = 0V, STB = 0V, 50Ω ≤ RL ≤ 65Ω, CL = open, RCM = open	2.75		4.5	V
Bus Output Voltage (Dominant), CANL			0.5		2.25	V
Bus Output Voltage (Recessive), CANH and CANL	VO(REC)	TXD = VCC or VIO, VIO = VCC, S = 0V, RL = open (noload), RCM = open	2	0.5 × VCC	3	V
Differential Output Voltage (Dominant), CANH - CANL	VOD(DOM)	TXD = 0V, STB = 0V, 50Ω ≤ RL < 65Ω, CL = open, RCM = open	1.5		3	V
		TXD = 0V, STB = 0V, 45Ω ≤ RL ≤ 70Ω, CL = open, RCM = open	1.4		3	V
		TXD = 0V, STB = 0V, RL = 2240Ω, CL = open, RCM = open	1.5		5	V
Differential Output Voltage (Recessive), CANH - CANL	VOD(REC)	TXD = VCC, STB = 0V, RL = 60Ω, CL = open, RCM = open	–120		12	mV
		TXD = VCC, STB = 0V, RL = open (no load), CL =open, RCM = open	–40		40	mV
Output Symmetry (Dominant or Recessive) (VO(CANH) + VO(CANL)) / VCC	VSYM	STB at 0V, Rterm = 60Ω , Csplit = 4.7nF, CL = open, RCM = open, TXD = 1MHz	0.9		1.1	V/V
DC Output Symmetry (Dominant or Recessive) (VCC – VO(CANH) –	VSYM_DC	STB = 0V, RL = 60Ω, CL = open, RCM = open	–0.4		0.4	V
Short-Circuit Steady-State Output Current, Dominant, Normal Mode	IOS(SS_DOM)	STB at 0V, VCANH = -5V to 40V, CANL = open, TXD = 0V	–100			mA
		STB at 0V, VCANL = –5V to 40V, CANH = open, TXD = 0V			100	mA
Short-Circuit Steady-State Output Current, Recessive, Normal Mode	IOS(SS_REC)	STB at 0V, –27V ≤ VBUS ≤ 32V, where VBUS = CANH = CANL, TXD = VCC	–5		5	mA

Notes

All typical values are at 25°C and supply voltages of VCC = 5V and VIO = 5V (if applicable), RL = 60Ω.

5.6 SWITCHING CHARACTERISTICS

TA = –40°C to 125°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER ELECTRICAL CHARACTERISTICS						
Common-Mode Range, Normal Mode	VCM	STB = 0V	–30		30	V
Positive-Going Input Threshold Voltage, Normal Mode	VIT+	STB = 0V, –20V ≤ VCM ≤ +20V			900	mV
Negative-Going Input Threshold Voltage, Normal Mode	VIT–		500			mV
Positive-Going Input Threshold Voltage, Normal Mode	VIT+	STB = 0V, –30V ≤ VCM ≤ +30V			1000	mV
Negative-Going Input Threshold Voltage, Normal Mode	VIT–		400			mV
Hysteresis Voltage (VIT+ – VIT –), Normal Mode	VHYS	STB = 0V			120	mV

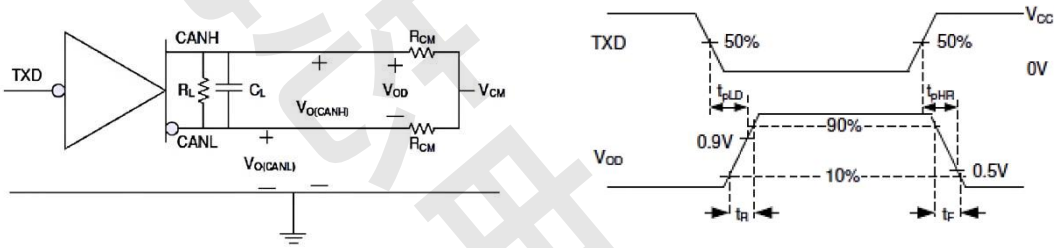
Common-Mode Range, Standby Mode	VCM	Devices with the "V" suffix (I/O level-shifting), STB = VIO, 4.5V≤ VIO ≤ 5.5V	− 12		12	V
		Devices with the "V" suffix (I/O level-shifting), STB = VIO, 3.0V ≤ VIO ≤ 4.5V	−2		7	V
		Devices without the "V" suffix (5V only), STB= VCC	− 12		12	V
Input Threshold Voltage, Standby Mode	VIT(STANDBY)	STB = VCC or VIO	400		1150	mV
Power-Off (Unpowered) Bus Input Leakage Current	ILKG(IOFF)	CANH = CANL = 5V, VCC = VIO = 0V			4.8	µA
Input Capacitance to Ground (CANH or CANL)	CI	TXD = VCC, VIO = VCC		24	30	pF
Differential Input Capacitance (CANH to CANL)	CID	TXD = VCC, VIO = VCC		12	15	pF
Differential Input Resistance	RID	TXD = VCC = VIO = 5V, S = 0V, −30V ≤ VCM ≤+30V	40		90	kΩ
Input Resistance (CANH or CANL)	RIN		20		45	kΩ
Input Resistance Matching: [1 − RIN(CANH) / RIN(CANL)] × 100%	RIN(M)	VCANH = VCANL = 5V	− 1%		1%	kΩ
DEVICE SWITCHING CHARACTERISTICS						
Total Loop Delay, Driver Input (TXD) to Receiver Output (RXD), Recessive to Dominant	tPROP(LOOP1)	STB = 0V, RL = 60Ω , CL = 100pF, CL(RXD) = 15pF		60	68	ns
Total Loop Delay, Driver Input (TXD) to Receiver Output (RXD), Dominant to Recessive	tPROP(LOOP2)			62	73	ns
Mode Change Time, From Normal to STB or From STB to Normal	tMODE			17	21	µs
Long Filter Time for Valid Wake-Up Pattern	tWK_FILTER		0.5		1.8	µs
Short Filter Time for Valid Wake-Up Pattern	tWK_FILTER		0.5		5	µs
DRIVER SWITCHING CHARACTERISTICS						
Propagation Delay Time, High TXD to Driver Recessive (Dominant to Recessive)	tpHR	STB = 0V, RL = 60Ω , CL = 100pF, RCM = open		80		ns
Propagation Delay Time, Low TXD to Driver Dominant (Recessive to Dominant)	tpLD			70		ns
Pulse Skew (|tpHR − tpLD |)	tsk(p)			20		ns
Differential Output Signal Rise Time	tR			30		ns
Differential Output Signal Fall Time	tF			50		ns
Dominant Timeout	tTXD_DTO	STB = 0V, RL = 60Ω , CL = open	1.2		4	ms
RECEIVER SWITCHING CHARACTERISTICS						
Propagation Delay Time, BusRecessive Input to High Output (Dominant to Recessive)	tpRH	STB = 0V, CL(RXD) = 15pF		60		ns
Propagation Delay Time, Bus Dominant Input to Low Output (Recessive to Dominant)	tpDL			65		ns
RXD Output Signal Rise Time	tR			10		ns
RXD Output Signal Fall Time	tF			10		ns
FD TIMING PARAMETERS						
Bit Time on CAN Bus Output Pins with tBIT(TXD) = 500ns, All Devices	tBIT(BUS)	STB = 0V, RL = 60Ω , CL = 100pF, CL(RXD) = 15pF, ΔtREC = tBIT(RXD) − tBIT(BUS)	435		530	ns
Bit Time on CAN Bus Output Pins with tbit(TXD) = 200ns, G Device			155		210	ns
Bit Time on RXD Output Pins with tbit(TXD) = 500ns, All Devices	tBIT(RXD)		400		550	ns

Bit Time on RXD Output Pins with tbit(TXD) = 200ns, G Device Variants Only			120		220	ns
Receiver Timing Symmetry with tbit(TXD) = 500ns, All Devices	ΔtREC		−65		40	ns
Receiver Timing Symmetry with tbit(TXD) = 200ns, G Device Variants Only			−45		15	ns

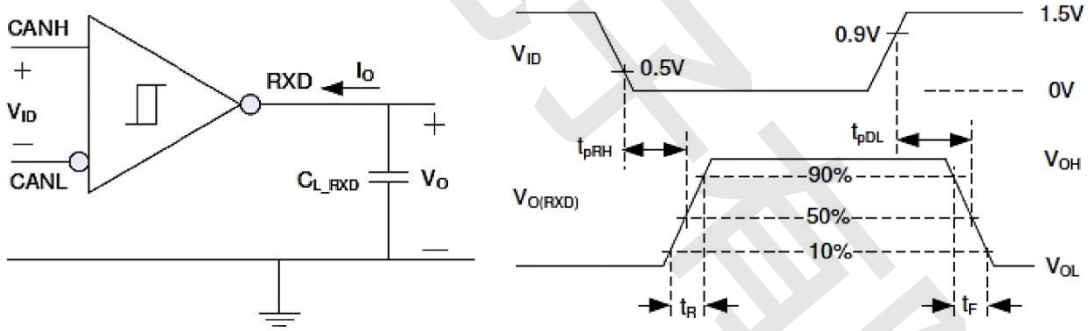
Notes

All typical values are at 25°C and supply voltages of VCC = 5V and VIO = 5V (if applicable), RL = 60Ω

6. Parameter measurement information

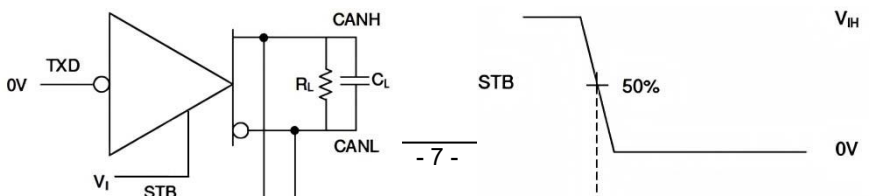


Driver Test Circuit and Measurement

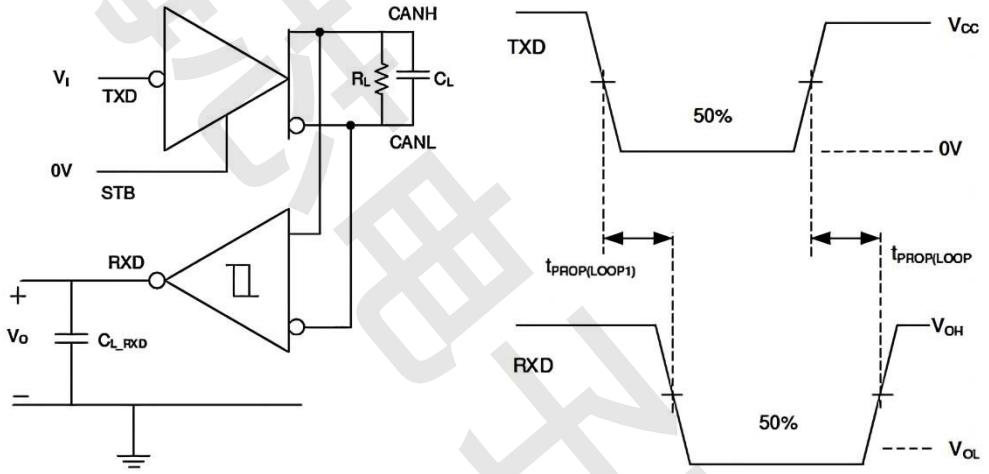


Receiver Test Circuit and Measuremen

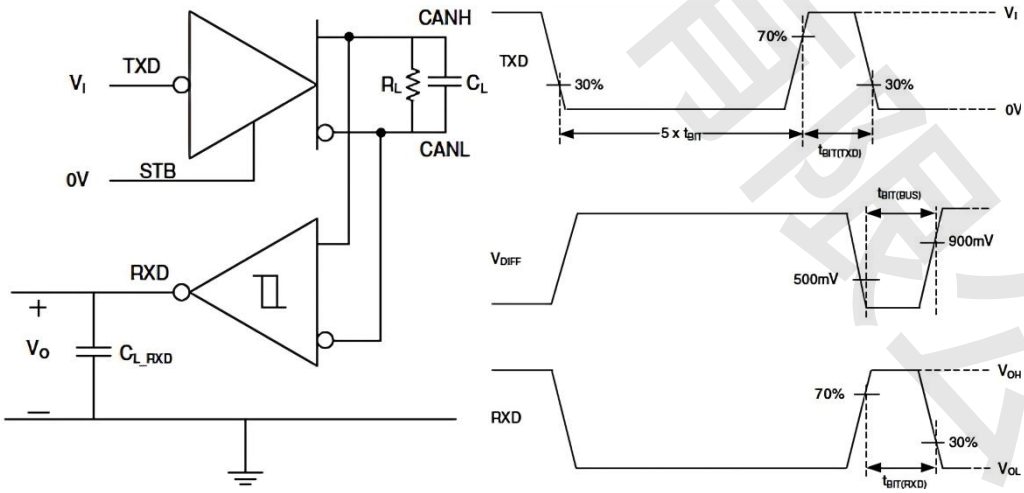
Receiver Differential Input Voltage Threshold Test				
INPUT			OUTPUT	
VCANH	VCANL	|VID |	RXD	
−29.5V	−30.5V	1000mV	L	VOL
30.5V	29.5V	1000mV	L	
− 19.55V	−20.45V	900mV	L	
20.45V	19.55V	900mV	L	
− 19.75V	−20.25V	500mV	H	VOH
20.25V	19.75V	500mV	H	
−29.8V	−30.2V	400mV	H	
30.2V	29.8V	400mV	H	
Open	Open	X	H	



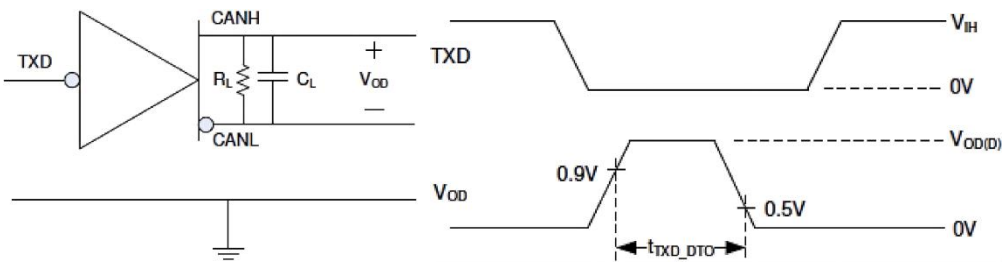
t_{MODE} Test Circuit and Measurement



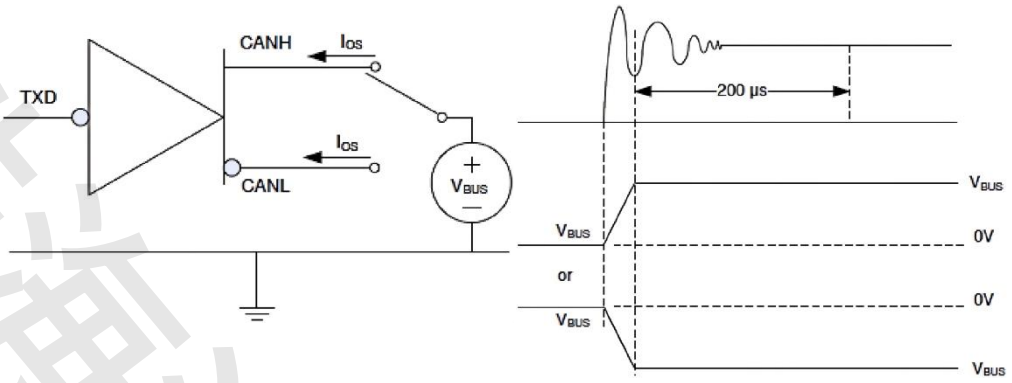
$T_{PROP(LOOP)}$ Test Circuit and Measurement



CAN FD Timing Parameter Measurement



TXD Dominant Timeout Test Circuit and Measurement



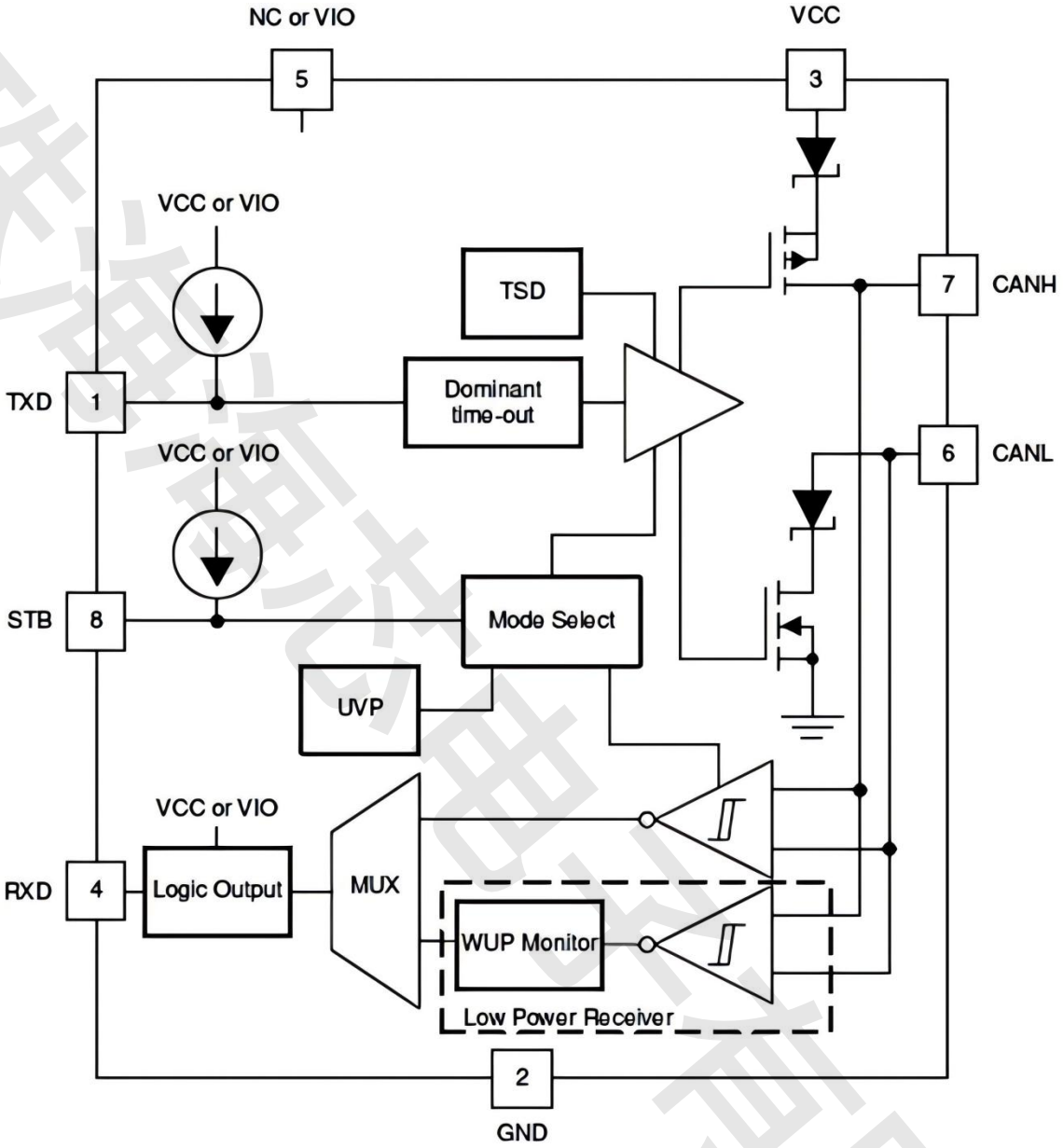
Driver Short Circuit Current Test and Measurement

7. Detailed description

7.1 Overview

These CAN transceivers adhere to the ISO 11898-2 (2016) standard for the high-speed CAN (Controller Area Network) physical layer. They are specifically engineered for CAN FD networks that exceed 1 Mbps data rates, offering enhanced timing margins for higher data transfer rates in long-distance and high-load scenarios. These devices incorporate numerous protection features that bolster the robustness of both the transceivers themselves and the CAN network as a whole.
At TA=+25oC, VS=+5V, and RL=100KΩ connected to VS/2, unless otherwise noted.

7.2Functional Module Block Diagram

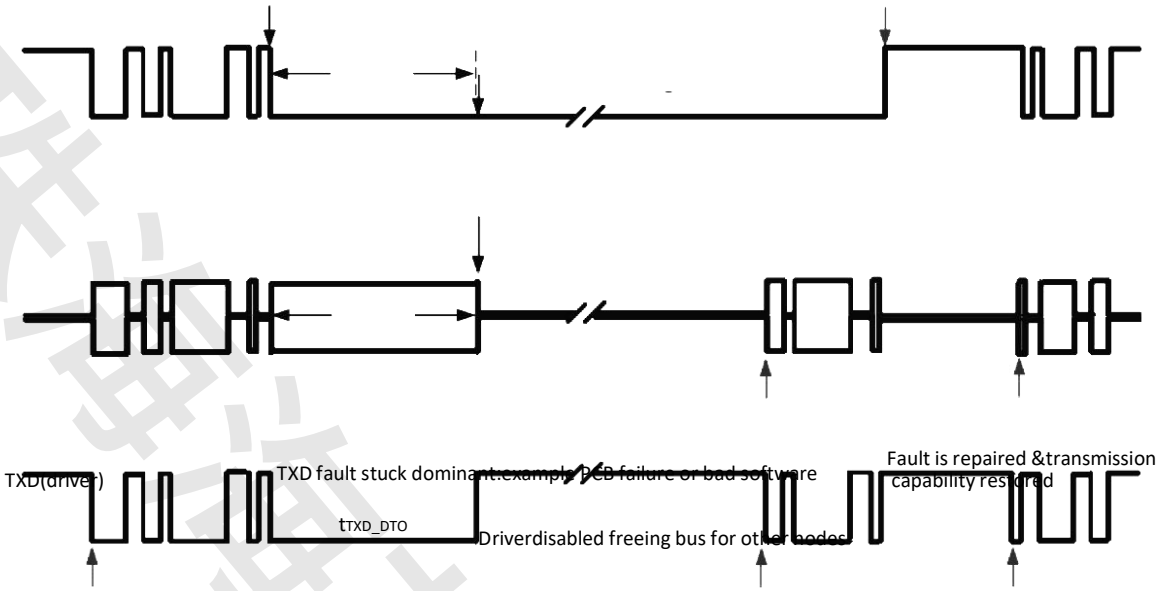


Functional Block Diagram

7.3 Feature Description

7.3.1 TXD Dominant Timeout (DTO)

During normal mode, which is the sole mode where the CAN driver is active, the TXD DTO (Dominant Timeout) circuitry prevents the transceiver from blocking network communication in the event of a hardware or software fault, where TXD remains in the dominant state for longer than the timeout period, tTXD_DTO. The DTO circuit timer initiates upon the falling edge of TXD. If a rising edge is not observed before the timeout expires, the DTO circuitry disables the CAN bus driver, thereby releasing the bus for communication among other nodes on the network. When a recessive signal is detected on the TXD terminal, the CAN driver is reactivated, clearing the TXD DTO condition. The receiver and RXD terminal continue to reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during the TXD dominant timeout period.



Example Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the TXD DTO (Dominant Timeout) circuitry imposes a limit on the minimum possible transmission data rate of the device. In the worst-case scenario, the CAN protocol permits up to 11 consecutive dominant bits (on TXD), with 5 consecutive dominant bits immediately following an error frame. This, in conjunction with the minimum value of tTXD_DTO, restricts the minimum achievable data rate. The minimum data rate can be calculated using the following formula:

Minimum Data Rate = 11 / tTXD_DTO.

7.3.2 Thermal Shutdown (TSD)

When the junction temperature of the device rises above the thermal shutdown threshold (TTSD), the CAN driver circuitry is automatically deactivated by the device itself, effectively cutting off the signal transmission from TXD to the bus. During this thermal shutdown period, the CAN bus terminals are driven to the recessive state, whereas the pathway from the receiver to RXD remains functional. The shutdown condition is resolved once the junction temperature decreases to below the thermal shutdown hysteresis temperature (TTSD_HYS), which is set at a lower level compared to the device's thermal shutdown temperature (TTSD).

7.3.3 Under-Voltage Lockout (UVLO)

The power supply terminals are equipped with under-voltage detection functionality, which can put the device into a protection mode. This can safeguard the bus during under-voltage events occurring on the VCC or VIO power terminals.

Undervoltage Lockout I/O Level Shifting Devices (Devices with the "V" Suffix)				
VCC	**VIO**	**DEVICE STATE**	**BUS OUTPUT**	**RXD**
> UVVCC	> UVVIO	Normal	Per TXD	Mirrors Bus(1)
< UVVCC	> UVVIO	Protected	High Impedance	High (Recessive)
> UVVCC	< UVVIO	Protected	High Impedance	High Impedance
< UVVCC	< UVVIO	Protected	High Impedance	High Impedance

Notes

(1) Mirror bus status: It is low if the CAN bus is dominant; it is high if the CAN bus is recessive.

(2) After the under-voltage condition is cleared and the power supply returns to a valid level, the device will usually resume normal operation within 50μs.

7.3.4 Passive device

This device is designed to be "ideally passive" or "unloaded" on the CAN bus when unpowered. When the device is not energized, the bus terminals (CANH, CANL) exhibit extremely low leakage currents to prevent any degradation of the bus load. This is crucial in scenarios where some nodes of the network are powered down while the rest of the network remains operational. Additionally, when the device is unpowered, the logic terminals also maintain extremely low leakage currents to avoid loading other circuits that may remain energized.

7.3.5 Floating terminal

These critical terminals feature internal pull-up resistors that ensure the device is in a defined state when the terminals are not connected. Specifically, the TXD terminal is pulled up to either VCC or VIO, thereby establishing a recessive input level when floating. Analogously, if the S terminal remains disconnected, it is pulled down to compel the device into its normal operational mode.

7.3.6 CAN bus short circuit current limiting

The device incorporates two protection mechanisms to limit short-circuit current during CAN bus line faults: driver current limitation (in both dominant and recessive states) and TXD dominant state timeout, preventing persistent high short-circuit current in the dominant state during system faults. During CAN communication, the bus alternates between dominant and recessive states, hence the short-circuit current can be viewed as either an instantaneous current during each bus state or an average current over both states. For system current (power) and power considerations in terminal resistance and common-mode choke ratings, the average short-circuit current is used. The ratio of dominant to recessive bits is determined by the CAN frame data, alongside protocol and PHY factors that enforce either recessive or dominant states at specific times, including:

Control fields with set bits
Bit stuffing
Interframe spacing
TXD dominant timeout (for fault condition mitigation)

These factors ensure minimal recessive time on the bus, even when the data field contains a high proportion of dominant bits. The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current can be calculated using the formula:

$$IOS(AVG) = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC]$$

Where:

IOS(AVG) represents the average short-circuit current.
%Transmit is the percentage of CAN messages transmitted by the node.
%Receive is the percentage of CAN messages received by the node.
%REC_Bits is the percentage of recessive bits in transmitted CAN messages.
%DOM_Bits is the percentage of dominant bits in transmitted CAN messages.
IOS(SS)_REC denotes the recessive steady-state short-circuit current.
IOS(SS)_DOM denotes the dominant steady-state short-circuit current.

Note: When determining the power ratings for terminal resistors and other network components, consider the short-circuit current of the network and potential fault scenarios.

7.3.7 Digital input and output

7.3.7.1 5V VCC with VIO I/O level conversion (devices with "V" suffix)

These devices employ a 5V VCC power supply for CAN drivers and high-speed receiver modules. These transceivers feature a secondary power supply for I/O level shifting (VIO), which is utilized to set the CMOS input thresholds for the TXD and STB pins, as well as the RXD high-level output voltage. Notably, the TXD pin is internally pulled up to VIO, whereas the STB pin is pulled down to GND.

7.4 Device functional mode

The device operates in two primary modes: Normal Mode and Silent Mode. The selection of the operating mode is made through the S input terminal.

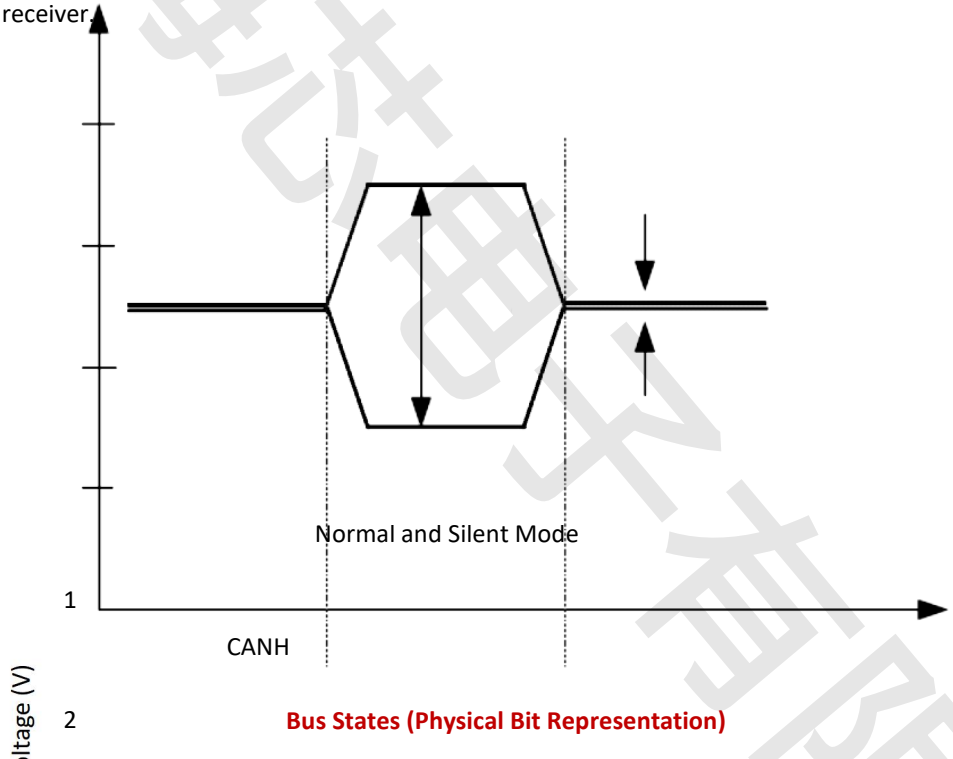
Operating Modes				
S TERMINAL	**MODE**	**DRIVER**	**RECEIVER**	**RXD TERMINAL**
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	STB Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State(1)

Note:

(1)Mirror bus state: If the CAN bus is dominant, it is low; if the CAN bus is recessive, it is high.

7.4.1 CAN Bus State

The CAN bus exhibits two states during the powered operation of devices: dominant and recessive. The dominant bus state corresponds to a logical low level on the TXD and RXD terminals when the bus is differentially driven. In contrast, the recessive bus state corresponds to a logical high level on the TXD and RXD terminals when the bus is biased to VCC/2 through the high-impedance internal input resistance (RIN) of the receiver.



Bus States (Physical Bit Representation)

The normal operating mode of the device is selected by setting the STB terminal to a low level, allowing the CAN driver and receiver to be fully operational and enabling bidirectional CAN communication. The driver converts digital inputs on the TXD into differential outputs on CANH and CANL, while the receiver translates differential signals from CANH and CANL into digital outputs on RXD.

7.4.2 Standby Mode

The Standby mode is activated by setting the STB terminal to a high level. In standby mode, the BUS end has very low leakage and power consumption. The chip is in the standby state.

7..4.3 Driver and Receiver Function Table

Driver Function Table					
DEVICE	**INPUTS**		**OUTPUTS**		**DRIVEN BUS STATE**
	STB(1)	**TXD(1)(2)**	**CANH(1)**	**CANL(1)**	
All Devices	L or open	L	H	L	Dominant
		H or open	Z	Z	Recessive
	H	X	Z	Z	Recessive

Notes

(1) H = high level, L = low level, X = irrelevant, Z = VCC / 2. For information about bus status and common mode bias, see CAN BUS STATES.
(2) The device has an internal pull-up to the VCC or VIO on the TXD terminal. If the TXD terminal is open, the terminal is pulled up and the transmitter remains hidden (non-driven).

Receiver Function Table			
DEVICE MODE	**CAN DIFFERENTIAL INPUTS VID = VCANH – VCANL**	**BUS STATE**	**RXD TERMINAL(1)**
Normal or STB	VID ≥ VIT+(MAX)	Dominant	L(2)
	VIT-(MIN) < VID < VIT+(MAX)	?	?(2)
	VID ≤ VIT-(MIN)	Recessive	H(2)
	Open (VID ≈ 0V)	Open	H

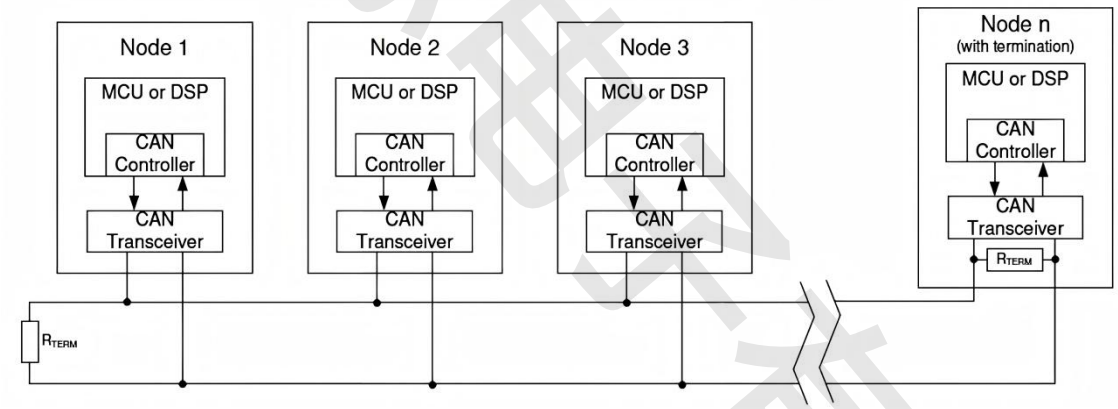
Notes
(1) H = high level, L = low level,?= indeterminacy.
(2) For information on the input thresholds, see the ELECTRICAL CHARACTERISTICS section.

8. Application and implementation

8.1 application message

These CAN transceivers are commonly used for applications with a host microprocessor or an FPGA, which includes the data link layer portion of the CAN protocol. The following are typical application configurations for both the 5V and 3.3V microprocessor applications. Display bus terminals are intended for illustrative purposes.

8.2 Typical application



Typical CAN Bus Application

8.2.1 design requirement； design requirements

8.2.1.1 Bus load, length, and number of nodes

The ISO 11898-2 standard specifies a maximum bus length of 40 meters and a maximum stub length of 0.3 meters. However, with meticulous design, users can achieve longer cables, extended stub lengths, and accommodate more bus nodes. For high node counts, transceivers with high input impedance, such as the TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series, are essential.

Numerous CAN organizations and standards have extended the application of CAN beyond the original ISO 11898-2, conducting systematic trade-offs in data rates, cable lengths, and parasitic loads on the bus. Examples of such specifications include ARINC825, CANopen, DeviceNet, and NMEA2000.

The TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series is specified to meet a 1.5V requirement under a 50Ω load, accounting for worst-case scenarios including parallel transceivers. The differential input resistance of the TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series is a minimum of 30kΩ. Connecting 100 TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series transceivers in parallel on a single bus equates to a worst-case differential load of 300Ω. When combined with a 60Ω termination, this 300Ω transceiver load results in an equivalent load of 50Ω, theoretically allowing up to 100 transceivers on a single bus segment. Nevertheless, CAN networks necessitate design margins for signal loss, parasitic loads, network imbalance, ground offsets, and signal integrity within the system and wiring, leading to a significantly lower practical maximum node count.

Bus lengths can also be extended beyond the original 40-meter limit set by ISO 11898 standards through careful system design and data rate trade-offs. For instance, the CANopen network design guidelines permit networks as long as 1 kilometer, albeit with adjustments to terminal resistances, cabling, a reduced node count of fewer than 64, and a notable decrease in data rates.

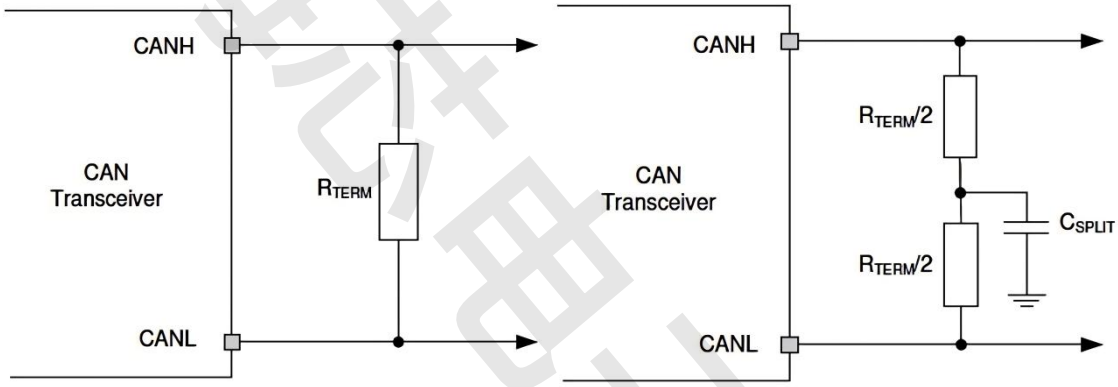
This flexibility in CAN network design represents one of the key advantages of various extensions and additional standards built upon the original ISO 11898-2 CAN standard. Employing this flexibility comes with the responsibility of meticulously designing networks and balancing these trade-offs.

8.2.2 Detailed design procedure

8.2.2.1 CAN Termination

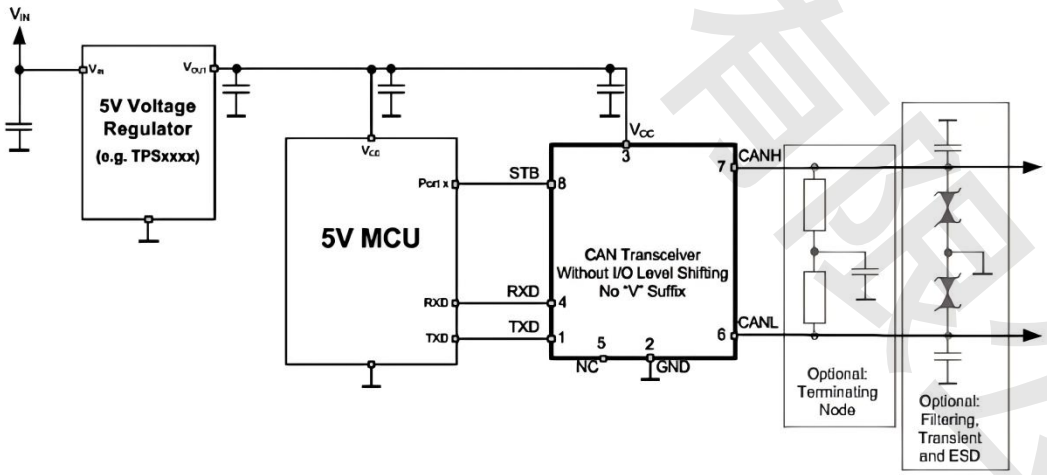
The ISO 11898 standard specifies the interconnection as twisted-pair cables (shielded or unshielded) with a characteristic impedance (Z0) of 120Ω. To prevent signal reflections, resistors equal to the line's characteristic impedance should be used to terminate both ends of the cable. The unterminated branch lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination can be located on the cable or within the nodes, but if nodes can be removed from the bus, care must be taken to ensure that two terminations are always present on the network.

Termination can consist of a single 120Ω resistor at each end of the bus, either mounted on the cable or within a terminating node. In cases where filtering and stabilization of the bus's common-mode voltage are required, split termination (as depicted in Figure CAN Bus Termination Concepts) can be employed. Split termination improves the network's electromagnetic emissions by eliminating fluctuations in the bus's common-mode voltage at the start and end of message transmission.

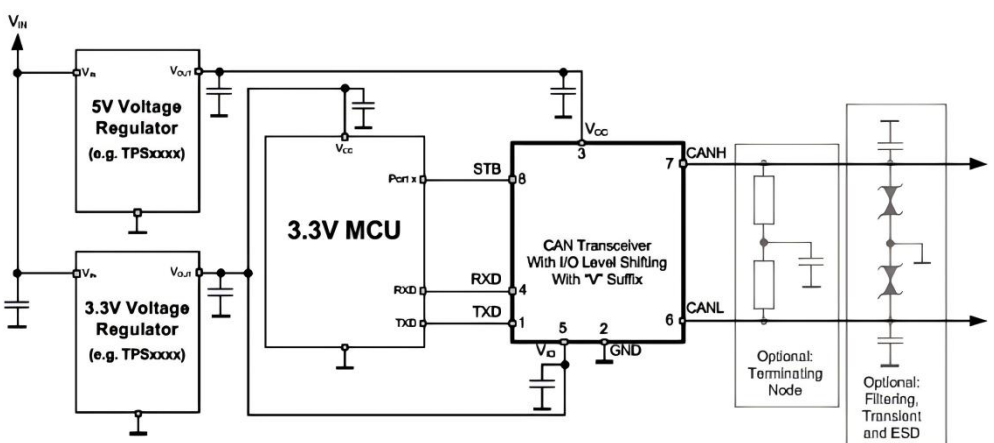


CAN Bus Termination Concepts

The TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX transceiver has variants suitable for only 5V applications and 3.3V microcontrollers requiring level conversion.



Typical CAN Bus Application Using 5V CAN Controller



Typical CAN Bus Application Using 3.3V CAN Controller

9. Power Supply Recommendations

These devices are designed to operate within a VCC input supply voltage range of 4.5V to 5.5V. Some devices feature an output level-shifting power input VIO, intended for a range between 3V and 5.5V. Both power inputs must be well-regulated. Large-capacity capacitors (typically 4.7µF) should be placed close to the CAN transceiver's primary VCC power output, while bypass capacitors (typically 0.1µF) should be positioned as close as possible to the device's VCC and VIO power terminals. This aids in reducing power supply voltage ripple at the output of switching mode power supplies and compensates for the resistance and inductance of PCB power planes and traces.

10. Layout Considerations

Robust and reliable bus node designs often necessitate the use of external transient protection devices to shield against EFTs and surge transients that may occur in industrial environments. Since ESD and transients have a wide frequency bandwidth ranging from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design. The TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series boasts high on-chip IEC ESD protection, but for higher levels of system-level immunity, external TVS diodes can be employed. TVS diodes and bus filter capacitors should be positioned as close as possible to the onboard connectors to prevent noise transients from propagating further into the PCB and system.

10.1 Layout Guidelines

Locate protection and filtering circuitry near the bus connector J1 to prevent issues like transients, ESD, and noise. Use a transient voltage suppressor (TVS) like D1 for extra protection. Optional bus filter capacitors (e.g., C4, C5) can also be added. A common-mode choke (CMC) can be placed between the transceiver and connector (not shown).
Route protection components along the signal path. Avoid diverting transient currents.
Use power (VCC) and ground planes for low inductance, noting high-frequency currents follow paths of least impedance.
Minimize inductance by using at least two vias for power and ground connections of capacitors and protection devices.
Place bypass and bulk capacitors close to the transceiver's power terminals (e.g., C1, C2 on VCC; C6, C7 on VIO).
For bus termination, use split termination with resistors (R6, R7) and a grounding capacitor (C3). Ensure terminating nodes stay connected to the bus. Series resistors (e.g., R2, R3, R4) on digital lines are optional for current limiting.
Terminal 1: R1 is optionally shown as the device's TXD input. If using an open-drain host processor, ensure compliance with bit timing into the device.
Terminal 5: For the "V" variants of the TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX series, bypass capacitors should be placed as close as possible to the pin (e.g., C6 and C7). For device options without VIO I/O level shifting, this pin is not internally connected and can be left floating or connected to any existing net, such as the split pin connection.
Terminal 8: Assuming mode terminal S will be used. If the device operates solely in normal mode, R4 is not required, and R5 can serve as a pull-down resistor to ground.

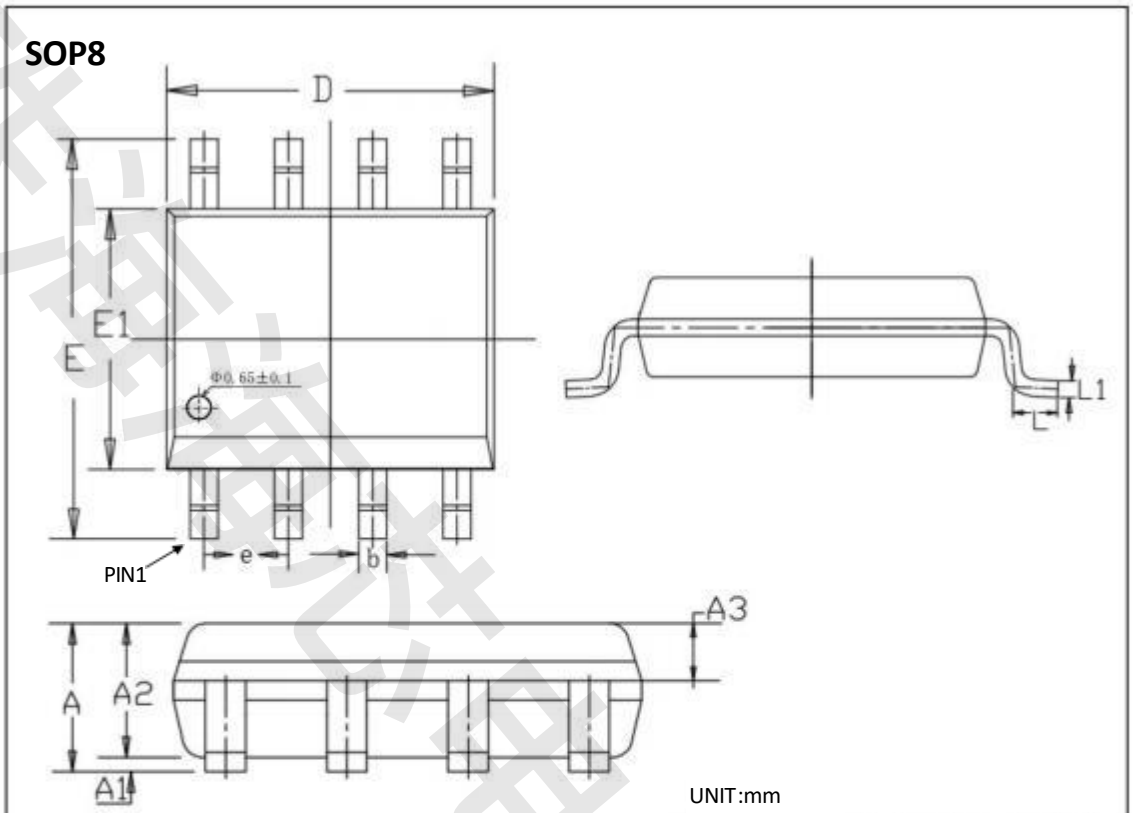
ORDERING INFORMATION

Ordering Information

Part Number	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
TJA1044GT-3Z-HX/TJA1044GT-1Z-HX/TJA1044T-1Z-HX	SOP-8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500

DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	–	0.25BSC	–